Homework 1 – Solutions

Problem 1

This question **is** as easy as it looks, no tricks here.

a. The delay from 'a' to 'b' is simply the delay of an inverter times the number of inverters which would be 10 ns.

b.

i. The period in this case is simply twice the delay around the loop, T=20 ns.

ii. The frequency is 1/T =50 MHz.

Problem 2

The delay of an RC circuit with a step input applied is:

$$V(t) = 1.2(1 - e^{-t/RC})$$

In our case, we are solving for *t*:

a.) For V(t)=0.6V:

$$t = 12.5(10^3) \times (100)10^{-15} \ln\left(\frac{1.2}{0.6}\right) = 12.5\square 10^{-10} \ln(2) = 866 ps$$

b.) 1.2V:

$$t = \infty$$

This circuit will never read 1.2V.

c.) The delay from 10% to 90% V_{DD}:

$$0.1 = (1 - e^{-t/RC})$$
$$\therefore t_{10\%} = 132 ps$$

$$0.9 = (1 - e^{-t/RC})$$
$$\therefore t_{90\%} = 2.88 ns$$

$$t = t_{90\%} - t_{10\%} = 2.88 - 0.132 = 2.75 ns$$

Problem 3

The delay for 0 and 0 uses the exponential rise/fall equation:

a.) For R_{DOWN}:

$$V(t) = 1.2\,e^{-t/RC} \qquad \therefore t_{DOWN} = 8.66ms$$

b.) For R_{UP}:

$$V(t) = 1.2\,(1 - e^{-t/RC}) \qquad \therefore t_{UP} = 20.8ms$$

c.) The ratio of delays is:

$$t_{RATIO} = \frac{t_{UP}}{t_{DOWN}} = \frac{20.8}{8.7} = 2.4$$

or 0.42 (depending on which way you did the ratio.)

Problem 4

a) The solution for the NMOS case is based on Example 2.4:

The equation for V_{T0} is: $V_{T0} = V_{FB} - 2\phi_F - \frac{Q_B}{C_{OX}}$

Calculate each individual component.

$$\phi_{Fp} = \frac{kT}{q}\ln\frac{n_i}{N_A} = -0.026\ln\frac{3\times10^{17}}{1.4\times10^{10}} = -0.44 \text{ V}$$

$$\phi_{GC} = \phi_{Fp} - \phi_{G(gate)} = -0.44 - 0.55 = -0.99 \text{ V}$$

$$\varepsilon_{OX} = 4\varepsilon_0 = 3.5\times10^{-13} \text{ F/cm} \qquad C_{OX} = 1.6\times10^{-6} \text{ F/cm}^2$$

$$Q_{B0} = 3\times10^{-7}\,C/cm^2 \qquad \frac{Q_{B0}}{C_{OX}} = \frac{3\times10^{-7}}{1.6\times10^{-6}} = 0.188 \text{ V}$$

$$\frac{Q_{OX}}{C_{OX}} = \frac{6\times10^{11}\times1.6\times10^{-19}}{1.6\times10^{-6}} = 0.06 \text{ V}$$

$$V_{TO} = -0.99 - (-0.88) - (-0.188) - 0.060 = +0.018 \text{ V}$$

Problem 4 - Continued

For the PMOS device:

$$\phi_{Fn} = \frac{kT}{q}\ln\frac{N_D}{n_i} = 0.026\ln\frac{3\times10^{17}}{1.4\times10^{10}} = 0.44 \text{ V}$$

$$\phi_{GC} = \phi_{Fn} - \phi_{G(gate)} = 0.44 + 0.55 = +0.99 \text{ V}$$

$$Q_{B0} = 3\times10^{-7} C/cm^2 \qquad \frac{Q_{B0}}{C_{OX}} = \frac{3\times10^{-7}}{1.6\times10^{-6}} = 0.188 \text{ V}$$

$$\frac{Q_{OX}}{C_{OX}} = \frac{6\times10^{11}\times1.6\times10^{-19}}{1.6\times10^{-6}} = 0.06 \text{ V}$$

$$V_{TO} = 0.99 - (0.88) - (0.188) - 0.060 = -0.138 \text{ V}$$

b) The magnitude of V_{T0} would be higher. Since the device is PMOS this means that V_{T0} is lowered. Since the only thing that's been changed is the doping of the gate, only ϕ_G changes.

The new V_{T0} then becomes:

$$V_{T0} = -0.11 - 0.88 - 0.188 - 0.6 = -1.24\text{V}$$

c) Since V_{T0} will be adjusted with implanted charge (Q_I):

$$\frac{Q_I}{C_{OX}} = 0.4 - 0.018$$

$$\frac{Q_I}{C_{OX}} = 0.382V$$

$$Q_I = (1.6\times10^{-6})(0.382V)$$

To calculate the threshold implant level N_I:

$$qN_I = |Q_I|$$

$$N_I = \frac{|Q_I|}{q}$$

For the NMOS device from part(a):

$$N_I = -\frac{Q_I}{q} = -\frac{0.6\times10^{-6}}{1.6\times10^{-19}} = 3.82\times10^{12} ions/cm^2 \textbf{ (p-type)}$$

Problem 4 - Continued

For the PMOS device from part(a):

$$N_I = -\frac{Q_I}{q} = -\frac{(1.6\times10^{-6})(0.4-0.138)}{1.6\times10^{-19}} = 2.62\times10^{12}\, ions/cm^2 \quad \textbf{(n-type)}$$

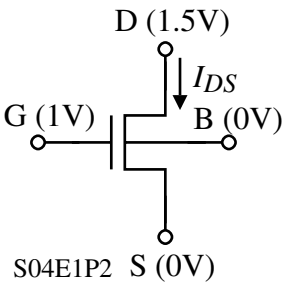
For the PMOS device from part(b):

$$N_I = -\frac{Q_I}{q} = -\frac{(1.6\times10^{-6})(1.24-0.4)}{1.6\times10^{-19}} = 8.4\times10^{12}\, ions/cm^2 \quad \textbf{(p-type)}$$

d) The advantage of having the gate doping be n^+ for NMOS and p^+ for PMOS could be seen from analysis above. Doping the gates in such a way leads to devices with lower threshold voltages, but enables the implant adjustment with the same kind of impurities that used in the bulk (p-type for NMOS and n-type for PMOS). If we were to use the same kind of doping in gate as in the body (i.e. n^+ for PMOS and p^+ for NMOS) that would lead to higher un-implanted threshold voltages. Adjusting them to the required lower threshold voltage would necessitate implantation of the impurities of the opposite type near the oxide-Si interface. This is not desirable. Also, the doping of the poly gate can be carried out at the same time as the source and drain and therefore does not require an extra step.

Problem 5

Solve for the dc value of the drain current, I_{DS}, for the NMOS transistor shown assuming 0.18μm CMOS technology. The W and L for this transistor are given in Problem 3.



Solution

Check for saturation.

$$V_{DS}(\text{sat}) = \frac{(V_{GS} - V_T)E_cL}{(V_{GS} - V_T) + E_cL} = \frac{(1\text{-}0.5)(1.2)}{(1\text{-}0.5) + 1.2} = 0.353\text{V}$$

$V_{DS} = 1.5\text{V} \Rightarrow$ NMOS in saturation

$$\therefore I_{DS} = Wv_{sat}C_{ox}\frac{(V_{GS} - V_T)^2}{(V_{GS} - V_T) + E_cL)}$$

$W = 0.6\text{x}10^{-4}$ cm

$$v_{sat} = \frac{\mu_e E_c}{2} = \frac{270\ (\text{cm}^2/\text{V}\cdot\text{s})\ 6\text{x}10^4(\text{V/cm})}{2} = 8.1\text{x}10^6\ \text{cm/sec}$$

$$C_{ox} = \frac{\varepsilon_r(\varepsilon_o)}{t_{ox}} = \frac{4\cdot 8.85\text{x}10^{-14}\ (\text{F/cm})}{35\text{x}10^{-8}\ \text{cm}} = 1.01\text{x}10^{-6}\ \text{F/cm}^2$$

$$\therefore \quad I_{DS} = (0.6\text{x}10^{-4}\text{cm})(\ 8.1\text{x}10^6\ \text{cm/sec})(\ 1.01\text{x}10^{-6}\ \text{F/cm}^2)\left(\frac{0.5^2}{0.5 + 1.2}\right)(\text{V})$$

$$= \underline{72.18\ \mu\text{A}}$$