

Homework Assignment No. 11

Due on Wednesday, April 13, 2005

1.) Problem P7.15 of the text

[Ans: a.) $V_x = V_{DD} - V_T$].

2.) Problem P8.4 of the text.

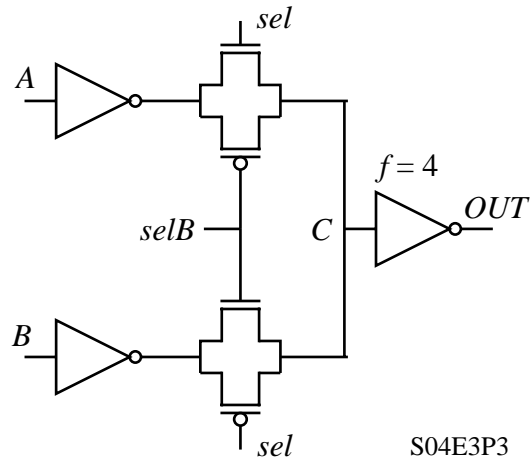
[Ans. $W_1 = W_2 = 0.4\mu\text{m}$ and $W_3 = W_4 = W_5 = W_6 = 0.75\mu\text{m}$ (I think, the answers are not obvious from the solutions)]

3.) Problem P.8.7 of the text.

4.) Problem P8.8 of the text.

[Ans: (a) $I_{SS} = 90\mu\text{A}$ (b) $W/L = 2$, (d) $W/L = 1.7$ and (d) $W/L = 0.8$]

5.) For the logic circuit shown below, assume that the transmission gates are all $4\lambda:2\lambda$ and that the inverters driving the transmission gates have PMOS transistors that are $8\lambda:2\lambda$, and NMOS transistors that are $4\lambda:2\lambda$, where $\lambda = 0.1\mu\text{m}$. The output inverter is to drive a 50 fF load. The output inverter is 4 times larger than the input inverters.



(a.) Write the logic expression for the output function in terms of A , B , sel , and $selB$.

(b.) Draw an equivalent RC circuit model for the path from A to C assuming that the sel signal is high. Write down the individual contributions for each resistance and capacitance and place the total values at the appropriate nodes.

(c.) Find the Elmore delay from A to C .