Homework No. 11 – Solutions

Problem 1 – P7.15

$$V_{OUT} = V_{OL}$$
$$V_X = V_{DD} - V_T$$

First, let's find the required change in voltage:

$$\Delta V_{OUT} = V_{DD} - V_{OL}$$
$$\Delta V_X = \left(V_{DD} + V_T\right) - \left(V_{DD} - V_T\right) = 2V_T$$

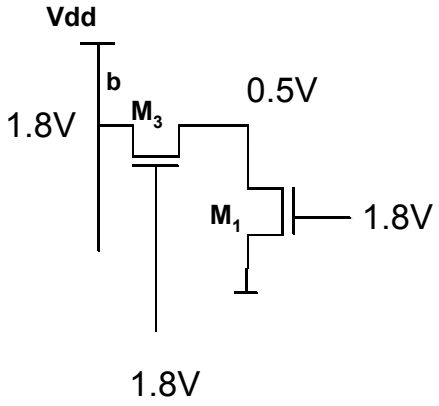
Now, let's set up the clock feedthrough equation and solve for C_b:

$$\Delta V_X = \frac{C_b \Delta V_{OUT}}{C_b + C_X}$$
$$C_b = \frac{\Delta V_X C_X}{\Delta V_{OUT} - \Delta V_X} = \frac{2V_T C_X}{V_{DD} - V_{OL} - 2V_T}$$

Problem 2 – P8.4

To compute the device sizes, start with the access transistor and the pull-down transistor:

We can compute the needed size of M_3 to deliver 300uA:



$$I_{cell} = \frac{W_L \nu_{sat} C_{ox} (V_{DD} - V_{OL} - V_{TL})^2}{(V_{DD} - V_{OL} - V_{TL}) + E_{CN} L_L} = \frac{W_L (8)(1.6)(1.8 - 0.5 - 0.5)^2}{(1.8 - 0.5 - 0.5) + 1.2} = 300\mu A$$
$$W_L \approx 0.75\mu m$$

Now determine the minimum W_D for the pull-down transistor:

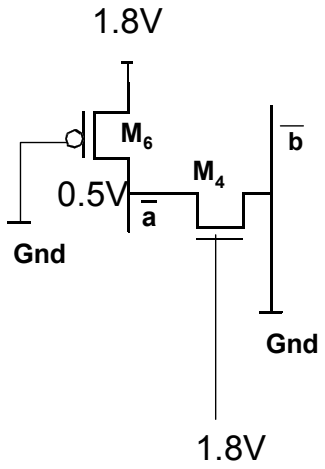
$$\therefore \frac{W_D}{L} \frac{\mu_N C_{ox}}{\left(1 + \frac{V_{OL}}{E_{CN} L}\right)} \left[\left(V_{DD} - V_T\right) V_{OL} - \frac{V_{OL}^2}{2}\right] = \frac{W_L \nu_{sat} C_{ox} (V_{DD} - V_{OL} - V_{TL})^2}{(V_{DD} - V_{OL} - V_{TL}) + E_{CN} L}$$

$$\frac{W_D}{L} \frac{(270)(1.6 \times 10^{-6})}{\left(1 + \frac{0.5}{1.2}\right)} \left[\left(1.8 - 0.5\right) 0.5 - \frac{0.5^2}{2}\right] = I_{cell}$$

$$\frac{W_D}{L} \approx 2 \qquad W_D = 0.4\mu m \qquad \text{(min)}$$

P8.4 - Continued

For the write operation, we must pull the internal node low against the PMOS pullup device. Try forcing the output to 0.5V which is below the expected V_S.



$$I_N = \frac{W_D}{L}\frac{\mu_N C_{ox}}{\left(1+\frac{V_{OL}}{E_{CN}L}\right)}\left[\left(V_{DD}-V_T\right)V_{OL}-\frac{{V_{OL}}^2}{2}\right] = (3.75)\frac{(270)(1.6\times10^{-6})}{\left(1+\frac{0.5}{1.2}\right)}\left[\left(1.8-0.5\right)0.5-\frac{0.5^2}{2}\right] = 600\mu A$$

$$I_P = \frac{W_P v_{sat} C_{ox}(V_{DD}-|V_{TP}|)^2}{(V_{DD}-|V_{TL}|)+E_{CP}L} = \frac{W_L(8)(1.6)(1.8-0.5)^2}{(1.8-0.5)+4.8} = 600\mu A$$

$$W_P \approx 1.7\mu m \quad \text{(max)}$$

Set W_p=0.75um.

Compute V_S to ensure that the output will be below this value:

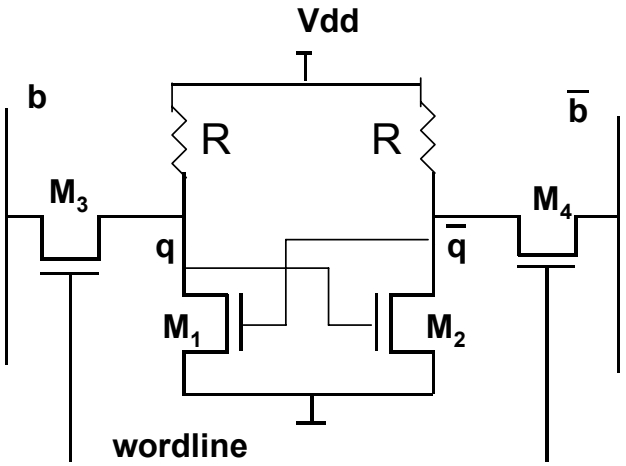
$$X = \sqrt{\frac{\frac{W_N}{E_{CN}L_N}}{\frac{W_P}{E_{CP}L_P}}} = \sqrt{\frac{W_N E_{CP}}{W_P E_{CN}}} = \sqrt{\frac{(24)}{(6)}} = 2$$

$$V_S = \frac{1.3+(0.5)2}{1+2} = 0.767V$$

Yes. This is still above the target V_{OL} so it should work just fine.

Problem 3 – P8.7

The following is a resistive load SRAM cell:



P3.1

The circuit is static in nature. Assume that q is low and qbar is high. During a read, M_3 and M_1 behave the same was as a 6T cell and act to discharge b. Meanwhile, M_4 turns on and hold the high value at qbar. To write a 1 into q, the bbar line is pulled low and M_4 pulls qbar low while M_3 pulls q high. Effectively, M_3 and M_4 acts as pull-ups for this type of SRAM cell.

Problem 4 – P8.8

(a)

$$I_{SS} = C\frac{dV}{dt} = 50\,fF\,\frac{0.9V}{500\,ps} = 90\,\mu A$$

(b) Assume long channel transistors:

$$I_{DS} = \frac{W}{L}\frac{\mu_N C_{ox}}{2}(V_{GS} - V_T)^2$$

$$45\,\mu A = \frac{W}{L}\frac{(270)(1.6uF/um^2)C_{ox}}{2}(0.1)^2$$

$$W/L = 21$$

(c) Use 8.13(c) as the column pullup circuitry. The initial voltage is V_{DD}-V_T.

(d) The voltage at the sources of the input transistors are both at V_{DD}-V_T-V_T-0.1=0.7V.

The maximum allowable gate voltage of M_5 is 0.7+V_T=1.2V. Choose 1.0V.

$$I_{DS} = \frac{W}{L}\frac{\mu_N C_{ox}}{2}(V_{GS} - V_T)^2$$

$$90\,\mu A = \frac{W}{L}\frac{(270)(1.6uF/um^2)C_{ox}}{2}(1.0 - 0.5)^2$$

$$W/L = 1.7$$

(e) Assume loads are in saturation and have V_{GS}-V_T=0.5V.

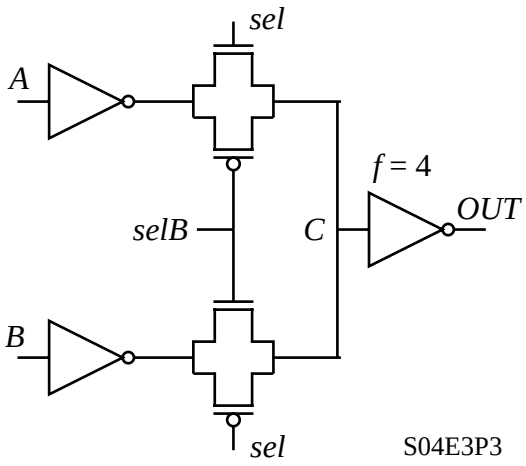
$$I_{DS} = \frac{W}{L}\frac{\mu_N C_{ox}}{2}(V_{GS} - V_T)^2$$

$$45\,\mu A = \frac{W}{L}\frac{(270)(1.6uF/um^2)C_{ox}}{2}(0.5)^2$$

$$W/L = 0.8$$

Problem 5

For the logic circuit shown below, assume that the transmission gates are all 4λ:2λ and that the inverters driving the transmission gates have PMOS transistors that are 8λ:2λ, and NMOS transistors that are 4λ:2λ, where λ = 0.1μm. The output inverter is to drive a 50 fF load. The output inverter is 4 times larger than the input inverters.



S04E3P3

(a.) Write the logic expression for the output function in terms of *A*, *B*, *sel*, and *selB*.

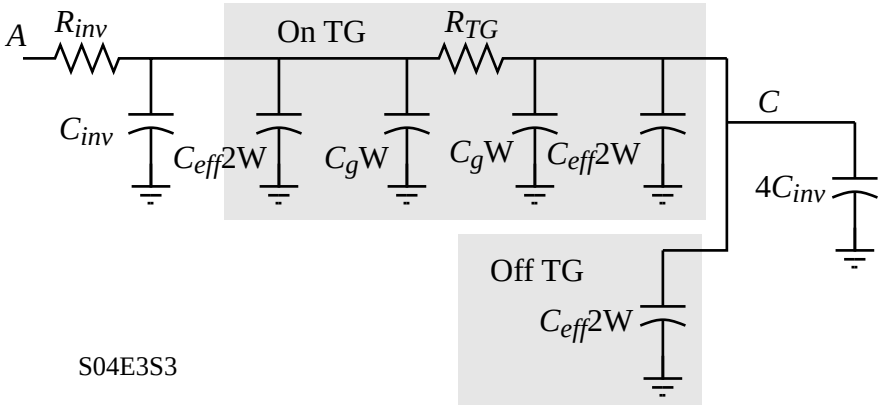
(b.) Draw an equivalent *RC* circuit model for the path from *A* to *C* assuming that the *sel* signal is high. Write down the individual contributions for each resistance and capacitance and place the total values at the appropriate nodes.

(c.) Find the Elmore delay from *A* to *C*.

Solution

(a.) $OUT = \overline{sel\cdot\overline{A} + \overline{sel}\cdot\overline{A}} = (\overline{sel} + A)\cdot(sel\cdot B) = A\cdot sel + B\cdot selB$

(b.) The equivalent *RC* circuit model is shown below.



S04E3S3

The quantities in this model are:

$R_{inv} = 12.5\text{k}\Omega\left(\frac{2\lambda}{4\lambda}\right) = 6.25\text{k}\Omega$, $C_{inv} = C_{eff}(W_n+W_p) = 1\text{fF/}\mu\text{m}(0.4\mu\text{m}+0.8\mu\text{m}) = 1.2\text{fF}$,

$C_{eff}(2W) = 1\text{fF/}\mu\text{m}(0.8\mu\text{m}) = 0.8\text{fF}$, $C_gW = 2\text{fF/}\mu\text{m}(0.4\mu\text{m}) = 0.8\text{fF}$

$R_{TG} = 12.5\text{k}\Omega\left(\frac{2\lambda}{4\lambda}\right) = 6.25\text{k}\Omega$, and $4C_{inv} = 4C_gW = 4(2\text{fF/}\mu\text{m})(1.2\mu\text{m}) = 9.6\text{fF}$

(c.) The Elmore delay from *A* to *C* is given as

$t_{AC} = 6.25\text{k}\Omega(1.2\text{fF}+0.8\text{fF}+0.8\text{fF}) + (6.25\text{k}\Omega+6.25\text{k}\Omega)(0.8\text{fF}+0.8\text{fF}+0.8\text{fF}+9.6\text{fF})$

$= 6.25\text{k}\Omega(2.8\text{fF}) + 6.25\text{k}\Omega(12\text{fF}) = 17.5\text{ps} + 150\text{ps} = \underline{167.5\text{ps}}$