Homework No. 13 – Solutions

Problem 1 – P10.11

The following numbers are used in this problem:

0.18 um numbers
Rsq = 27 mΩ/sq
Wwire = 0.4 um
Rint = 67.5 mΩ/um
Cint = 0.2 fF/um

0.13 um numbers

Rsq = 21 mΩ/sq
Wwire = 0.2 um
Rint = 105 mΩ/um
Cint = 0.2 fF/um

The number of repeaters required in 0.18 um technology:
$N = \text{sqrt}[(RintCintL^2/2)/(Reqn(C_J + C_G)(1 + B))] = 5.47 \approx \mathbf{5}$

The number of repeaters required in 0.13 um technology:

$N = \text{sqrt}[(RintCintL^2/2)/(Reqn(C_J + C_G)(1 + B))] = 9.67 \approx \mathbf{10}$

Therefore, for long wires we need approximately double the number of buffers in 0.13 um technology as we do in 0.18 um technology.

Problem 2 – P11.2a

a) Assuming that the 16 switching inverters are all located at the end of the power bus, which is the worst-case scenario, the worst-case voltage drop at the far end of the power bus can be found.

The power bus has a total resistance of:

Rwire = Rsq(L/W) = 54 mΩ/sq (400/0.4) = 54 Ω

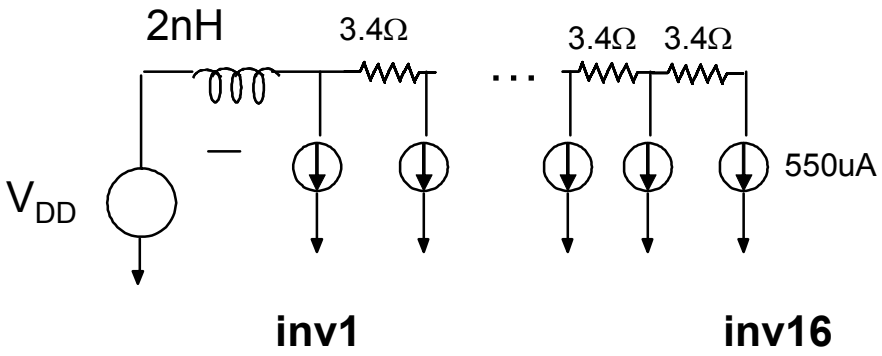
The resistance between switching inverters is = 54 Ω/16=3.4 Ω

Assuming that the inverters are of minimum length (0.2 um), and have an NMOS width of 1 um, the current through each inverter is:

Ion = 550uA/um x 1um = 550uA.

Since there are 16 of these switching inverts in parallel, we can assume that the following circuit exists.

Problem 2 - Continued



Therefore, the total current drawn from the power supply is:

I = 16 x 550uA = 8.8mA

Assuming simultaneous switching, the voltage drop due to the inductor is:

Vdrop1 = Ldi/dt = 2 nH (8.8 mA / 100 ps) = **0.176 V**

The voltage drop at the far end due to the IR drop is based on different levels of voltage drop across each resistor due to the current source arrangement shown above. The voltage drop at the far end is:

Vdrop2 = I (1 +2 + 3 + 4 + … + 16) 3.4Ω = 550uA x (16)(17)/2 x 3.4Ω = **0.254 V**

The total drop is Vdrop = Vdrop1 + Vdrop2 = **0.430 V**

This voltage drop is too large to ensure reliable operation of the circuit, therefore something must be done to reduce this problem (which is the subject of parts b and c).

Problem 3 – P11.10

A 10mm m5 wire in 0.18um technology has parasitic as follows
(Data from Assignment 2)

- C_{wire} = 10,000um x 0.1fF/μm = 1pF
- C_{int} = 0.1fF/μm
- R_{wire} = (10,000um/0.4μm) x 27mΩ = 675Ω
- R_{int} = 67.5mΩ/□
- C_G = C_gW = 2fF/μm x 2 x 0.2μm = 0.4fF
- C_j = C_{eff}W = 1fF/μm x 0.2μm = 0.2fF

The circuit setup will constitute a chain of inverters driving a long wire with buffers inserted to reduce delay.

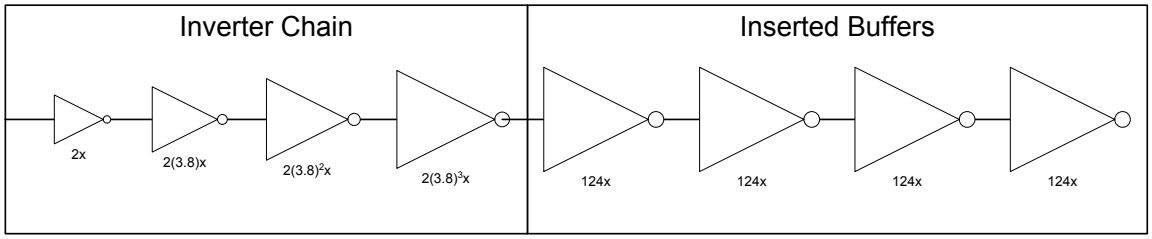


Figure 11.10(a)

Problem 3 - Continued

Analysis will proceed in two steps:

- Buffer Insertion Design
- Chain of Inverters Design (Logical Effort)

Buffer Insertion Design

First the inserted buffers will be designed to optimize delay.
Number of stages is given by the equation:

$$N = \sqrt{\frac{R_{\text{int}} C_{\text{int}} L^2 / 2}{R_{eqn}(C_G + C_J)3}}$$

$$= \sqrt{\frac{67.5 \times 0.1 \times 10000^2 / 2}{12.5e3 \times (0.4 + 0.2)3}}$$

$$= 3.87 \rightarrow 4 segments$$

So the wire is divided into 4 segments for buffer insertion.

Size of the buffers to insert:

$$M = \sqrt{\frac{R_{eqn} C_{\text{int}}}{C_G(1+\beta)R_{\text{int}}}}$$

$$= \sqrt{\frac{12.5e3 \times 0.1}{0.4 \times (1+2) \times 67.5e-3}}$$

$$= 124.2$$

As calculated, the buffers being inserted into the line will be 124 times the minimum buffer size. In order to drive such a large buffer, a chain of inverters will be required.

Therefore, use FO4 inverters as follows: 2x -> 8x -> 32x -> 124x.
The delay for the first three stages is 3 x 75ps = **225ps**.

Buffer & Wire Delay

Buffer insertion results in 4 wire segments driven by large buffers. The model is shown in figure below:

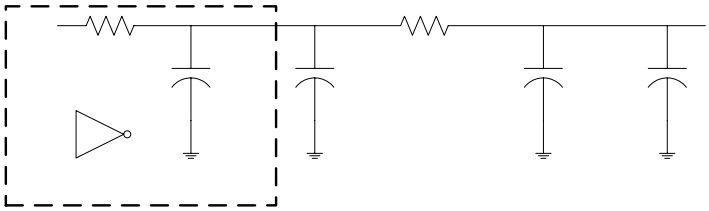


Figure 11.10(d)

Using Elmore $t_{segment}$ can be calculated.

$$t_{segment} = \frac{R_{eqn}}{M}\left(C_j M(1+\text{B}) + \frac{C_{\text{int}} L}{2N}\right) + \left(\frac{R_{eqn}}{M} + \frac{R_{\text{int}} L}{M}\right)\left(C_G M(1+\text{B}) + \frac{C_{\text{int}} L}{2N}\right)$$

$$= \frac{12.5k}{124}\left(0.2f(3) + \frac{0.1f(10000)}{2(4)}\right) + \left(\frac{12.5k}{124} + \frac{67.5m(10000)}{4}\right)\left(0.4f(124)(3) + \frac{0.1f(10000)}{2(4)}\right)$$

$$= 93.8 ps$$

Problem 3 - Continued

The results of the Elmore calculation indicate that

$$t_{segment} = 93.8ps$$

Since there are 4 segments, the total delay through all the wire segments is

$$t_{totalwiresegments} = 4 \times 93.8ps = \mathbf{375.2ps}$$

Total Delay through the circuit is:

$$t_{chain\ delay} + t_{totalwiresegments} = 225ps + 375ps = \mathbf{600ps}$$

As shown in Figure 11.10(e), spice measurements indicate a delay of 572ps,.

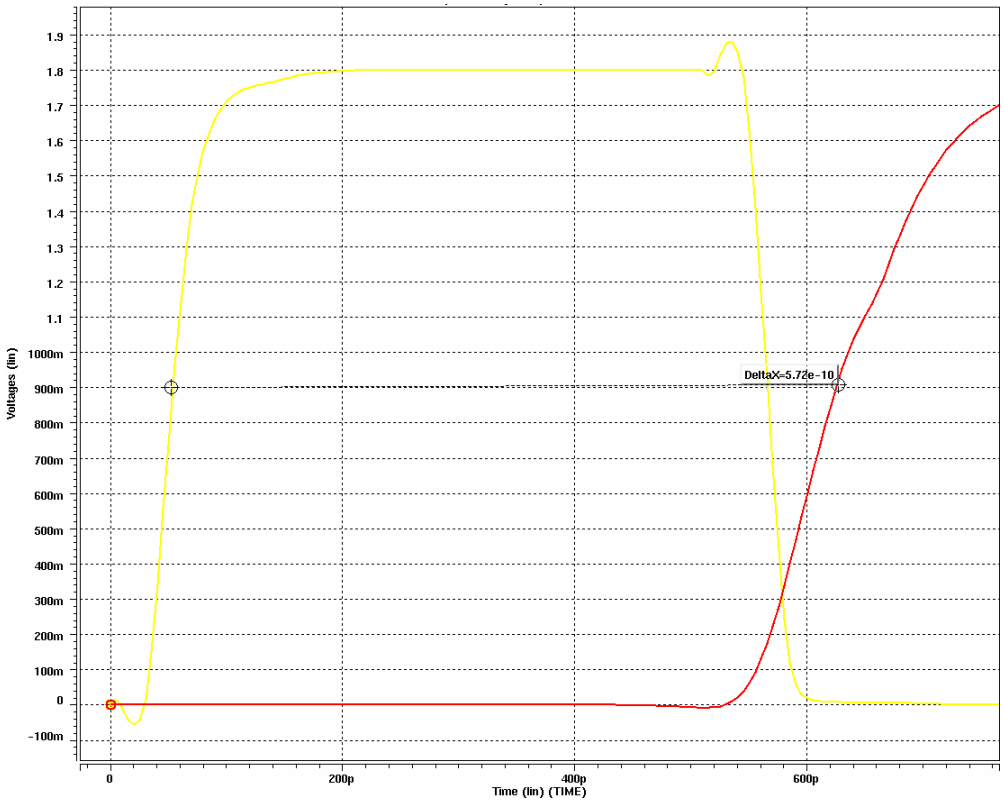


Figure 11.10(e) – Entire circuit input to output delay

This is a difference of 5%. This exercise demonstrates that hand calculations for are quite accurate in comparison to spice.