# DIGITAL INTEGRATED CIRCUITS

## INTRODUCTION

### (1.) Course

Objective - Design of digital ICs in DSM technologies

Goals -

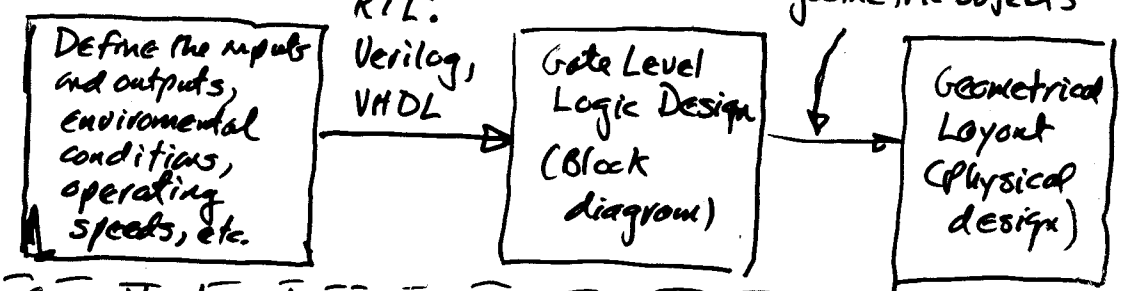
- Devel the models & intuition to do digital IC design in DSM technology
- Examine actual circuits designed in industry and learn about tradeoffs
- Be able to work with future advances in technology

$$f_T \propto \frac{1}{(\text{Channel length})^2}$$

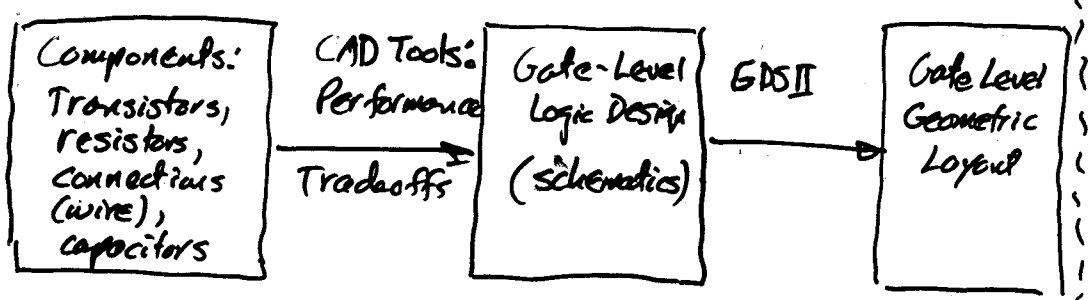
- Provide the basis and foundation for more courses on the topic of logic design.

### (2.) Design

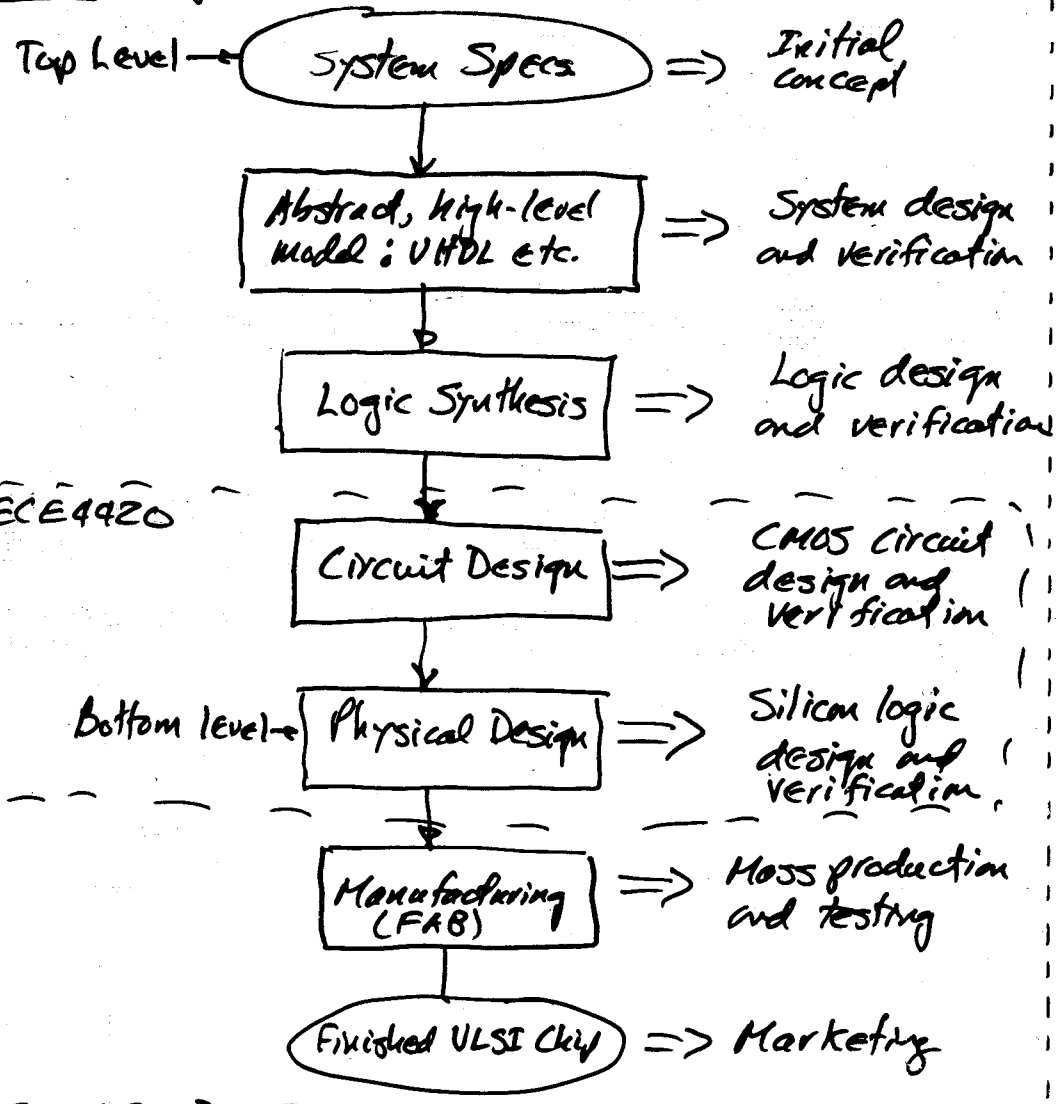
Systems level -




Circuits Level - ECE 4420



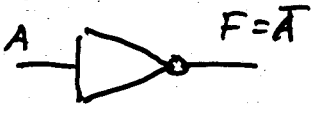
## Design Flow (Digital Logic)




## REVIEW OF DIGITAL GATE LOGIC

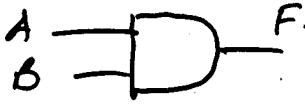
Basic Logic Functions-

1.) Inverter (NOT)



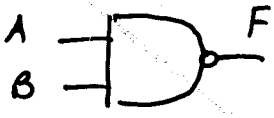

| A | F |
|---|---|
| 0 | 1 |
| 1 | 0 |

2.) AND ("·")



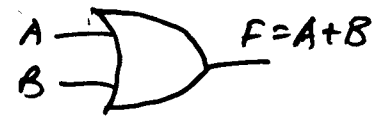

| A | B | F |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

3.) NAND



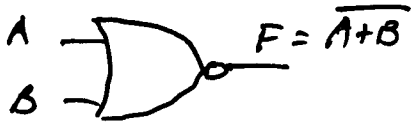

| A | B | F |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

4.) OR ("+")




| A | B | F |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 1 |

5.) NOR




| A | B | F |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 0 |

6.) XOR


$F = A \oplus B$

$= A\bar{B} + \bar{A}B$

| A | B | F |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

7.) XNOR . . . .

## De Morgan's Laws

$\overline{(A+B)} = \bar{A} \cdot \bar{B}$

$\overline{(A \cdot B)} = \bar{A} + \bar{B}$

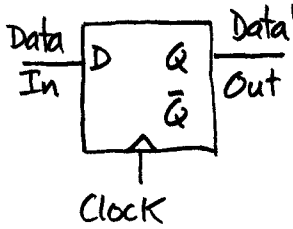
## Sequential Logic Circuits

A digital ckt. whose output is determined by both the present input and the results of a previous event

Flip-flops (FF):

D-FF, JK-FF, T-FF, SR-FF, etc.

DFF:




Positive-edge triggered DFFs

| CLK | D | Q(old) | Q(new |
|---|---|---|---|
| 0 | X | 0 | 0 |
| 0 | X | 1 | 1 |
| 0→1 | 0 | X | 0 |
| 0→1 | 1 | X | 1 |
| ⊓ | X | 0 | 0 |
| ⊓ | X | 1 | 1 |
| 1→0 | X | 0 | 0 |
| 1→0 | X | 1 | 1 |