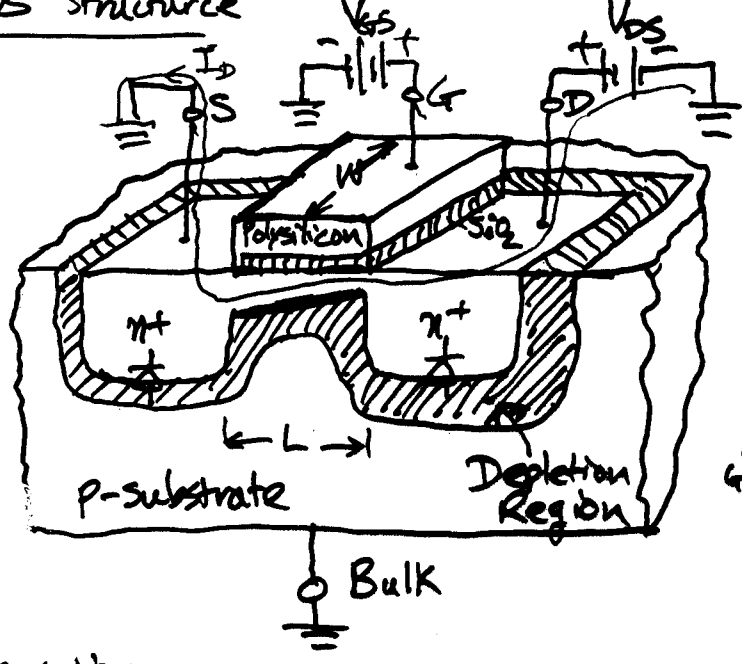
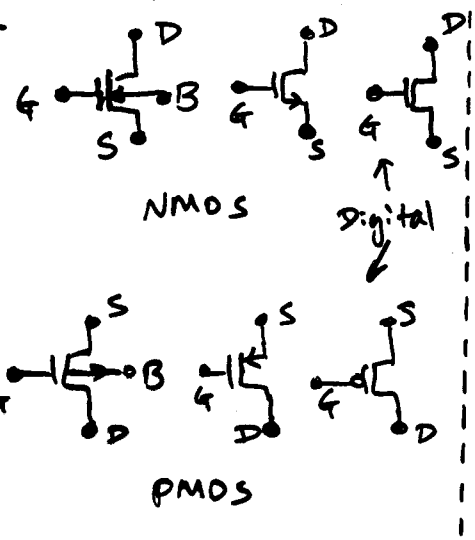
MOSFET TRANSISTOR

NMOS structure



Symbol:



Operation:

	form channel via y-$\mathcal{E}$-field	Drift via x-$\mathcal{E}$ field
NMOS	$V_{GS} > V_T$	$V_{DS} > 0$
PMOS	$V_{GS} < V_T$	$V_{DS} < 0$

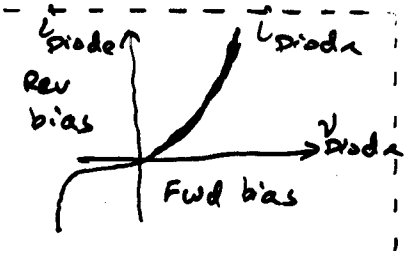
Comments:

1) N in NMOS means negative ⇒ e^- major carrier
   P in PMOS means positive ⇒ h^+ major carrier
   NMOS + PMOS = CMOS "complimentary"

2) As IC Designer, you can only play with horizontal Dimentions such as (W) and L. All vertical dimensions are fixed for given technology.

3) Y-$\mathcal{E}$-field will induce leakage current, a very very bad behavior as we shrink transistors. (t_{SiO_2} ↓)
   Also ↓ L resulting high x-$\mathcal{E}$ field (horizontal) ⇒ drift velocity will saturate ⇒ reduced current drivability

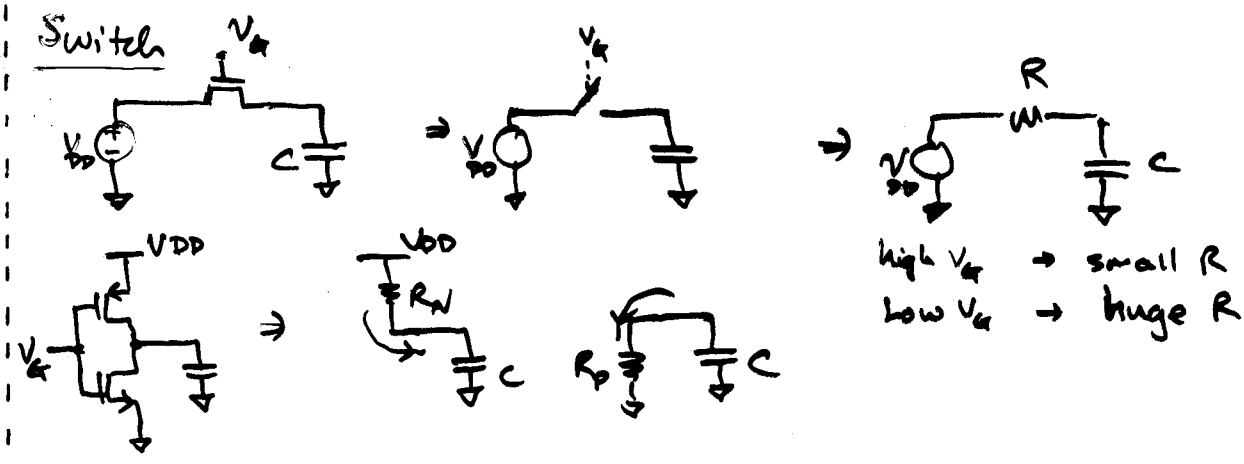
4) depletion region due to the PN junction isolates the transistor from others in the same substrate



⇒ { NMOS → tie P-substrate to ground
PMOS → tie n-well to VDD (Power supply)

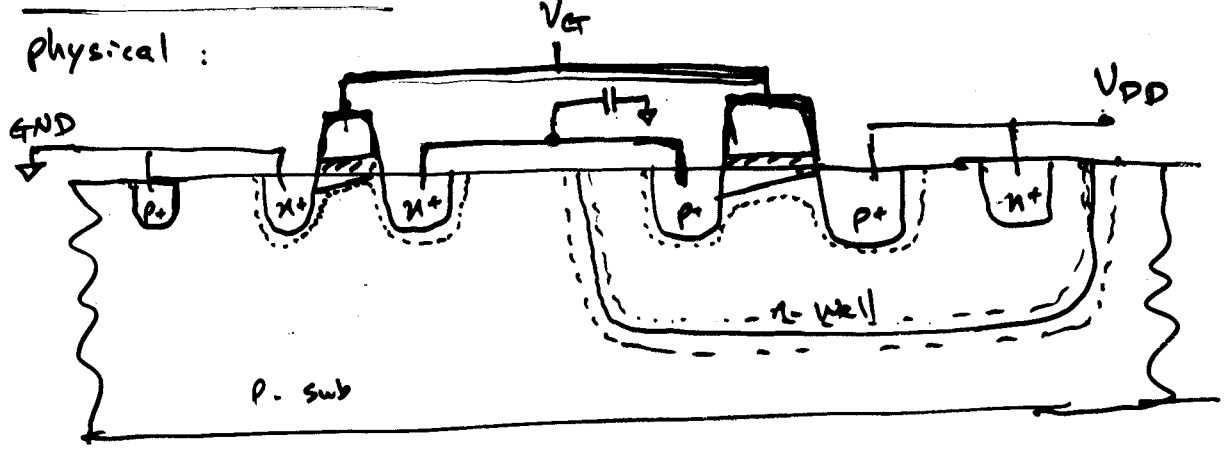
5) MOS transistor are symmetrical i.e. **D and S are interchangable**
You define the lower voltage node as Source node as it provide/source e^- which is collected/drained by Drain node. Similar argument holds for PMOS.

Switch

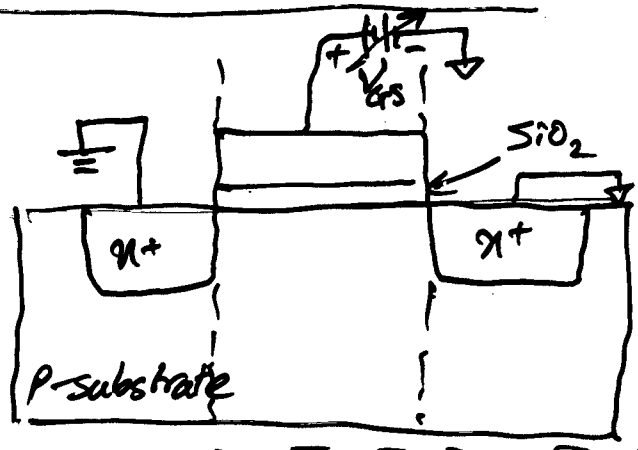


CMOS transistors

physical :



Threshold voltage of the MOS transistor



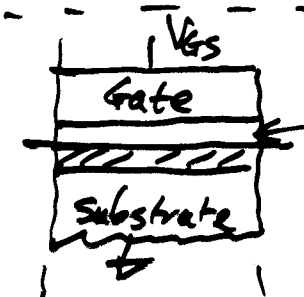
What happens as V_{GS} increases from zero?

$V_{GS}<0$

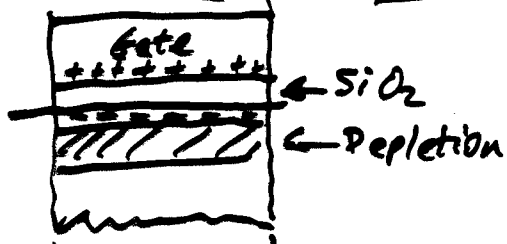
Accumulation

0V

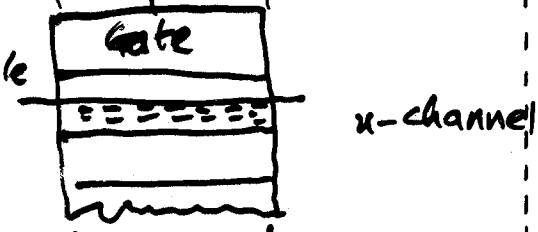
1.) A depletion region forms under the gate. There are no holes, only negatively charged atoms



2.) A thin layer of mobile electrons appear at the surface of the silicon (Weak inversion)

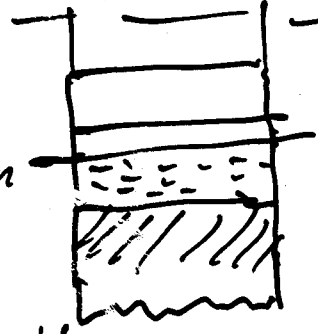


3.) Finally, the mobile electron concentration equals the mobile hole concentration in the semiconductor (substrate) $V_{GS}=V_T$ (strong inversion)



4.) Further increases simply increase the channel depth and the electron concentration is much greater than the hole concentration

V_{GS} increase



NEXT – Components that make up the V_T