Exam #1 – Friday, Feb. 11 – Closed book (Study Guide for Exam 1)
Problem Session?

Temperature Effects of the MOSFET

$$i_{DS} = \frac{KP}{2} \cdot \frac{W}{L} (v_{GS} - V_T)^2$$

1.) Mobility (KP):

$$KP(T) = KP\left(\frac{T}{T_0}\right)^{-1.5}$$

$$\mu(T) = \mu_0 \left(\frac{T}{T_0}\right)^{-1.5}, \quad \mu_0 = \mu(T_0)$$

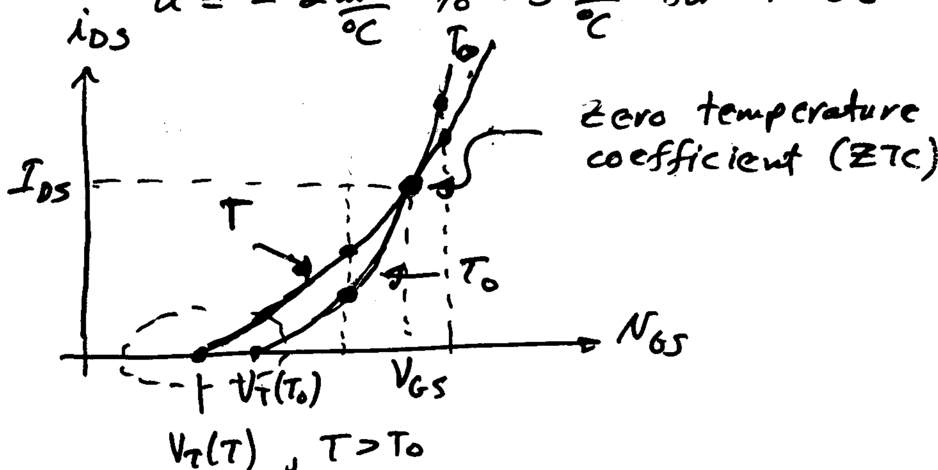
(T_0 ← 300°K)

2.) Threshold voltage:

$$V_T(T) = V_T(T_0) + \alpha(T - T_0) + \beta(T-T_0)^2 + \cdots$$

$$V_T(T) \approx V_T(T_0) + \alpha(T - T_0)$$

$$\alpha = -2\frac{mV}{°C} \text{ to } -3\frac{mV}{°C} \text{ for NMOS}$$



3.) Subthreshold

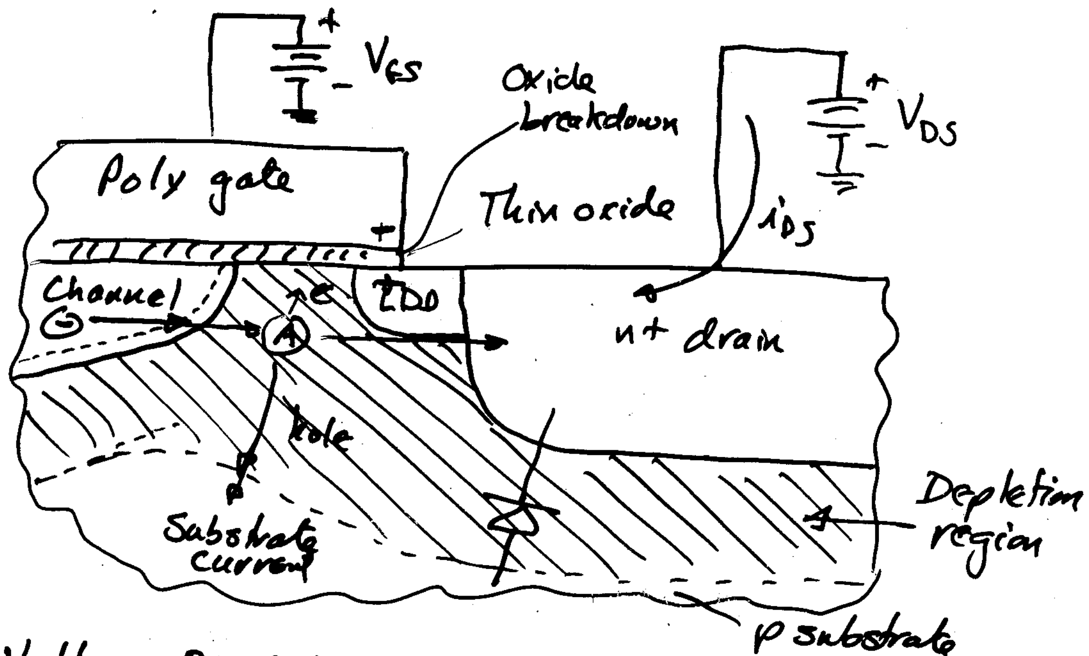
Since the current is now controlled by minority carrier concentration, it is strongly dependent on n_i.

$$\therefore n_i(T) = 1.45\times10^{16}\left(\frac{T}{300°K}\right)^{1.5} \exp\left[\frac{1.12}{0.0516} - \frac{E_g(T)}{2V_t}\right]$$

$$i_{DS}(T) \propto T$$

Voltage Limitations

1.) Hot carrier effect (HCE) - LDD reduces the electric field which in turn reduces the HCE.

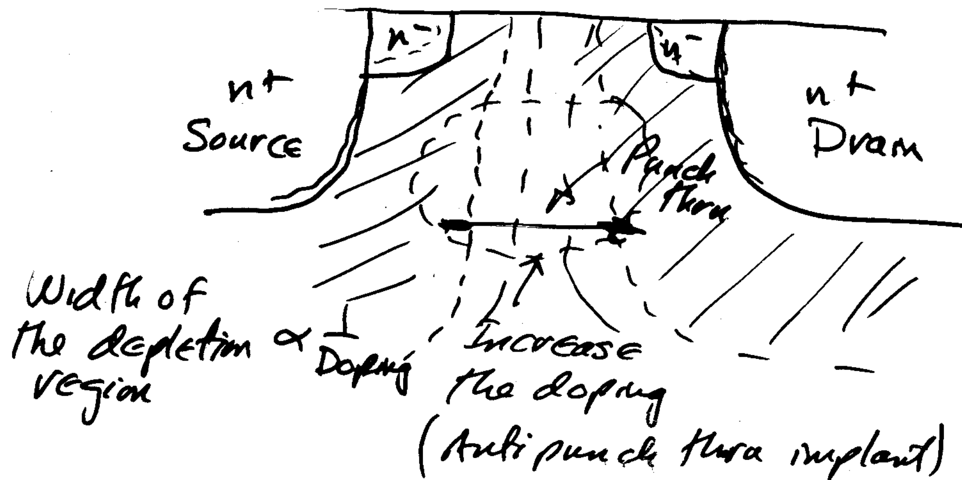


2.) Voltage Breakdown

a.) PN junction ($BV \propto \frac{1}{Doping}$)

b.) Oxide breakdown → $V_{DD}(max) \cong 10 \times L_{min}$

c.) Punch thru

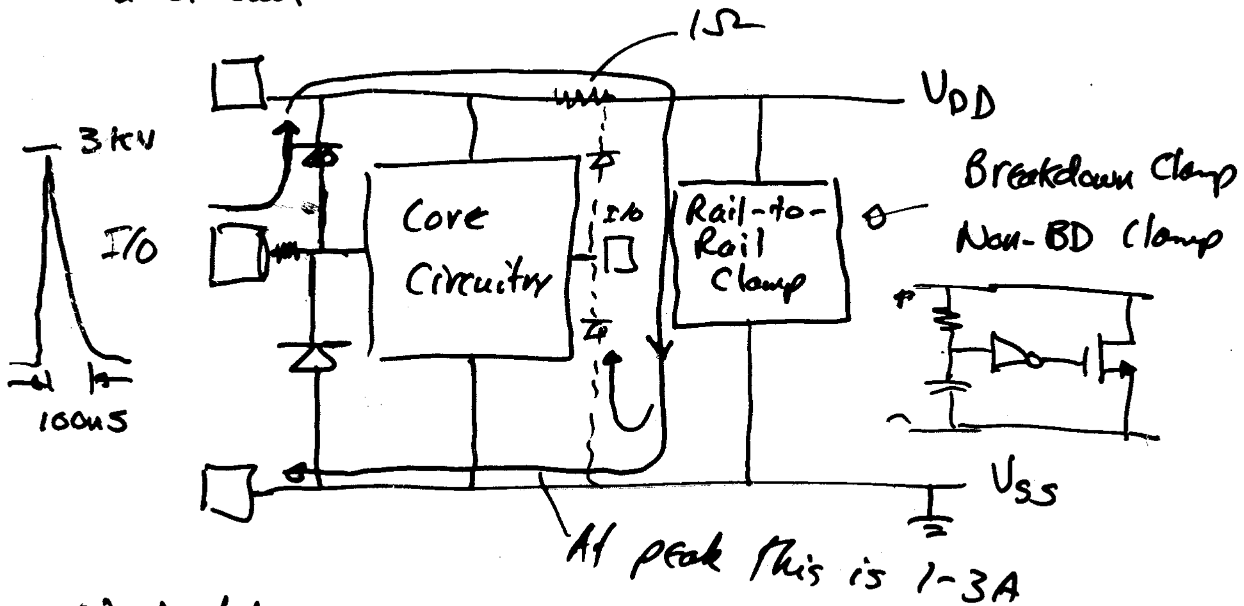


3.) Electrical Overstress (EOS)

a.) Electrostatic discharge
b.) Metal migration
c.) Antenna ~~diode~~ effect

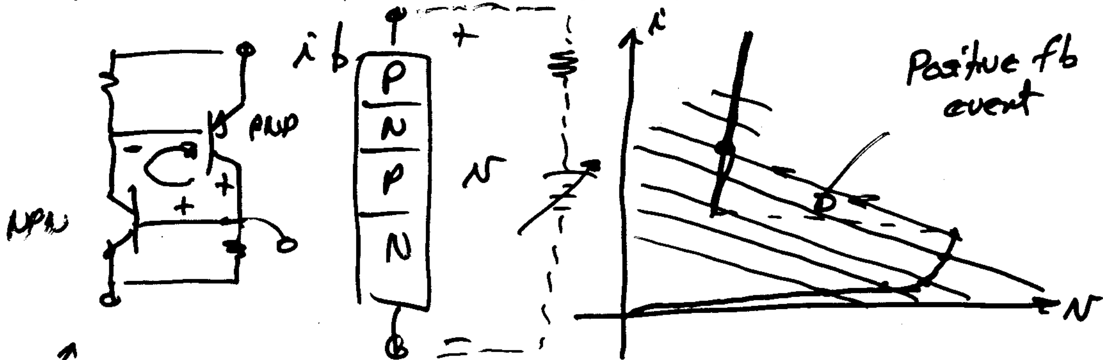
ESD –

Large static voltages applied momentarily to a circuit.



4.) Latchup

Silicon Controlled Rectifier (SCR)



Latchup occurs when the loopgain > 1