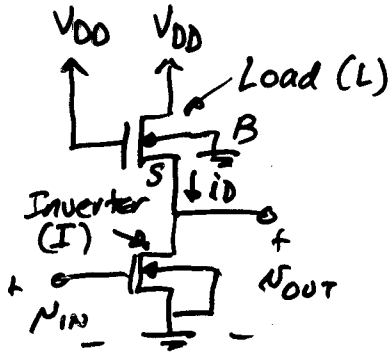
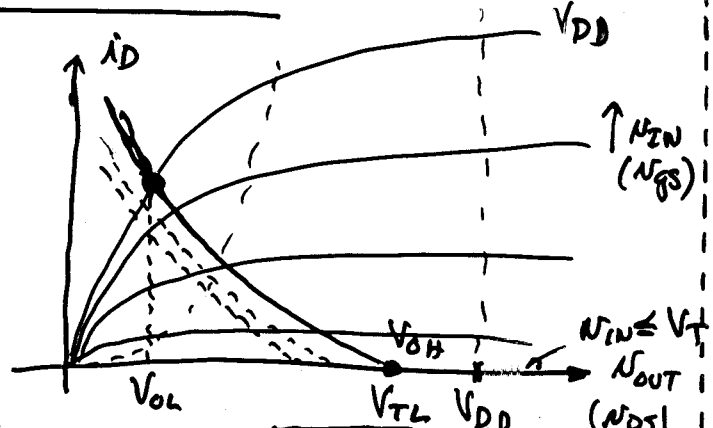
4.2 V_{OL} = ? ii. $V_{OUT} = V_{SB} = V_{OH} = V_{TO} + \gamma\sqrt{V_{OH} + |2\phi_f|} - \gamma\sqrt{|2\phi_f|}$

ACTIVE LOAD INVERTERS

Saturated Enhancement Load Inverter

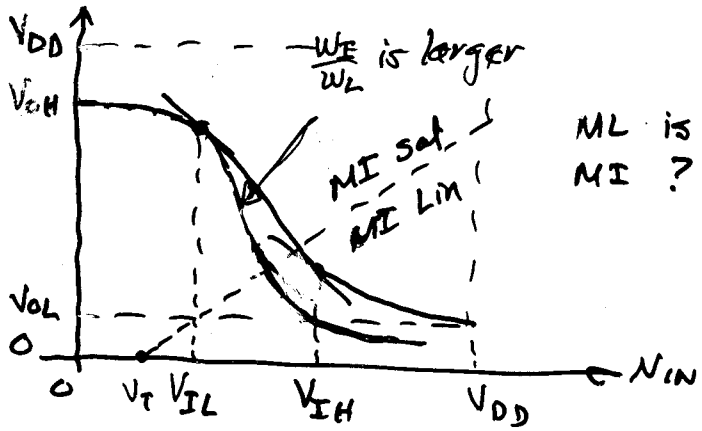




Voltage Transfer Curve –

$V_{TL} = V_{TO} + \gamma\sqrt{V_{SB} + 2\phi_F} - \gamma\sqrt{2\phi_F}$

V_{OUT}



ML is always saturated (cutoff)

MI ?

$V_{DS} > V_{DS}(sat) = V_{GS} - V_T$

$V_{DS} = V_{GS} - V_T$

$V_{OUT} = V_{IN} - V_T$

To find V_{IL}: Assume MI sat & ML sat. V_{out} is small

V_{OH}, V_{OL} and V_{IH} and V_{IL} are challenging

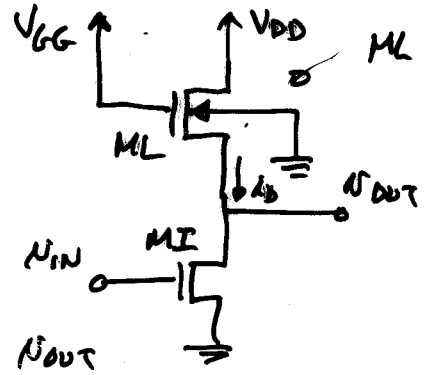
General approach:

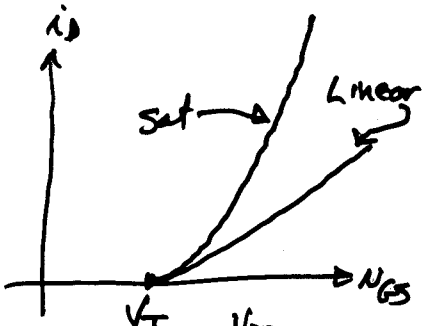
1.) Identify states of the MOSFETs

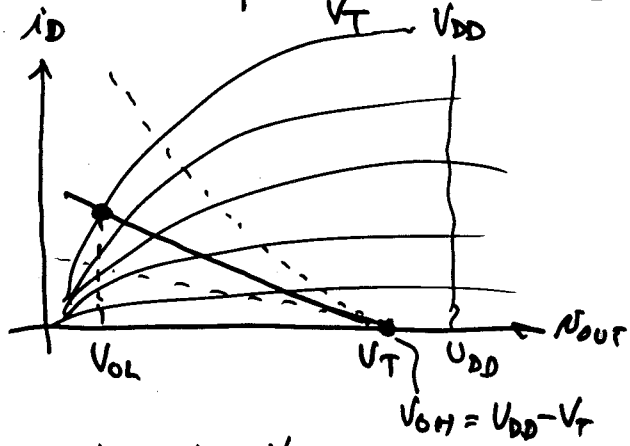
2.) Equate currents

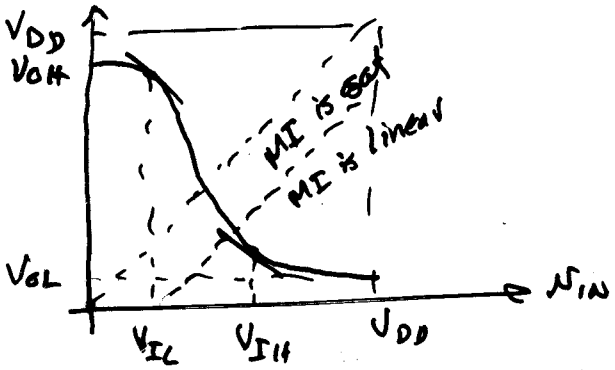
3.) Solve for V_{OH} (V_{OL})

Linear, Enhancement, Load Inverter









$V_{OH} = V_{DD} - V_{T2}$

More gain compared to Sat., enh. load inverter

Disadvantages -

1.) $V_{GG} \geq V_{DD}$

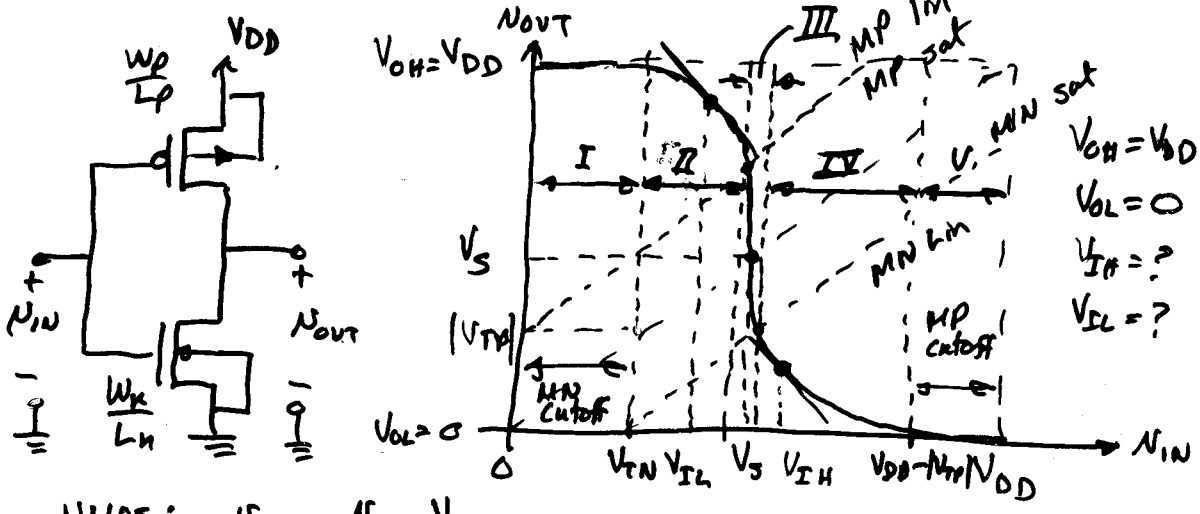
2.) Chip area is required for V_{GG}

3.) $K_R = \frac{(W/L)_I}{(W/L)_L}$ $\quad K_R(lin) > K_R(sat)$

4.) DC power dissipation

CMOS INVERTER

DC Analysis of the CMOS inverter



NMOS: $V_{OUT} = V_{GS} - V_{TN}$

PMOS: $V_{SD} = V_{SG} - |V_{TP}| \rightarrow V_{DD} - V_{OUT} = V_{DD} - V_{GN} - |V_{TP}|$

$V_{OUT} = V_{IN} + |V_{TP}|$

Region	NMOS	PMOS
I	Cutoff	Linear
II	Sat	Linear
III	Sat.	Sat
IV	Linear	Sat
V	Linear	Cutoff

Finding V_S (Region III)

$i_N(sat) = i_p(sat) \rightarrow$ $\dfrac{W_n v_{sat} C_{ox}(V_{IN}-V_{TN})^2}{(V_{IN}-V_{TN})+E_{CN}L_N} = \dfrac{W_p v_{sat} C_{ox}(V_{DD}-V_{IN}-|V_{TP}|)^2}{(V_{DD}-V_{IN}-|V_{TP}|)+E_{CP}L_P}$

Set $V_{IN} = V_S$ and solve ($V_{DD}/2$, $V_{DS}/2$)

Assuming $V_S \approx \frac{V_{DD}}{2}$, then: ($V_{IN} = V_S$) $V_{IN} - V_{TN} < E_{CN}L_N$

$$\frac{W_N (V_S - V_{TN})^2}{E_{CN}L_N} \simeq \frac{W_p (V_{DD} - V_S - |V_{TP}|)^2}{E_{CP}L_P} \qquad L_p = L_n$$

$$\boxed{V_S = \frac{V_{DD} - |V_{TP}| + \chi V_{TN}}{1+\chi}} \qquad \chi = \sqrt{\frac{E_{CP} W_N}{E_{CN} W_P}} = \sqrt{\frac{\mu_n W_N}{\mu_P W_P}}$$