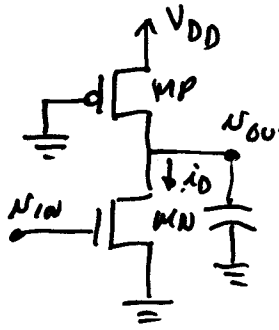
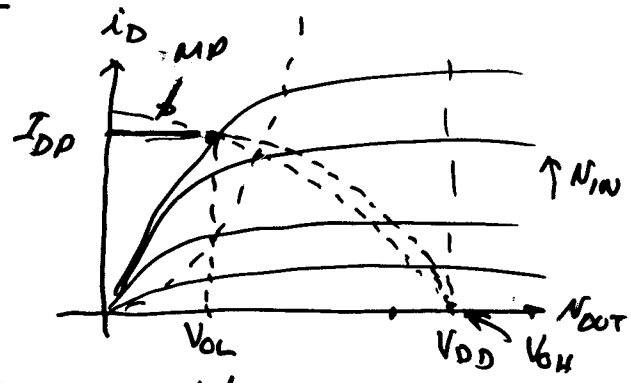
Pseudo-NMOS Inverters



$V_{OH} = V_{DD}$

$V_{OL} = ?$



$V_{OL} = ?$ $\quad I_D(sat) = I_N(Lin) = $ Fixed value

$$I_{DD}(sat) = \frac{W_N}{L_N}\frac{\mu_n C_{ox}}{\left(1+\frac{V_{OL}}{E_{CN}L_N}\right)}\left[(V_{DD}-V_{TN})(V_{OL}) - \frac{V_{OL}^2}{2}\right]$$

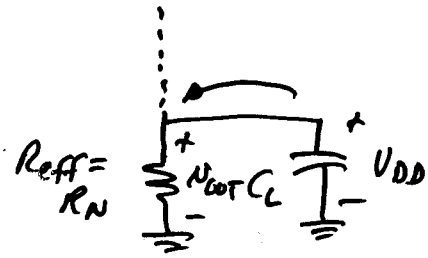
Assume $V_{OL} < 1$

$$I_{DD}(sat) \approx \frac{W_N}{L_N}\left(\frac{\mu_n C_{ox}}{1}\right)(V_{DD}-V_{TN})V_{OL} = k_N(V_{DD}-V_{TN})V_{OL}$$

$$V_{OL} \approx \frac{I_{DD}(sat)}{k_N(V_{DD}-V_{TN})} \qquad k_N = \mu_n C_{ox}\frac{W_N}{L_N}$$

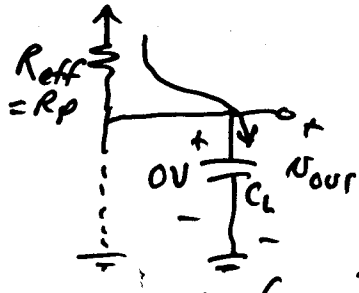
Sizing Inverters

Pull down:

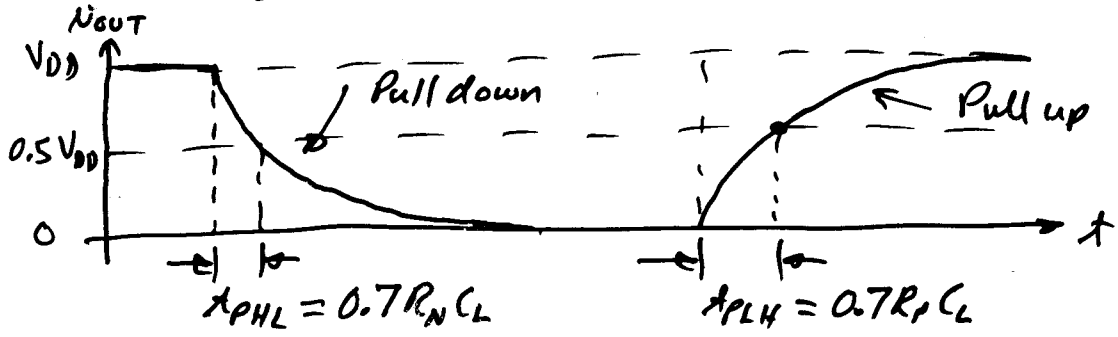


$$v_{OUT} = V_{DD}e^{-t/R_N C_L}$$

Pull up:



$$v_{OUT} = V_{DD}\left(1 - e^{-t/R_p C_L}\right)$$



$t_{PHL} = 0.7R_N C_L$ $\qquad$ $t_{PLH} = 0.7R_p C_L$

Example 4.9 – Sizing CMOS and Pseudo-NMOS Inverters

Size the CMOS & pseudo-NMOS inverters using 0.13 μm technology if $C_L = 50fF$. (see text for process data)

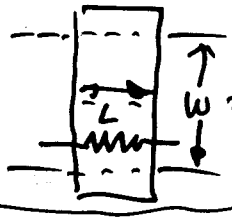
For the CMOS inverter: $t_{PHL} = t_{PLH} \le 50ps$, $V_{OH} = 1.2V$, $V_{OL} = 0V$

For the pseudo-NMOS inverter: $t_{PHL} \le 50ps$, $V_{OH} = 1.2V$, $V_{OL} = 0.1V$

1.) CMOS (speed is highest priority)

$$t = 0.7 R_{eff} C_L = 50ps \rightarrow R_{eff} = 1.4k\Omega$$

From simulation of the CMOS technology we find that eq. on resistance for a NMOS $\simeq 12.5k\Omega/\square$ and for PMOS $\simeq 30k\Omega/\square = R_{eqp}$. R_{eqn}



$$R_N = 12.5k\Omega \frac{L}{W}$$
$$R_P = 30k\Omega \frac{L}{W}$$

$$R_N = R_{eqn}\left(\frac{L_N}{W_N}\right) = 12.5k\Omega\left(\frac{L_N}{W_N}\right) = 1.4k\Omega \Rightarrow \frac{W_N}{L_N} = 8.75$$

and

$$R_P = R_{eqp}\left(\frac{L_P}{W_P}\right) = 30k\Omega\left(\frac{L_P}{W_P}\right) = 1.4k\Omega \Rightarrow \frac{W_P}{L_P} = 21$$

2.) Pseudo-NMOS ($V_{OL} = 0.1V$ is the priority)

$$\frac{W_P \nu_{sat} C_{ox}(V_{DD} - |V_{TP}|)^2}{(V_{DD} - |V_{TP}|) + E_{CP}L_P} = \frac{W_N}{L_N}\left(\frac{\mu_n C_{ox}}{1 + \frac{V_{OL}}{E_{CN}L_N}}\right)\left[(V_{DD} - V_{TN})V_{OL} - \frac{V_{OL}^2}{2}\right]$$

Let the NMOS $\frac{W_N}{L_N}$ be 8.75: only unknown is W_P

$$2.56 W_P = 176 \times 10^{-4} \rightarrow W_P = 0.66\mu m$$

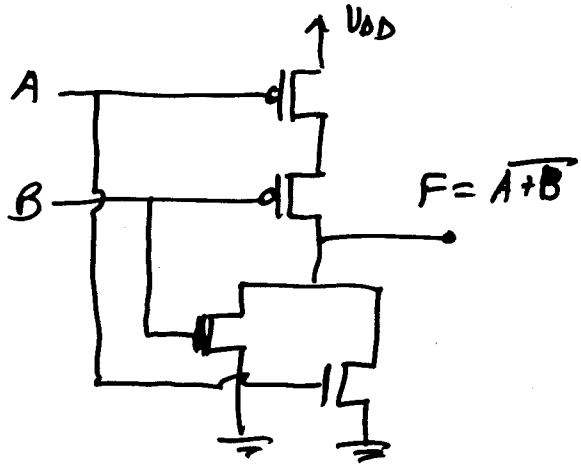
t_{PLH}: $R_{eqp} \times \frac{0.1}{0.66} = 4.54k\Omega \rightarrow t_{PLH} = (4.54K)(50fF)(0.7)$

$= 227ps$ (150ps)

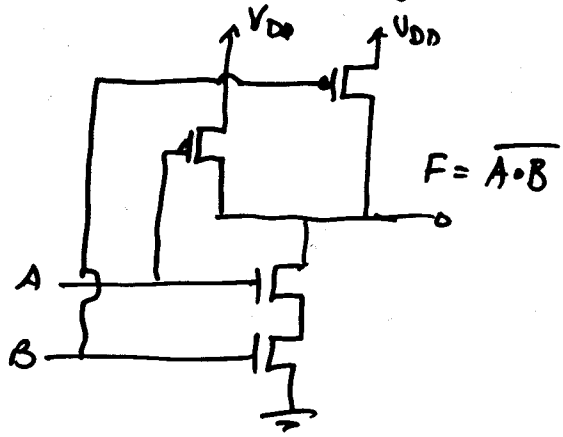
?

CHAP 5 - CMOS GATE CIRCUITS

2-input NOR gate:

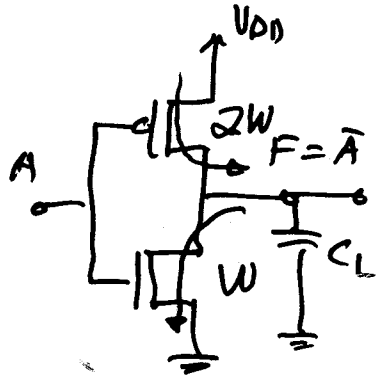


2-input NAND gate:



Basic Gate Sizing

All sizing will be based on the device sizes shown in the CMOS inverter



$L_p = L_n = L$

$\mu_n \approx 2\mu_p$

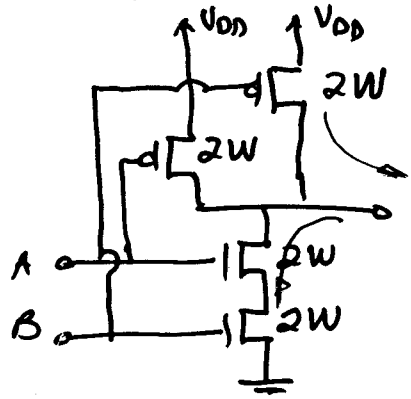
Worst Case Gate Sizing

(Do from a speed viewpoint)

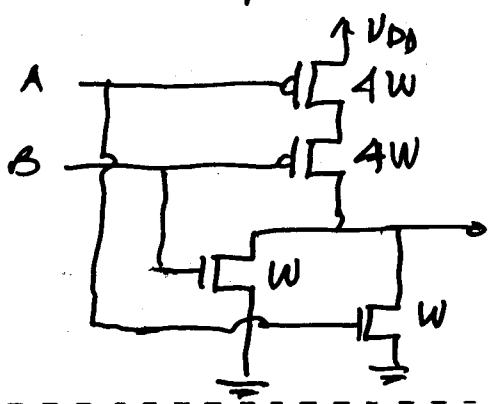
Assume that when V_{GS} or $|V_{SG}| = V_{DD}$, $R_{MOS} \approx 0$

and when V_{GS} or $|V_{SG}| = 0$, $R_{MOS} \approx \infty$

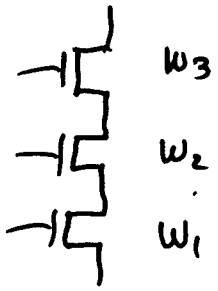
2 input NAND:



2 input NOR:



Effective Resistance for Series transistors-



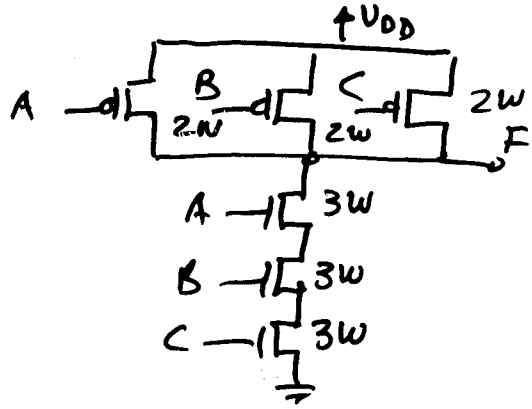
$$R_{MOS} \propto \frac{1}{W} = \frac{K}{W}$$

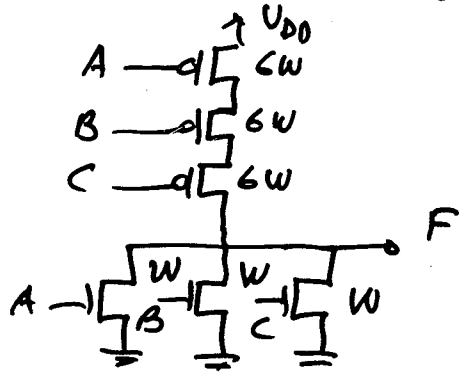
$$\therefore R_{eff} = R_1 + R_2 + R_3 = \frac{K}{W_1} + \frac{K}{W_2} + \frac{K}{W_3} = \frac{K}{W_{eff}}$$

$$W_{eff} = \frac{1}{\frac{1}{W_1} + \frac{1}{W_2} + \frac{1}{W_3}}$$

Example 5.1

Determine the device sizes for a 3-input NAND & NOR gate



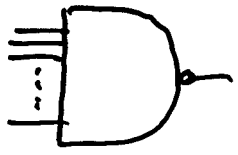


Fan-in and Fan-Out

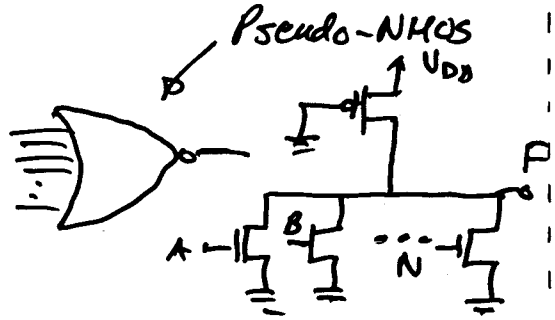
Too many inputs cause too much area.

Fan in:

1.)

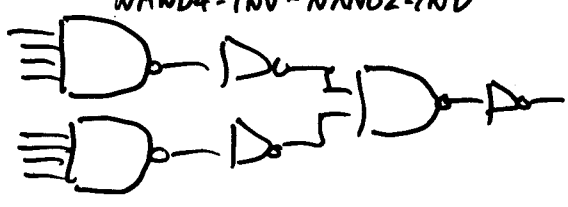


DeMorgan's equivalents



2.) AND 8

NAND4 - INV - NAND2 - INV



NAND2 - NOR2 - NAND2 - INV