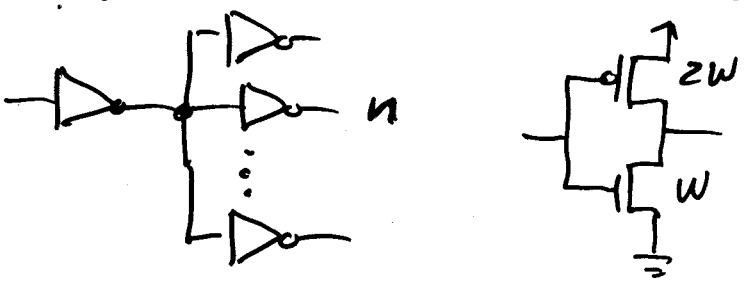
Shengyuan Li will lecture in ECE 4420 2/21 → 2/25

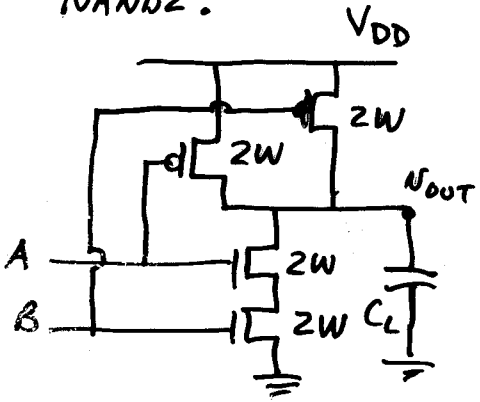
Fan-out (FO):

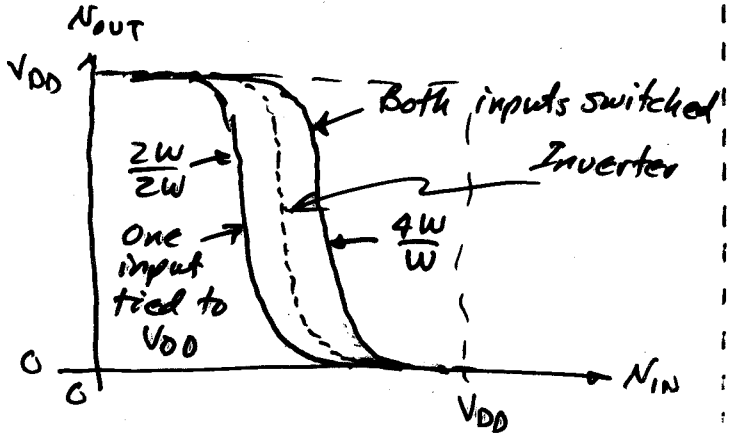
$$FO = \frac{C_{out}}{C_{gate}} = \frac{\text{Total capacitance driven by the gate}}{\text{Input capacitance of the gate}}$$



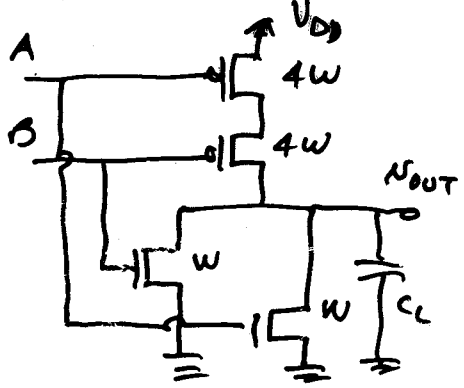
Voltage Transfer Curve of Some Simple CMOS Gates

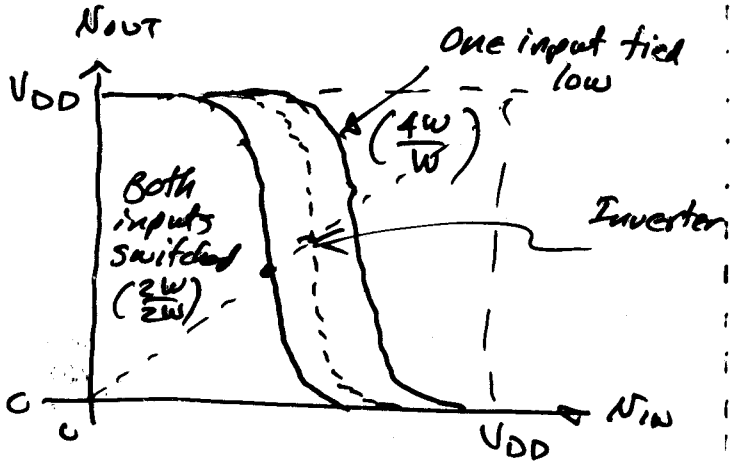
NAND2:





NOR2:





Example 5.2

Compute V_S for a NAND2 when a.) One-input is at V_{DD} and the other is switched from 0 to V_{DD}. b.) When both inputs are switched together. Assume 0.18 μm technology and all W's = 0.4 μm. (Assume $L = 0.2$ μm)

a.) $$X = \sqrt{\frac{W_N/E_{cN}L_N}{W_P/E_{cP}L_P}} = \sqrt{\left(\frac{W_N}{W_P}\right)\frac{E_{cP}L_P}{E_{cN}L_N}} = \sqrt{\frac{400}{400}\cdot\frac{4.8}{1.2}} = 2$$

$$\therefore V_S = \frac{V_{DD} - |V_{TP}| + X V_{TN}}{1+X} = \frac{1.8 - 0.5 + (2)(0.5)}{1+2} = 0.77V$$

b.) With both inputs tied together $W_P = 800$ nm, $W_L = 200$ nm

$$X = \sqrt{\frac{800}{800}\left(\frac{4.8}{1.2}\right)} = 1 \rightarrow V_{SS} = \frac{1.8 - 0.5 + 0.5(1)}{1+1} = 0.9V$$

COMPLEX CMOS GATES

Example

Synthesize $F = \overline{(A+B)\cdot C}$ in CMOS logic

How?

1.) De Morgan's Laws

$$\overline{(a+b)} = \bar{a}\cdot\bar{b}$$

$$\overline{(a\cdot b)} = \bar{a}+\bar{b}$$

Duality Relationships

$ab \Leftrightarrow a+b$

$(a+b)c \Leftrightarrow ab+c$

2.) AND in CMOS means series NMOS and parallel PMOS

OR in CMOS means parallel NMOS and series PMOS

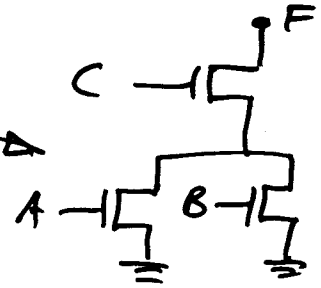
$$F = \overline{(A+B)\cdot C} = \overline{A+B} + \bar{C} = \bar{A}\cdot\bar{B} + \bar{C}$$

3.) Since NMOS acts to pull F low, synthesize the NMOS from $\bar{F}$.

$$F = \overline{(A+B)\cdot C} \rightarrow \bar{F} = \overline{\overline{(A+B)\cdot C}} = (A+B)\cdot C$$

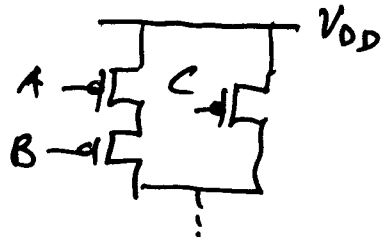
3.) Cont'd

$\bar{F} = (A+B)\cdot C$ →

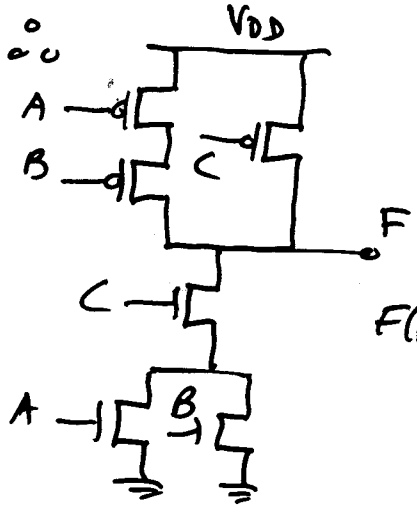


4.) Since the PMOS pulls F high, we can realize the PMOS by realizing F with all inputs complimented.

$F = \overline{(A+B)\cdot C} = \bar{A}\cdot\bar{B} + \bar{C}$ → $F = (A\cdot B) + C$



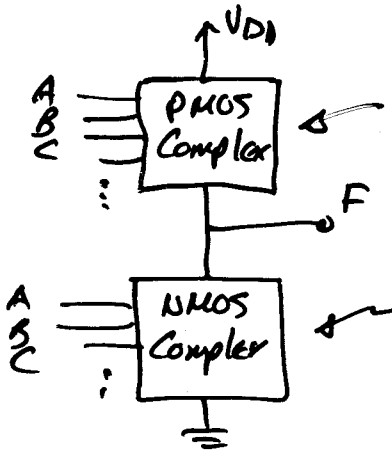
5.)



6) Note the $\bar{F}$ is the dual of $F(\bar{A},\bar{B},\bar{C})$

$F(\bar{A},\bar{B},\bar{C}) = A\cdot B + C \xrightarrow{\text{Dual}} \bar{F} = (A+B)\cdot C$

Generalization of Complex Gate Synthesis



Function of complemented variables that sets F = 1 and creates a path from F to V_{DD}.

Complement of the function that sets the output to 0 due to a path from F to ground.

1.) $\bar{F}$ → Implements the NMOS complex

2.) Dual $\bar{F}$ is used to implement the PMOS complex.

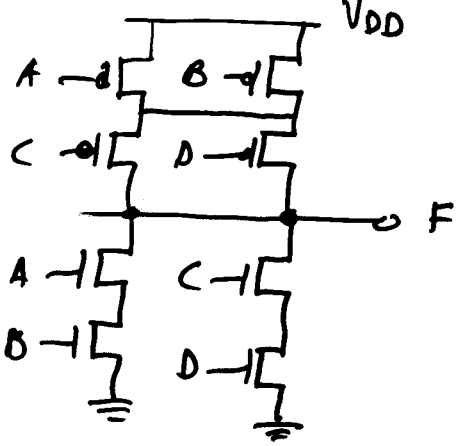
Ex. 5.3

Implement $F = \overline{AB+CD}$ as a single-stage CMOS gate and as a pseudo-NMOS gate.

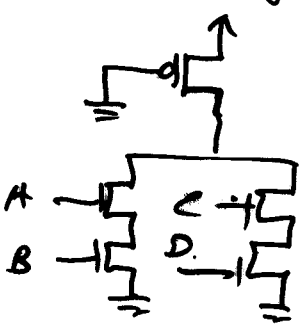
CMOS Gate:

$F = AB + CD$

$\bar{F}|_{dual} = (A+B)\cdot(C+D)$



pseudo-NMOS gate:



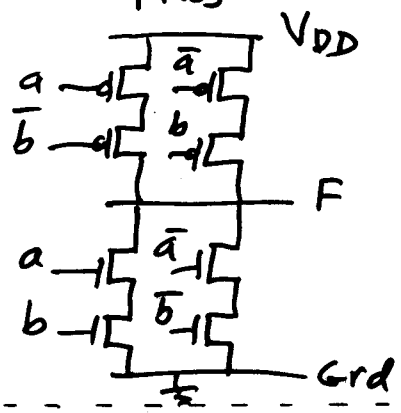
XOR Gate

$F_{XOR} = \bar{a}b + a\bar{b}$ → $\overline{F_{XOR}} = \overline{\bar{a}b + a\bar{b}} = (\bar{a}b)\cdot(a\bar{b})$

$= (a+\bar{b})\cdot(\bar{a}+b) = a\bar{a} + ab + \bar{b}\bar{a} + \bar{b}b$

$= ab + \bar{a}\bar{b}$ → NMOS

$F_{XOR}|_{dual} = \underbrace{a\cdot\bar{b} + \bar{a}b}_{PMOS}$



F_{XNOR} next