Power Dissipation in CMOS Gates

Fast chips get hot! Power Dissipation is a big deal now!

Types of Power:
- Dynamic: Capacitive Switching, Short-Circuit, & Glitches
- Static: Leakage Current and DC Standby Power

Dynamic (switching) Power:

\[
W = \int_0^t V_{in}(t)I(t)dt = \int_0^t V_{in}I(t)dt = \int_0^t V_{in}(\frac{dV}{dt})dt
\]

\[
= C_L V_{dd}^2
\]

In changing \( C_L \), Energy stored:

\[
\int_0^t V_{dd}^2 \frac{dV}{dt}dt = \int_0^t V_{dd}^2 dV = \frac{1}{2} C_L V_{dd}^2
\]

In changing \( C_F \), Energy dissipated by \( R_P \):

\[
\frac{1}{2} C_F V_{dd}^2 - \frac{1}{2} C_L V_{dd}^2 = \frac{1}{2} \left( C_L - C_F \right) V_{dd}^2
\]

Now in discharging \( C_F \) via \( R_N \):

Similar argument \( \Rightarrow \frac{1}{2} C_F V_{dd}^2 \) dissipated by \( R_N \)

\[
\Rightarrow \text{Thus in one complete cycle (charging & discharging), The total energy delivered by } V_{dd} \text{ is } \frac{1}{2} C_F V_{dd}^2
\]

\[
P_{\text{switching}} = (C_F V_{dd}^2) \frac{f_{avg}}{f_{clk}} = (C_F V_{dd}^2) \frac{f_{avg}}{f_{clk}}
\]

where \( \frac{f_{avg}}{f_{clk}} = \sum_{i=1}^{N-1} \frac{f_{avg}}{f_{clk}} = \frac{\text{No. of toggles}}{\text{No. of clock cycles} \times f_{clk}} \)

is the activity factor.
Dynamic Short Circuit Power

One interesting observation:
\[ V_{TN} < V_{IN} < V_{DD} - |V_{TP}| \text{ for both on. What if} \]
\[ V_{DD} \leq V_{TN} + |V_{TP}| ? \]

Tune back later.

Let \( \Delta V_{SC} = \Delta V_{Scr} + \Delta V_{Scf} \)

\[ \Delta V_{SC} \]

\[ P_{SC} = I_{SC} V_{DD} = \frac{\Delta V_{SC}}{I_{SC}(\text{aver.})} V_{DD} = \Delta V_{SC} I_{SC}(\text{aver.}) V_{DD} \text{ fck} \]

Let \( I_{SC}(\text{aver.}) = C_{dec} \frac{dV}{dt} = C_{L} V_{DD} \text{ fck} \rightarrow P_{SC} = C_{SC} V_{DD}^2 \text{ fck} \)

Define a switching activity factor \( \alpha_{SC} = \frac{C_{SC}}{C_L} \)

\[ P_{SC} = \alpha_{SC} C_{L} V_{DD}^2 \text{ fck} \]

Thus,
\[ P_{\text{dynamic}} = P_{\text{switching}} + P_{SC} = \alpha_{SC} C_{L} V_{DD}^2 \text{ fck} + \alpha_{SC} C_{L} V_{DD}^2 \text{ fck} \]

(Tradeoff occurs between the dynamic power of the previous gate and the short circuit power of the next gate)

Glitch Power

A glitch is an undesired switching of the output and adds to the switching power

See example 5.7:
Static Power

Sources:

1.) Subthreshold - \( I_{\text{sub}} = I_s \exp\left[\frac{q(V_{\text{DS}} - V_T - V_{\text{off}})}{m k T}\right] \left[1 - \exp\left(\frac{-q V_{\text{DS}}}{k T}\right)\right] \)

2.) pn junction - \( I_{\text{pn}} = I_o \left[\exp\left(\frac{q V_{\text{GS}}}{k T}\right) - 1\right] \), \( I_o = A J_3 \)

\[ P_{\text{static}} = (I_{\text{sub}} + I_{\text{pn}}) V_{\text{DD}} = I_{\text{leak}} V_{\text{DD}} \]

Pseudo-NMOS logic:

This logic has a current flow, \( I_{\text{dc}} \), when \( V_{\text{out}} = V_{\text{OL}} \).

\( \therefore P_{\text{dc}} = I_{\text{dc}} V_{\text{DD}} \)

Complete Power

CMOS: \( P = \alpha C V_{\text{DD}}^2 f_{\text{clk}} + I_{\text{leak}} V_{\text{DD}} \)

Pseudo-NMOS: \( P = \alpha C V_{\text{DD}}^2 f_{\text{clk}} + I_{\text{leak}} V_{\text{DD}} + I_{\text{dc}} V_{\text{DD}} \)

Power and Delay Tradeoffs

Power-delay product:

\[ PDP = P \times \frac{1}{f_{\text{clk}}} \]

\( \therefore PDP = \alpha C V_{\text{DD}}^2 f_{\text{clk}} \left(\frac{1}{f_{\text{clk}}}\right) = \frac{C V_{\text{DD}}^2}{2} \) (Energy)

Good metric but difficult to compare design with.

Energy-delay product:

\[ EDP = PDP \times \frac{1}{f_{\text{clk}}} \]

\( \therefore EDP = \frac{C^2 V_{\text{DD}}^3}{2 K_2 (V_{\text{DD}} - V_T)} \)

Optimum \( V_{\text{DD}} \) with \( V_{\text{DD}} \):

\[ \frac{\partial EDP}{\partial V_{\text{DD}}} = 0 \rightarrow V_{\text{DD}} (\text{opt}) = V_{\text{DD}}^* = \frac{3}{2} V_T \]