Power Dissipation in CMOS Gates

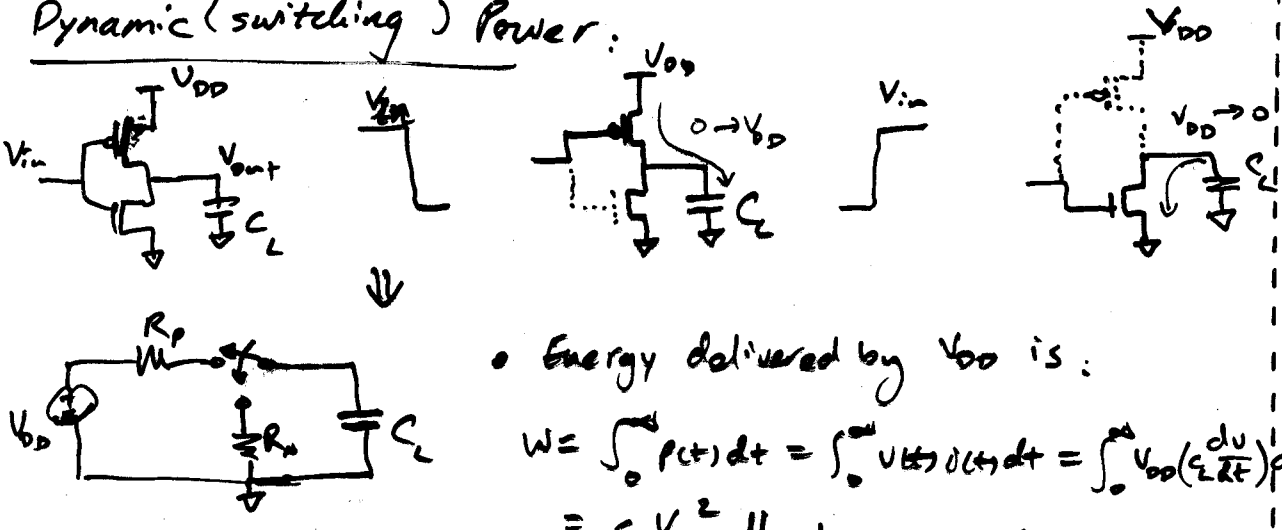
Fast chips get hot ! Power Dissipation is a big deal now !

Types of Power:

Dynamic : Cap. Switching , Short-ckt , & glitches

static : Leakage current and DC standby power

Dynamic (switching) Power:



- Energy delivered by V_{DD} is:

$$W = \int_0^\infty p(t)\,dt = \int_0^\infty V(t)\,i(t)\,dt = \int_0^\infty V_{DD}\left(C_L \frac{dv}{dt}\right)dt$$

$$= C_L V_{DD}^2$$

- In charging C_L, Energy stored:

$$\int_0^\infty V\left(C\frac{dv}{dt}\right)dt = \int_0^{V_{DD}} C_L V\,dv = \frac{1}{2}C_L V_{DD}^2$$

Hence, in charging C_L

$C_L V_{DD}^2 - \frac{1}{2}C_L V_{DD}^2 = \frac{1}{2}C_L V_{DD}^2$ Dissipated by R_P

- Now in discharging C_L via R_N

Similar argument $\Rightarrow \frac{1}{2}C_L V_{DD}^2$ dissipated by R_N

$\Rightarrow$ Thus in one complete cycle (charging & discharging):

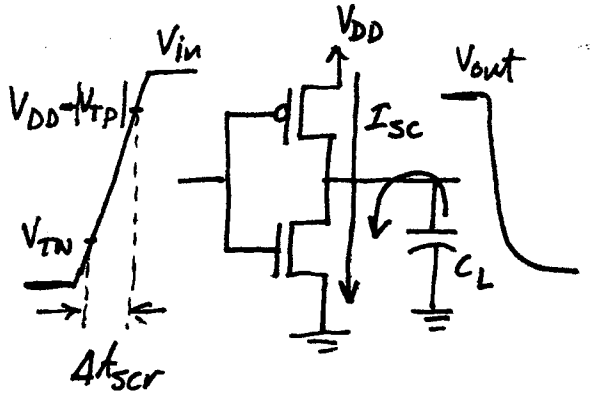
The total energy delivered by V_{DD} is $C V_{DD}^2$

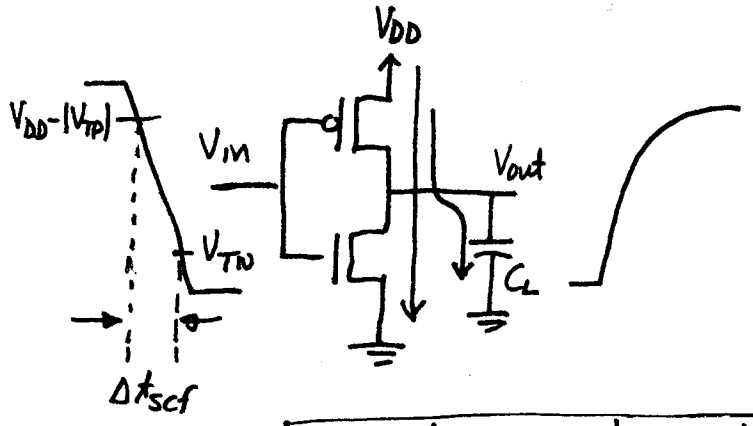
$$\Rightarrow P_{switching} = \left(C_L V_{DD}^2\right) f_{avg} = \left(C_L V_{DD}^2\right) \alpha_{0\to1} f_{CLK}$$

where $\alpha_{0\to1} = \dfrac{f_{avg}}{f_{CLK}} = \dfrac{(\text{No. of toggles}/2)}{\text{No. of clock cycle}}$

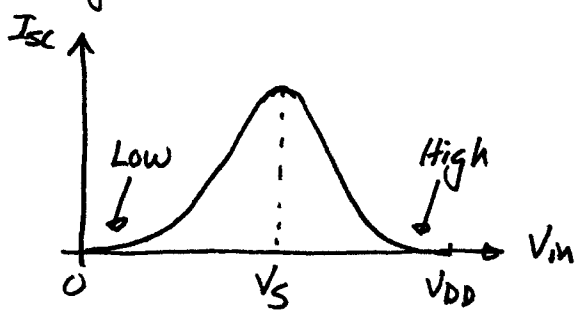
is the activity factor.

Dynamic Short Circuit Power





or another way,



One interesting observation: $V_{TN} < V_{in} < V_{DD} - |V_{TP}|$ for both on. What if $V_{DD} \leq V_{TN} + |V_{TP}|$?

Tune back Later.

Let $\Delta t_{sc} = \Delta t_{scr} + \Delta t_{scf}$

$\therefore P_{SC} = I_{SC} V_{DD} = \frac{\Delta t_{sc}}{T} I_{sc}(aver.) V_{DD} = \Delta t_{sc} I_{sc}(aver.) V_{DD} f_{clk}$

Let $I_{sc}(aver.) = C\frac{dv}{dt} = C_{sc}\frac{V_{DD}}{\Delta t_{sc}}$ $\rightarrow P_{SC} = C_{sc} V_{DD}^2 f_{clk}$

Define a switching activity factor $\alpha_{sc} = \frac{C_{sc}}{C_L}$

$\therefore P_{sc} = \alpha_{sc} C_L V_{DD}^2 f_{clk}$

Thus, $P_{dynamic} = P_{switching} + P_{SC} = \alpha_{0\rightarrow1} C_L V_{DD}^2 f_{clk} + \alpha_{sc} C_L V_{DD}^2 f_{clk}$

$= \alpha C_L V_{DD}^2 f_{clk}$

(Tradeoff occurs between the dynamic power of the previous gate and the short circuit power of the next gate

Glitch Power

A glitch is an undesired switching of the output and adds to the switching power

See example 5.7.

Static Power

Sources:

1.) Subthreshold – $I_{sub} = I_s \exp\left[\frac{q(V_{GS} - V_T - V_{offset})}{m k T}\right]\left[1 - \exp\left(\frac{-q V_{DS}}{kT}\right)\right]$

2.) pn junction – $I_{pn} = I_0\left[\exp\left(\frac{q V_{SB}}{kT}\right) - 1\right]$, $I_0 = A J_s$

$P_{static} = (I_{sub} + I_{pn}) V_{DD} = I_{leak} V_{DD}$

Pseudo-NMOS logic:

This logic has a current flow, I_{DC}, when $V_{out} = V_{OL}$.

$\therefore P_{DC} = I_{DC} V_{DD}$

Complete Power

CMOS: $P = \alpha C V_{DD}^2 f_{clk} + I_{leak} V_{DD}$

Pseudo-NMOS: $P = \alpha C V_{DD}^2 f_{clk} + I_{leak} V_{DD} + I_{DC} V_{DD}$

Power and Delay Tradeoffs

Power-delay product:

$$PDP = P_{avg.}\, t_p = \left(C V_{DD}^2 f_{clk}\right)\left(\frac{1}{2 f_{clk}}\right) = \frac{C V_{DD}^2}{2} \quad \text{(Energy)}$$

Good metric but difficult to compare design with.

Energy-delay product:

$$EDP = PDP \times t_p$$

$$t_p = \frac{C\Delta V}{I} = \frac{C\Delta V}{I_{sat.}} = \frac{C V_{DD}}{K_2(V_{DD} - V_T)}$$

$$\therefore EDP = \frac{C^2 V_{DD}^3}{2 K_2 (V_{DD} - V_T)}$$

K_2 = constant that depends on device sizes

Optimum w.r.t V_{DD}:

$$\frac{\partial EDP}{\partial V_{DD}} = 0 \longrightarrow V_{DD}(opt.) = V_{DD}^* = \frac{3}{2} V_T$$