HIGH-SPEED CMOS LOGIC DESIGN (Chap. 6)

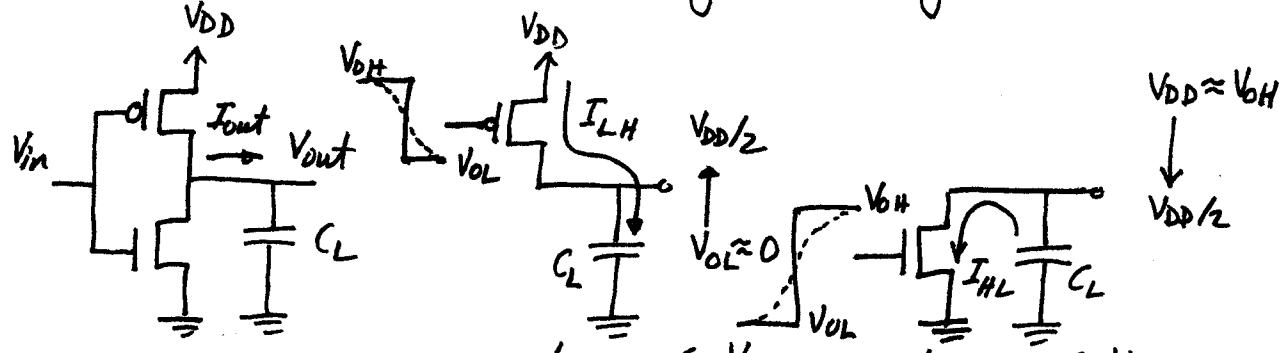
Introduction

Goal: Maximize the speed of a circuit while minimizing the area and power dissipation

Speed - propagation delay is the time from the 50% point of the input to the 50% point of the output. (can be negative ⇒ input rise/fall < output rise/fall)

Switching Time Analysis for a CMOS Gate

Goal: To size the transistors for a given delay given C_L.



$$t_{pLH} = \frac{C_L V_{DD}}{2 I_{LH}} \qquad t_{pHL} = \frac{C_L V_{DD}}{2 I_{HL}}$$

What is I_{LH} and I_{HL}?

$$t_p = \frac{t_{pLH} + t_{pHL}}{2}$$

1.) I_{LH} -

$$V_{Dsat} = \frac{(V_{GS} - V_T) E_c L}{(V_{GS} - V_T) + E_c L} \xrightarrow{0.13\mu m} V_{Dsat.} = \frac{(V_{DD} - |V_T|) E_c L}{(V_{DD} - |V_T|) + E_c L}$$

$\therefore$ PMOS is in saturation ← $V_{Dsat.} = \frac{(1.2 - 0.4)(2.4)}{(1.2 - 0.4) + 2.4} = 0.6V$

and $I_{LH} = (I_{Dsat})_p \rightarrow t_{pLH} = \frac{C_L V_{DD}}{2 (I_{Dsat.})_p}$

Previously, $t_{pLH} = 0.7 R_p C_L$

$$R_p = \frac{V_{DD}/2}{0.7 (I_{Dsat})_p}$$

2.) I_{HL}

$$V_{Dsat} = \frac{(1.2 - 0.4) 0.6}{(1.2 - 0.4) + 0.6} = 0.34V \Rightarrow \text{NMOS is in saturation}$$

$\therefore$ $I_{HL} = (I_{Dsat})_n \rightarrow t_{pHL} = \frac{C_L V_{DD}}{2 (I_{Dsat.})_n}$

Previously, $t_{pHL} = 0.7 R_N C_L$

$$R_N = \frac{V_{DD}/2}{0.7 (I_{Dsat})_n}$$

Example 6.1

Using 0.13μm technology, find R_{eqn} and R_{eqp}. ($W_N = W_P = 0.1\mu m$)

NMOS:

$$I_{Dsat} = \frac{W_N v_{sat} C_{ox} (V_{DD} - V_{TN})^2}{(V_{DD} - V_{TN}) + E_{CN} L_N} = \frac{(0.1\times10^{-4})(e\times10^{6})(1.6\times10^{-6})(1.2-0.4)^2}{(1.2-0.4)+0.6} = 585\mu A$$

$$\therefore R_{eqn} = R_N = \frac{L2/2}{0.7(585\mu A)} = 14.65 k\Omega \quad (R_{eqn.} \simeq 125 k\Omega/\square)$$

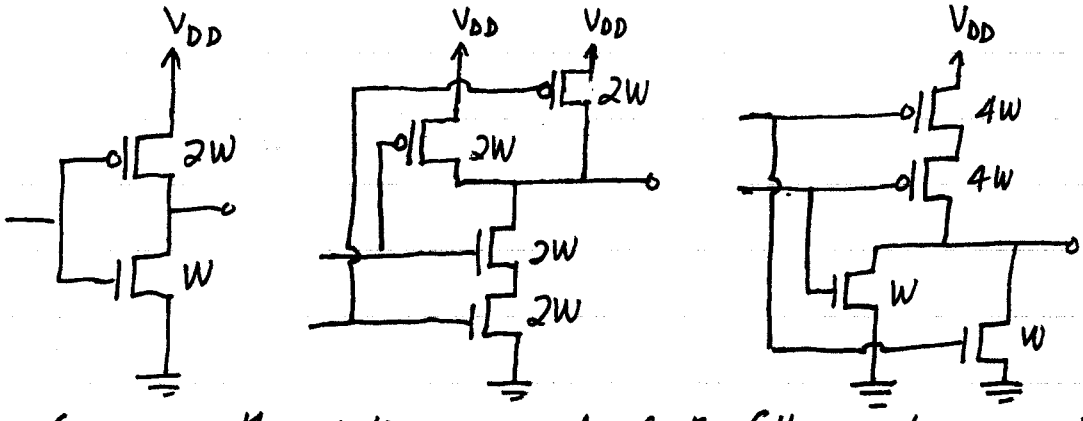
PMOS:

$$I_{Dsat} = \frac{W_P v_{sat} C_{ox} (V_{DD} - |V_{TP}|)^2}{(V_{DD} - |V_{TP}|) + E_{CP} L_P} = \frac{(0.1\times10^{-4})(e\times10^{6})(1.6\times10^{-6})(1.2-0.4)^2}{(1.2-0.4)+2.4} = 26\mu A$$

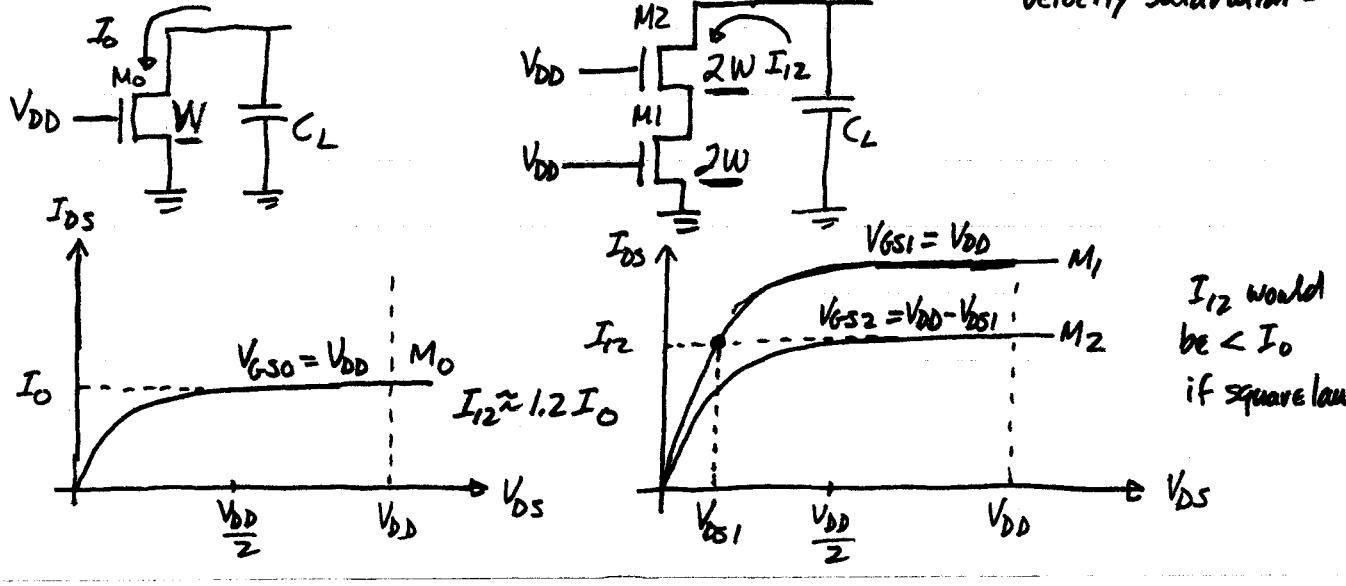
$$\therefore R_{eqp} = R_P = \frac{1.2/2}{0.7(26\mu A)} = 32.97 k\Omega \quad (R_{eqp.} \simeq 30 k\Omega/\square)$$

Logic Gate Sizing Including Velocity Saturation Effects

No velocity saturation:

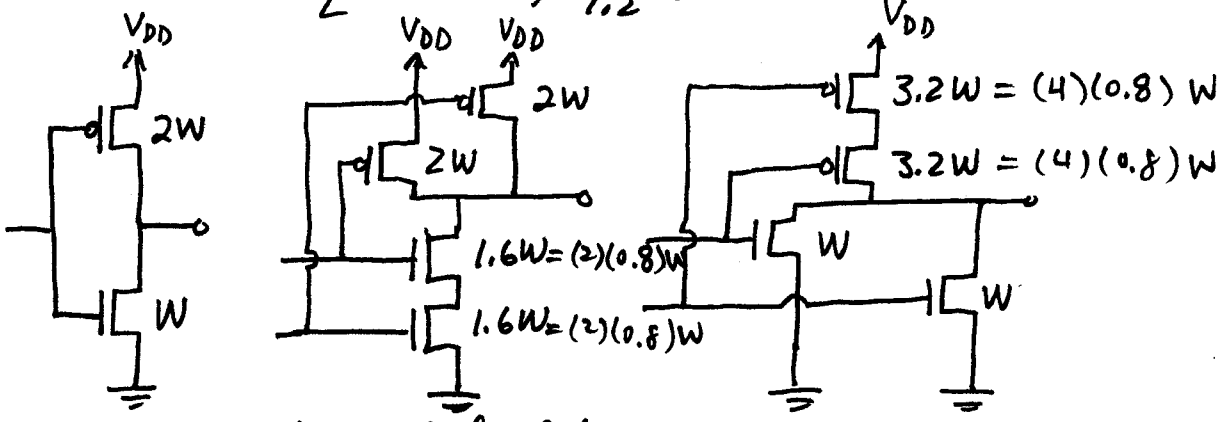


Compare the sinking current of the following two circuits assuming velocity saturation -

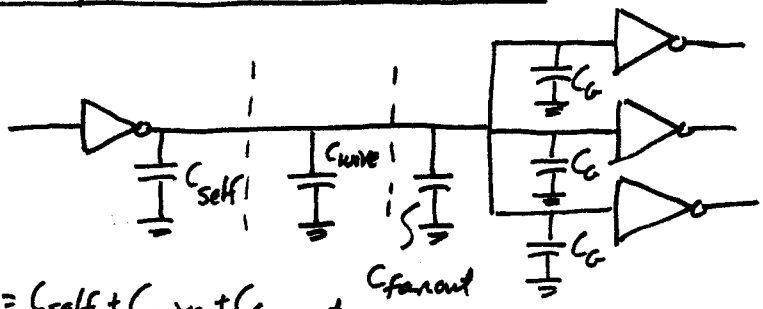


Logic Gate Sizing Including Velocity Sat. Effects - Cont'd

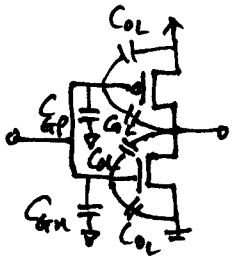
∴ For stacked devices with velocity saturation to produce the same current as a single transistor, scale the $\frac{W}{L}$ ratio by $\frac{1}{1.2} \simeq 0.8$.



Load Capacitance Calculation



$C_L = C_{self} + C_{wire} + C_{fanout}$



Fanout Capacitance

$C_{fanout} = \sum C_G =$

$C_G = C_{GN} + 2C_{OL} + C_{GP} + 2C_{OL}$

$= C_{ox} W_n L + 2C_{OL} W_n + C_{ox} W_p L + 2C_{OL} W_p$

$= (C_{ox} L + 2C_{OL})(W_n + W_p)$

$= C_g (W_n + W_p)$

$C_g = C_{ox} L + 2C_{OL}$

$= (1.6 \times 10^{-6}\ F/cm^2)(0.1\ \mu m)$

$+ 2\ (0.25\ fF/\mu m) \simeq 2\ fF/\mu m$

$\Rightarrow C_G = (2\ fF/\mu m)(W_n + W_p)$

$\Rightarrow C_{fanout} = \sum C_G = (n)(C_G)$ for n identical inverters

$= (2\ fF/\mu m)(\underbrace{W_{p_1} + W_{n_1}}_{\text{1st inv.}} + \underbrace{W_{p_2} + W_{n_2}}_{\text{2nd inv.}} + \ldots)$