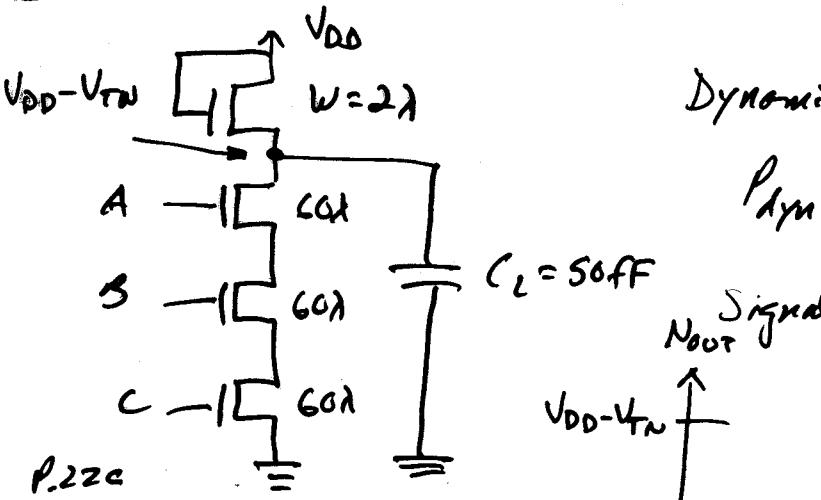
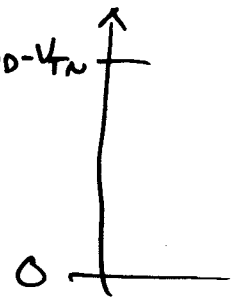
P5.11



Dynamic Power -

$P_{dyn} = C V_{DD}^2 f$

Signal swing



$P_{switching} = C_L \Delta V_{swing} f V_{DD}$

$= C(V_{DD}-V_{TN})V_{DD} f$

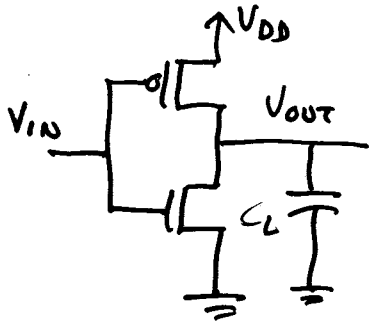
Lecture 2/21 — 2/25

Complex gates
Flip flops
Power dissipation in CMOS gates

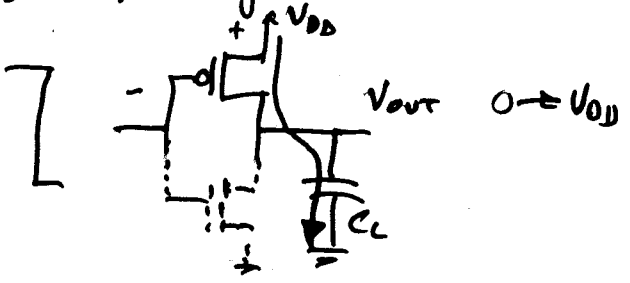
Types of Power

Dynamic – capacitor charging & discharging, short-ckt., glitches
Static – dc & leakage

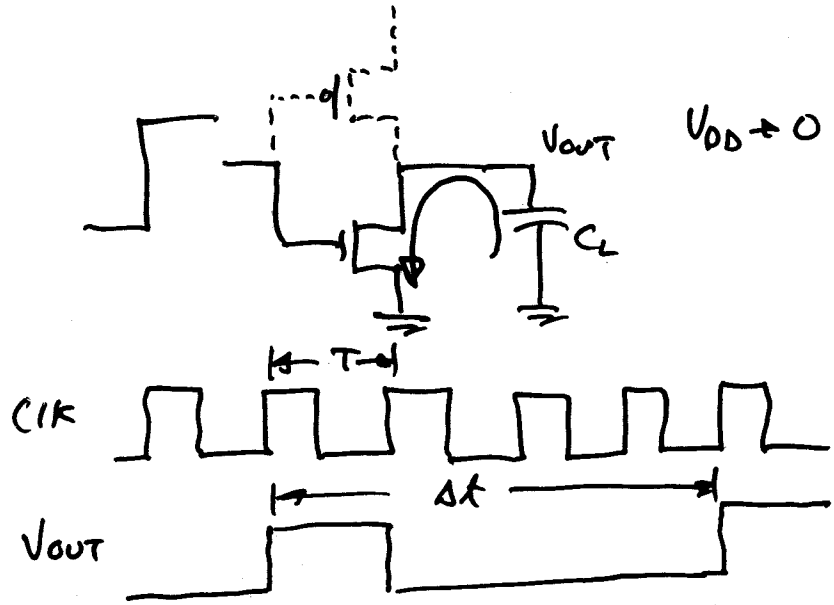
Dynamic (Switching) Power



1.) Input high → low



2.) Input low → high



$$I_D(aver) = C\frac{dv}{dt} = C_L \frac{\Delta V_{swing}}{\Delta t} = C_L V_{DD} f_{aver.}$$

where $f_{aver} = \frac{1}{\Delta t}$

$$P_{switching} = I_D(aver)\, V_{DD} = C_L V_{DD}^2 f_{aver.} = \alpha_{0\to1} C_L V_{DD}^2 f_{clk}$$

where $\alpha_{0\to1} = \frac{f_{aver.}}{f_{clk}} = \frac{\text{Toggle/2}}{\text{No. clock cycles}} = \frac{4/2}{8} = \frac{1}{4}$ for the above example

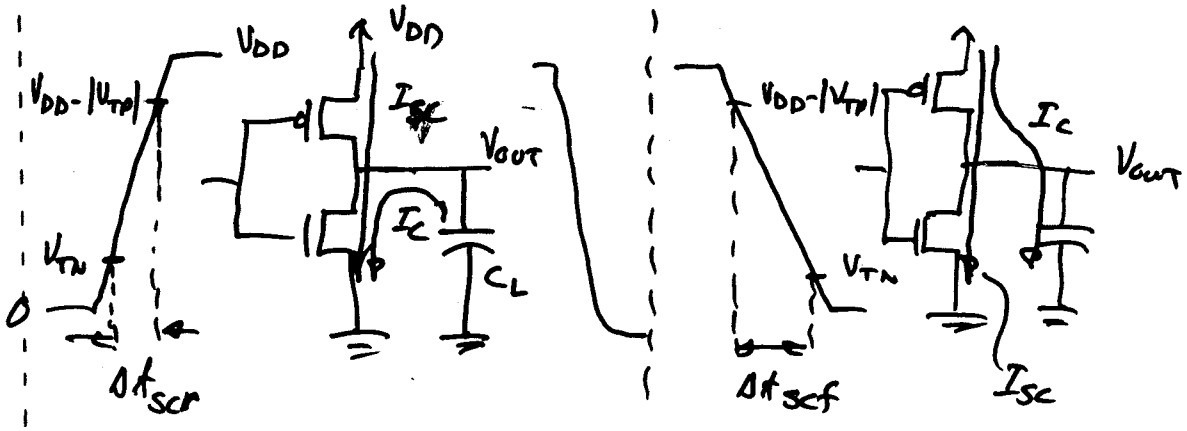
Example 5.6

Compute the switching power for a CMOS inverter with $C_L = 50fF$ and $f_{aver.} = 250MHz$. Let $V_{DD} = 1.8V$.

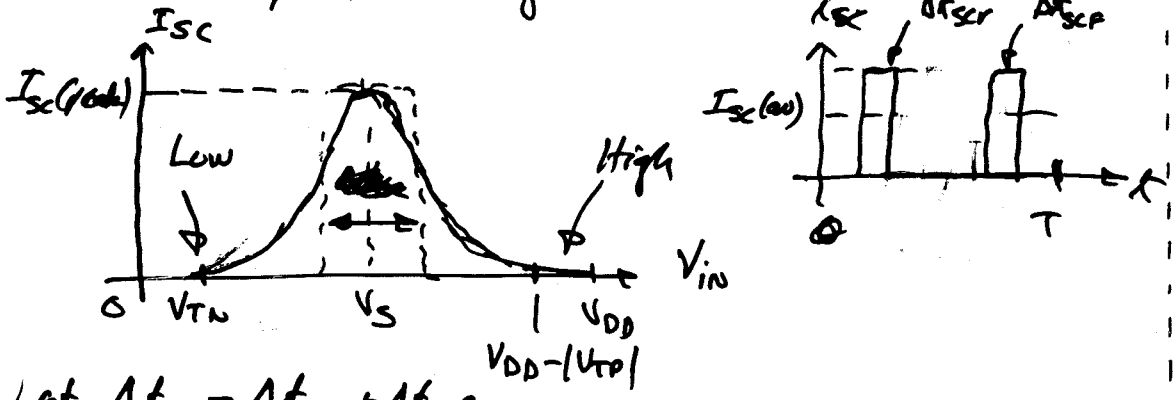
$$P = CV^2f = (50\times10^{-15})(1.8)^2(250\times10^6) = 40.5\mu W$$

(Simulation gives 46.3μW)

Dynamic Short Circuit Power



Another way of looking at the I_{sc}:



Let $\Delta t_{sc} = \Delta t_{scr} + \Delta t_{scf}$

$$P_{sc} = I_{sc} V_{DD} = \frac{\Delta t_{sc}}{T} \times I_{sc(ave)} V_{DD} = \Delta t_{sc} I_{sc(ave)} V_{DD} f$$

$$I_{sc(ave)} = C\frac{dv}{dt} = C_{sc}\frac{V_{DD}}{\Delta t_{sc}}$$

$$P_{sc} = \frac{C_{sc} V_{DD}}{\Delta t_{sc}} \cdot \Delta t_{sc} V_{DD} f = C_{sc} V_{DD}^2 f = \alpha_{sc} V_{DD}^2 C_L f$$

where $\alpha_{sc} = \frac{C_{sc}}{C_L}$ $\qquad$ $P_{sc} = \alpha_{sc} V_{DD}^2 C_L f$

$$P_{dynamic} = P_{switching} + P_{sc} = (\alpha_{0\to1} + \alpha_{sc}) V_{DD}^2 C_L f = \alpha V_{DD}^2 C_L f$$

(There can be a tradeoff between switching and SC power)

Glitch power –

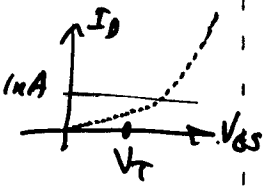
A glitch is an undesired switching of the output and adds to the power.

Static Power

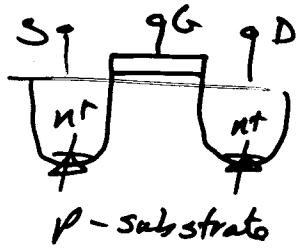
Sources:

1.) Subthreshold $I_{sub} = I_s \exp\left[\frac{q(V_{GS}-V_T-V_{off})}{nkT}\right]\left[1-\exp\left(-\frac{qV_{DS}}{kT}\right)\right]$

$I_{sub} \propto \exp\left[\frac{q(V_{GS}-V_T)}{nkT}\right]$



2.) PN junction leakage



$I_{pn} = I_o\left[\exp\left(\frac{qV_{SB}}{kT}\right)-1\right]$

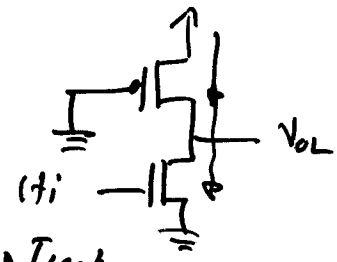
Reverse biased $I_{pn} \simeq -I_o$

Static Power = $P_{static} = \underbrace{(I_{sub} + I_{pn})}_{I_{leak}} V_{DD} \longrightarrow 0$

Psuedo-NMOS logic:

This logic has dc flow when $V_{out} = V_{OL}$.

$\therefore P_{DC} = I_{DC} V_{DD}$



Complete power:

CMOS – $P = \alpha C V_{DD}^2 f_{clk} + V_{DD} I_{Leak}$

Psuedo-NMOS – $P = \alpha C V_{DD}^2 f_{clk} + V_{DD}(I_{leak} + I_{DC})$

Power & Delay Tradeoff

Power x Delay = PDP and is a constant

$PDP = P_{aver} t_p = (C V_{DD}^2 f_{clk})\left(\frac{1}{2 f_{clk}}\right) = \frac{1}{2} C V_{DD}^2$ (energy)