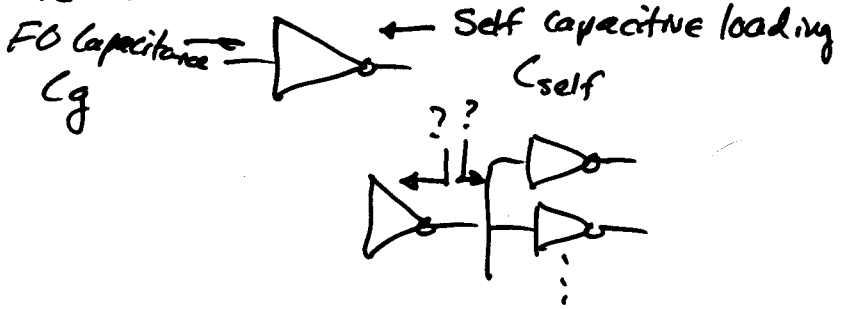
Homework #7 postponed until Friday (3/4/05)

Exam #2 3/11/05 Dr. Sengupta will lecture on Friday.

CHAPTER 6 – HIGH-SPEED CMOS LOGIC DESIGN

Overview:

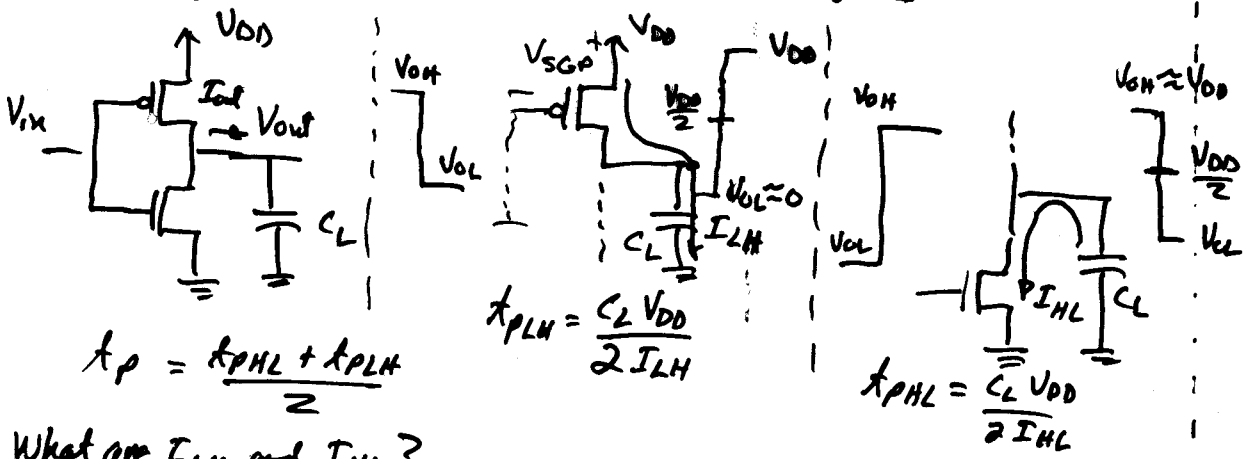


Goal of Chap. 6

Maximize the speed of a logic circuit while minimizing the power and area.

Speed => Propagation delay time

Switching Time Analysis for a CMOS gate



$$t_p = \frac{t_{PHL} + t_{PLH}}{2}$$

$$t_{PLH} = \frac{C_L V_{DD}}{2 I_{LH}}$$

$$t_{PHL} = \frac{C_L V_{DD}}{2 I_{HL}}$$

What are I_{LH} and I_{HL}?

1.) I_{LH}

$$V_{Dsat} = \frac{(V_{GS} - V_T) E_c L}{(V_{GS} - V_T) + E_c L} \xrightarrow{0.13\mu m} V_{Dsat} = \frac{(1.2 - 0.4)(2.4)}{(1.2 - 0.4) + 2.4} = 0.6$$

$\therefore$ PMOS is in saturation $\rightarrow I_{LH} = (I_{Dsat})_p$

$$t_{PLH} = \frac{C_L V_{DD}}{2 (I_{Dsat})_p} = 0.7 R_p C_L \rightarrow R_p = \frac{V_{DD}/2}{0.7 (I_{Dsat})_p}$$

2.) I_{HL}

$$V_{Dsat} = \frac{(1.2-0.4)(0.6)}{(1.2-0.4)+0.6} = 0.34V \leftarrow \text{NMOS saturated}$$

$$t_{pHL} = \frac{C_L V_{DD}}{2(I_{sat})_n} = 0.7 R_N C_L \rightarrow R_N = \frac{V_{DD}/2}{0.7(I_{sat})_n}$$

Ex. 6.1

Using 0.13 μm technology, find R_{eqn} and R_{eqp} ($W_N = W_p = 0.1\mu m$) ($L = 0.1\mu m$)

NMOS:

$$I_{Dsat} = \frac{W_N v_{sat} C_{ox}(V_{DD}-V_{TN})^2}{(V_{DD}-V_{TN}) + E_{CN} L_N} = \frac{(0.1\times10^{-4})(5\times10^{6})(1.6\times10^{-6})(1.2-0.4)^2}{(1.2-0.4)+0.6}$$

$$= 58.5\mu A$$

$$R_{eqn} = R_N = \frac{V_{DD}/2}{0.7(I_{Dsat})_n} = \frac{0.6}{0.7(58.5\mu A)} = 14.65k\Omega$$

Further examination shows that in general $R_{eqn} \approx 12.5k\Omega/\square$

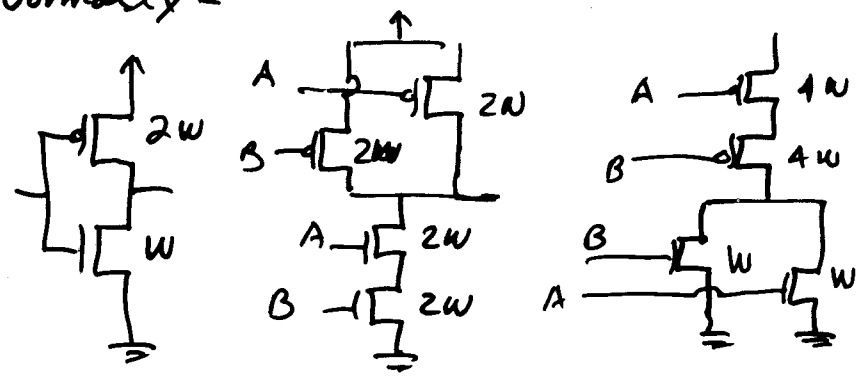
PMOS:

$$I_{Dsat} = \frac{(0.1\times10^{-4})(8\times10^{6})(1.6\times10^{-6})(1.2-0.4)^2}{(1.2-0.4)+2.4} = 26\mu A$$

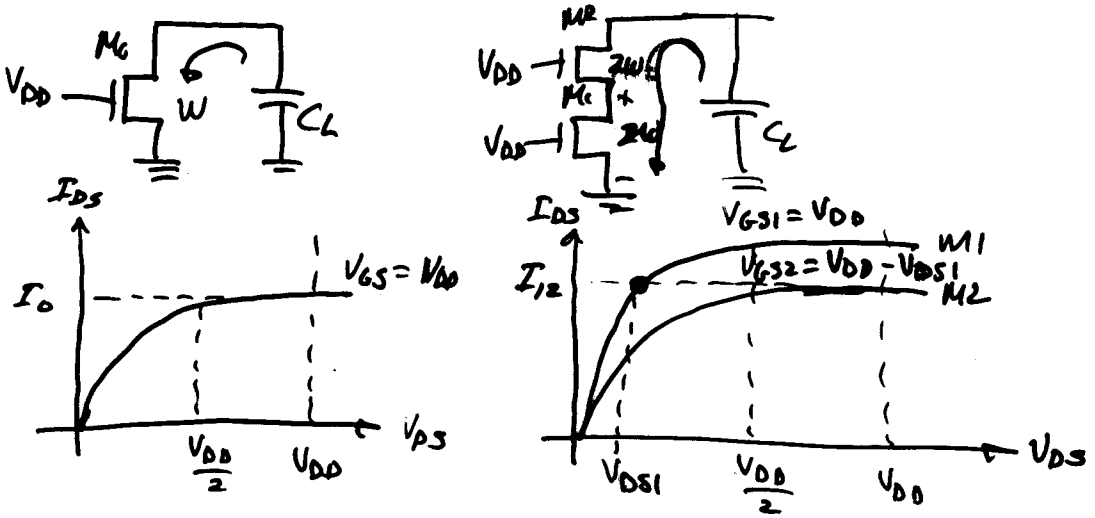
$$R_{eqp} = R_p = \frac{V_{DD}/2}{0.7(I_{Dsat})_p} = 32.97k\Omega \rightarrow R_{eqp} \approx 30k\Omega/\square$$

Logic Gate Sizing Including Velocity Sat. Effects

Normally –



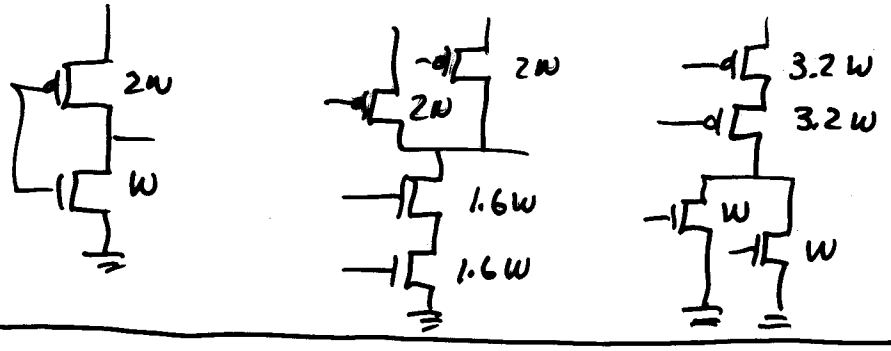
Velocity Saturation effects -



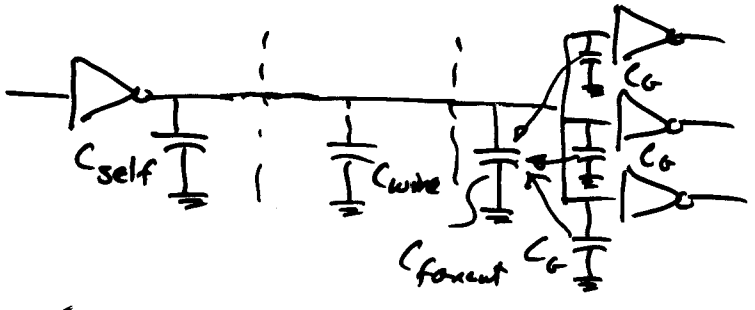
Because of velocity sat $I_{12} \approx 1.2 I_0$

For stacked devices with velocity saturation, to produce the same current as a single transistor, scale the W/L ratio by $\frac{1}{1.2} \approx 0.8$

For stacked transistor with velocity saturation -

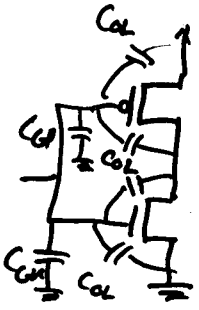


Find C_{FO} and C_{self} - Load capacitance calculation



$C_L = C_{self} + C_{wire} + C_{fanout}$

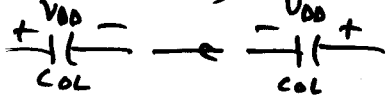
Fanout Capacitance



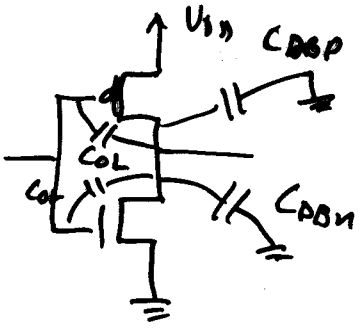
$$C_G = C_{Gn} + 2C_{OL} + C_{Gp} + 2C_{OL}$$
$$= C_{ox} W_N L + 2C_{ol} W_n + C_{ox} W_p L + 2C_{ol} W_p$$
$$= (C_{ox} + 2C_{ol})(W_n + W_p)$$
$$= \left[1.6 \frac{fF}{\mu m} + 2 \cdot 0.25 fF/\mu m\right](W_n + W_p)$$
$$= (2\ fF/\mu m)(W_N + W_p)$$

$\therefore C_G = C_g (W_n + W_p)$ $\quad \boxed{C_g \simeq 2 fF/\mu m}$ SPICE gives 2.2 fF/μm

$\therefore C_{fanout} = \Sigma C_G = n C_G = n C_g (W_n + W_p)$
$= C_g (W_{n1} + W_{p1} + W_{n2} + W_{p2} + \cdots)$



Self Capacitance



$C_{self} = C_{DBn} + C_{DBp} + 2C_{OL} + 2C_{OL}$
$= (C_j + 2C_{ol})(W_n + W_p)$

C_j: 1 fF/μm

$\boxed{C_{self} = 1 fF/\mu m}$

SPICE 0.7 ↑ 0.8 ↓