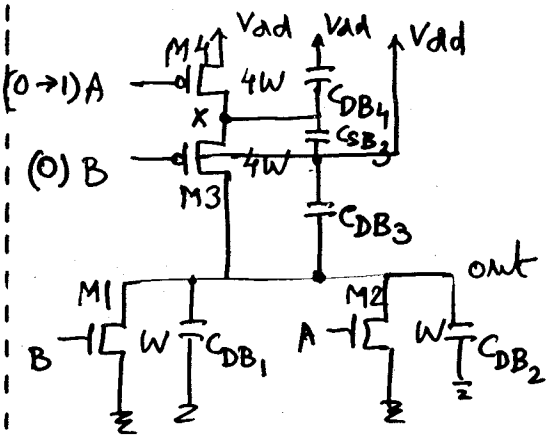
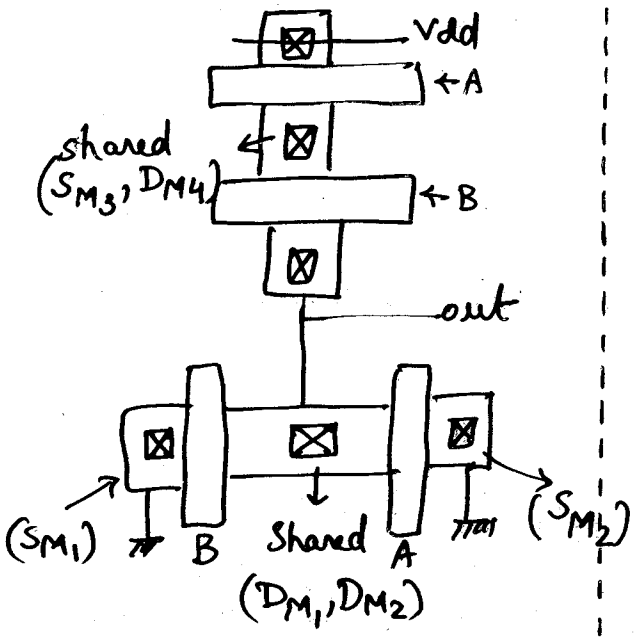
Capacitance of NOR2





Worst case

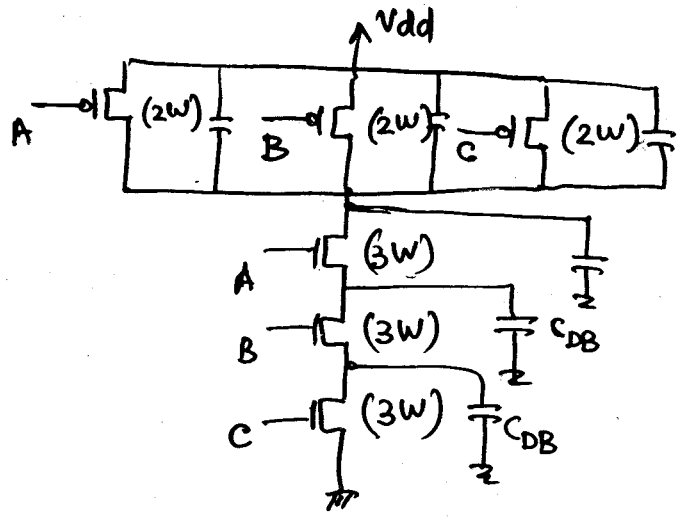
$$C_{load} = C_{self} = \underbrace{(C_{DB_1} + C_{DB_2})}_{\text{Shared}} + C_{DB_3} + \underbrace{(C_{SB_3} + C_{DB_4})}_{\text{shared}}$$

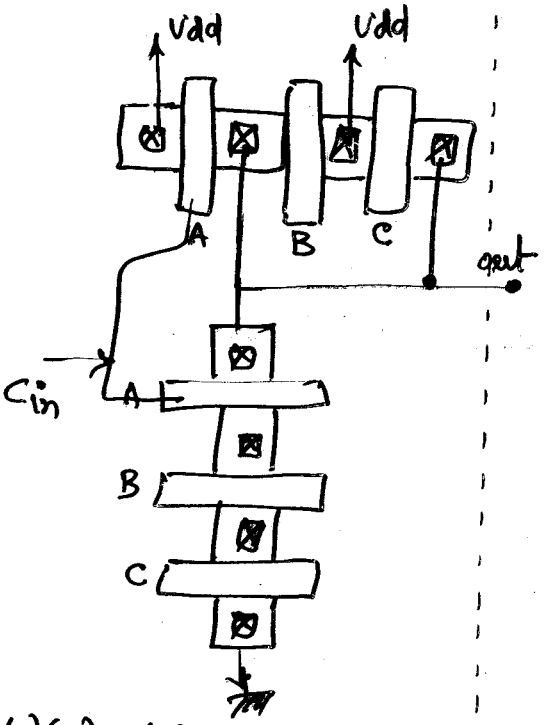
$$= C_{eff}(W_n) + C_{eff}(W_p) + C_{eff}(W_p)$$

$$= C_{eff}.(W_n + 2W_p) = 9W.(1ff/um)$$

$$C_{in}\ (\text{worst case}) = C_g(W_n + W_p) = 5W C_g = 5W(2ff/um)$$

NAND 3





C_{in} (worst case) $= C_g(W_n + W_p)$

$\approx 5W C_g = 5(0.4)(2) = 4$ ff.

W

$C_{Load} = C_{self}[2W_p + 3W_n] = (1\text{ ff/um})[4W + 9W] = 13(0.4)$

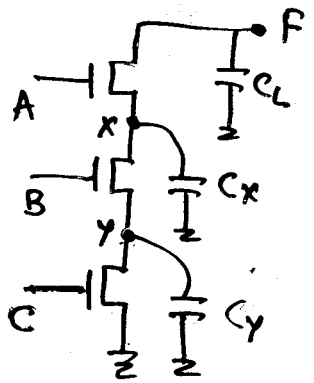
$= 5.2$ ff

Switching Implications on Gates

① A is late, only C_L needs to be charged.

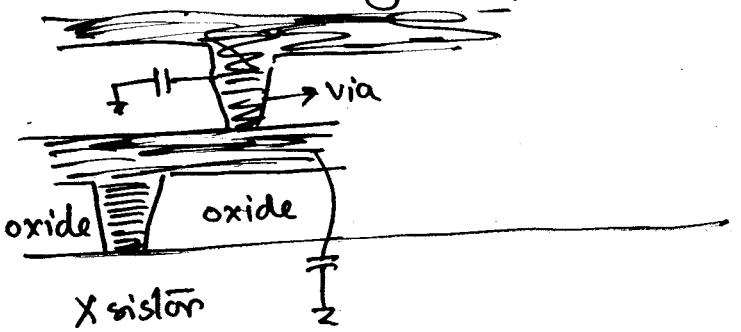
② B is late, both C_x and C_L need to be charged.

③ C is late, C_x, C_y and C_L need to be charged.

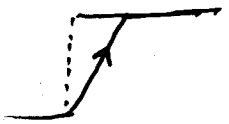


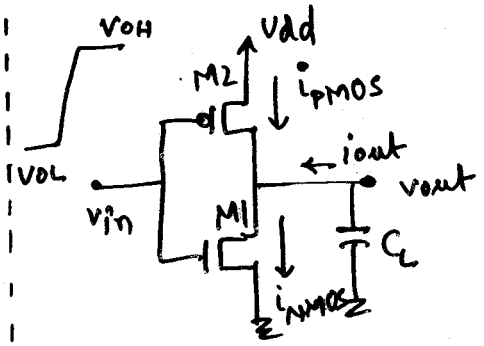
Wiring Capacitance

Cwire $\propto$ Length of the wire.



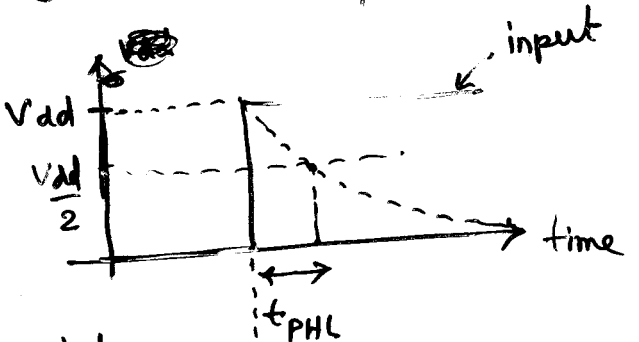
So far, all inputs → Ideal step inputs





Analytical Expressions

(1) Ideal step input.

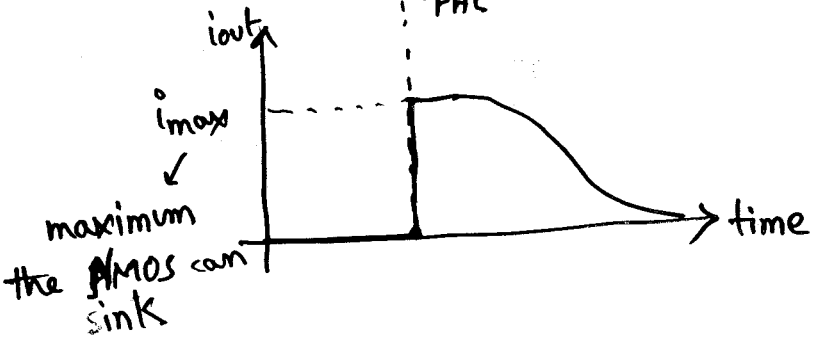


$$i = C\frac{dV}{dt}$$

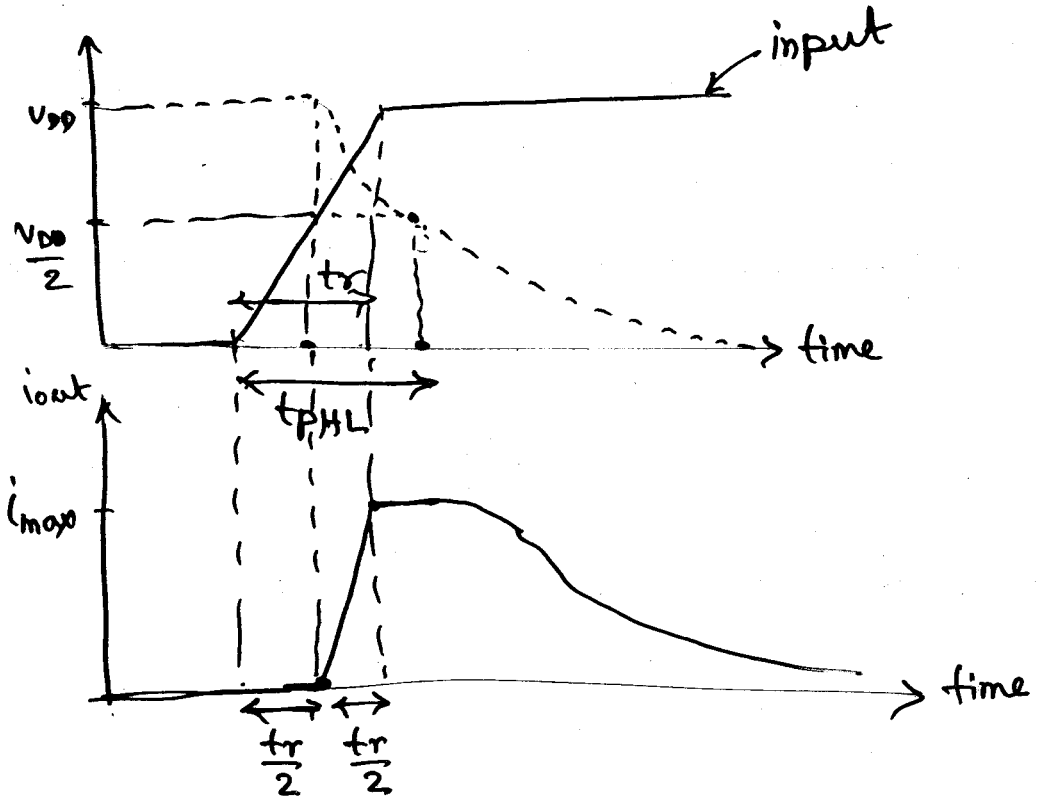
$$i_{max} = C_L \cdot \left(\frac{\Delta V}{\Delta t}\right)$$

$$= C_L \frac{(V_{DD}/2)}{t_{PHL}}$$

$$t_{PHL}(\text{step}) = \frac{C_L \cdot (V_{DD}/2)}{i_{max}}$$



Step with finite rise time



$$t_{PHL}(\text{ramp}) = \frac{t_r}{2} + t_{PHL}(\text{step})$$