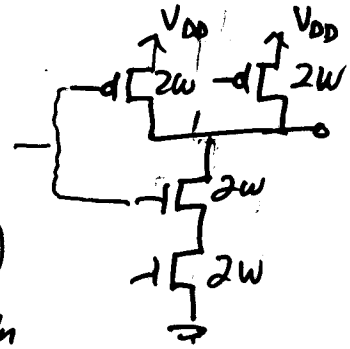
Exam #2 - Friday, March 11, 2005
Problem Session - Thursday, March 10, 2005 - 5pm - 6pm (C240)

Optimizing Logic Paths with NAND's, NOR's & Combinations

Inverter:

$$\text{Total delay} = \sum_j \tau_{inv}\left(\frac{C_{j+1}}{C_j} + \gamma_{inv}\right)$$

$$\tau_{inv} = 3 R_{eqn} C_g L_n$$



1.) NAND2

$$\text{Total delay} = \sum_j \tau_{nand}\left(\frac{C_{j+1}}{C_j} + \gamma_{nand}\right)$$

$$\tau_{nand} = R_{eff} C_{in} = R_{eqn}\left(\frac{L_n}{W_n}\right)(W_n + W_p) C_g = 4 R_{eqn} C_g L_n$$

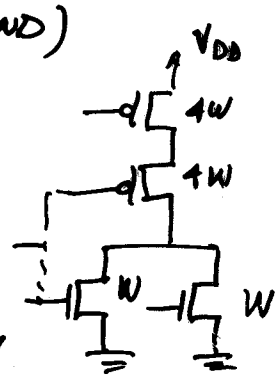
($4W_n$)

$f_{optimum} \simeq 4$ (Fig. 6.23 for NAND)

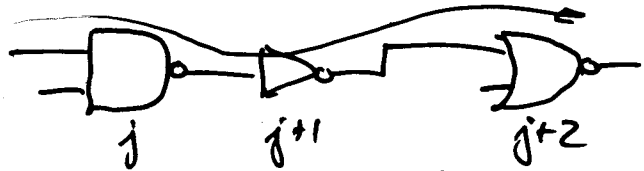
2.) NOR2

$$\text{Total delay} = \sum_j \tau_{nor}\left(\frac{C_{j+1}}{C_j} + \gamma_{nor}\right)$$

$$\tau_{nor} = R_{eqn}\left(\frac{L_n}{W_n}\right)(5W_n) C_g = 5 R_{eqn} C_g L_n$$



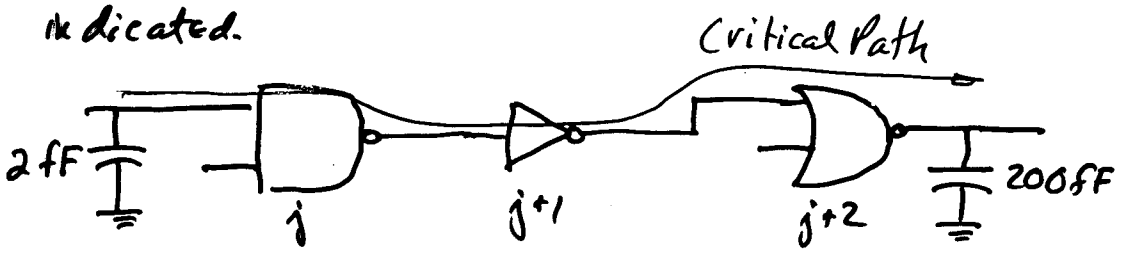
3.) Combinations of Gates



Delay is minimized when T·FO of a given gate is equal to the T·FO of the next gate, regardless of the type of gate.

Example of Computing the Optimal Gate Sizes along a Critical Path

Find the device sizes that optimize the delay thru the path indicated.



We know that

$$\tau_{nand} \times \left(\frac{C_{j+1}}{C_j}\right) = \tau_{nand}\left(\frac{C_{j+1}}{2fF}\right) = \tau_{inv}\left(\frac{C_{j+2}}{C_{j+1}}\right) = \tau_{nor}\left(\frac{200fF}{C_{j+2}}\right)$$

$$\text{Fanout-delay} = \sqrt[3]{\tau_{nand}\left(\frac{C_{j+1}}{2fF}\right)\tau_{inv}\left(\frac{C_{j+2}}{C_{j+1}}\right)\tau_{nor}\left(\frac{200fF}{C_{j+2}}\right)}$$

$$= \sqrt[3]{\tau_{nand}\cdot\tau_{inv}\cdot\tau_{nor}\left(\frac{200}{2}\right)} = \sqrt[3]{5\cdot 3\cdot 4\,(R_{eqn}C_gL_n)^3 100}$$

$$= 18.17\,R_{eqn}C_gL_n \approx 18.2\,R_{eqn}C_gL_n$$

C_{j+2}:

$$\tau_{nor}\left(\frac{C_{load}}{C_{j+2}}\right) = 5\,R_{eqn}C_gL_n\left(\frac{200}{C_{j+2}}\right) = 18.2\,R_{eqn}C_gL_n$$

$$C_{j+2} = \frac{5(200fF)}{18.2} = 55fF = 5W_nC_g$$

$$11fF = W_n\,2fF/\mu m \rightarrow W_n = \frac{11}{2}\,\mu m = 5.5\mu m$$

$$W_p = 4W_n = 22\mu m$$

C_{j+1}:

$$\tau_{inv}\left(\frac{C_{j+2}}{C_{j+1}}\right) = 3\,R_{eqn}C_gL_n\left(\frac{55}{C_{j+1}}\right) = 18.2\,R_{eqn}C_gL_n$$

$$C_{j+1} = \frac{3}{18.2}55fF = 9.1fF = 3W_nC_g \rightarrow W_n = 1.5\mu m$$

$$W_p = 3\mu m$$

C_{in}:

$$\tau_{nand}\left(\frac{C_{j+1}}{C_{in}}\right) = 4\,R_{eqn}L_n\left(\frac{9.1fF}{C_{in}}\right) = 18.2\,R_{eqn}L_n$$

$$C_{in} = \frac{4}{18.2} \times 9.1fF = 2fF = 4W_nC_g \rightarrow W_n = 0.25\mu m$$

$$W_p = 0.25\mu m$$

OPTIMIZING LOGIC DELAY PATHS WITH LOGICAL EFFORT

$$\text{Logical Effort} = LE = \frac{\text{Total delay}}{\tau_{inv}}$$

General path:

$$\frac{\text{Total Delay}}{\tau_{inv}} = \frac{\tau_{nand}}{\tau_{inv}}\left(\frac{C_{j+1}}{C_j} + \gamma_{nand}\right) + \frac{\tau_{inv}}{\tau_{inv}}\left(\frac{C_{j+2}}{C_{j+1}} + \gamma_{inv}\right) + \frac{\tau_{nor}}{\tau_{inv}}\left(\frac{C_{j+3}}{C_{j+2}} + \gamma_{nor}\right)$$

Normalized Total delay $= D = \frac{\tau_{nand}}{\tau_{inv}}\frac{C_{j+1}}{C_j} + \frac{\tau_{nand}}{\tau_{inv}}\gamma_{nand} + \cdots\cdots$

$$= \left[LE_{nand} \cdot FO_1 + P_{nand}\right] + \left[LE_{inv} \cdot FO_2 + P_{inv}\right] + \left[LE_{nor} \cdot FO_3 + P_{nor}\right]$$

where $LE_{gate} = \frac{\tau_{gate}}{\tau_{inv}}$, $FO_j = \frac{C_{j+1}}{C_j}$, & $P_{gate} = LE_{gate}\,\gamma_{gate}$

What are the LE_{gate}?

$\tau_{inv} = 3R_{eqn}C_g L_n$, $\tau_{nand_2} = 4R_{eqn}C_g L_n$, $\tau_{nor_2} = 5R_{eqn}C_g L_n$

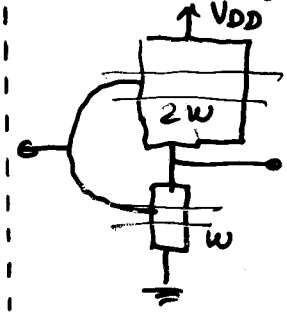
$LE_{inv} = 1$ $\quad LE_{nand_2} = \frac{4}{3}$ $\quad$ & $LE_{nor_2} = \frac{5}{3}$

For n-input gates → $LE_{nand} = \frac{n+2}{3}$ & $LE_{nor} = \frac{2n+1}{3}$

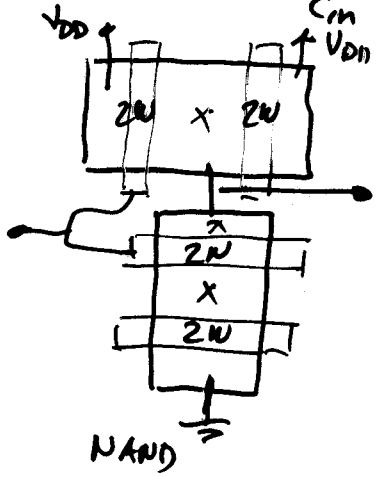
Table 6.1

Parasitic term, P:

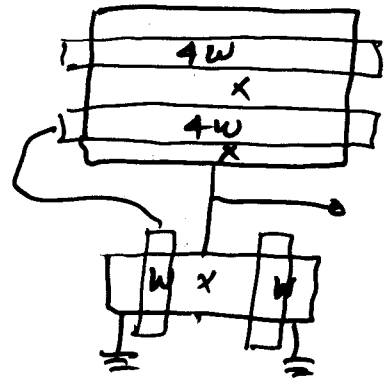
$P_{inv} = LE_{inv}\,\gamma_{inv} = LE_{inv}\,\frac{C_{self}}{C_{in}} = LE \times \frac{C_{eff}\cdot 3W}{C_g \cdot 3W} = LE\,\frac{C_{eff}}{C_g} = \frac{1}{2}$ (LE^{1}, $f^{\frac{1}{2}}$)



$$p_{nand} = LE_{nand} \times \frac{C_{self}}{C_{in}} = LE_{nand} \times \frac{C_{eff}(2W+2W+2W)}{C_g(2W+2W)} = \left(\frac{4}{3}\right)\left(\frac{1}{2}\right)\left(\frac{6}{4}\right) = 1$$



NAND



NOR

$$p_{nor} = LE_{nor\,2} \times \frac{C_{self}}{C_{in}} = LE_{nor} \times \frac{C_{eff}[W+4W+4W]}{C_g[W+4W]} = \frac{5}{3}\left(\frac{1}{2}\right)\left(\frac{9}{5}\right) = \frac{3}{2}$$

For n-input gates:

$p_{nand}(n\text{-inputs}) = \frac{n}{2}$ $\quad$ $p_{nor}(n\text{-inputs}) = \frac{3n}{4}$ (Table 6.2)

Next – Path Optimization of previous example using LE