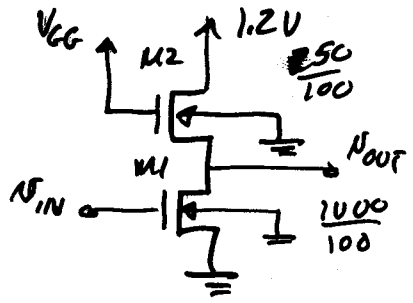
Exam #2 Solutions

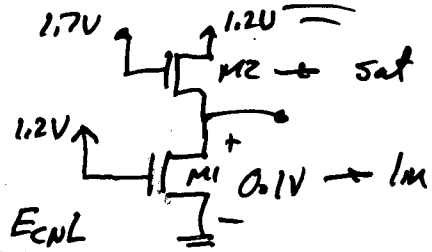
Problem 1



a.) $V_{TN2} = 0.5V$ instead $0.4V$

$V_{GG} = V_{TN2} + V_{OH} = 1.7V$

b.)

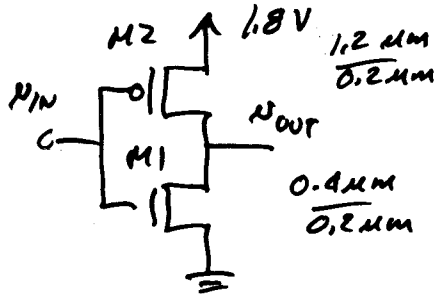


$$V_{DS}(sat) = \frac{(V_{GS} - V_{TN}) E_{CNL}}{V_{GS} - V_{TN} + E_{CNL}}$$

$V_{DS1}(sat) = 0.343V$ $\quad V_{DS2}(sat) = \underline{0.4V}$

c.) $I_{DS1}(lin) = \underline{278\mu A}$ $\quad I_{DS2}(sat) = \underline{256\mu A}$

Problem 2



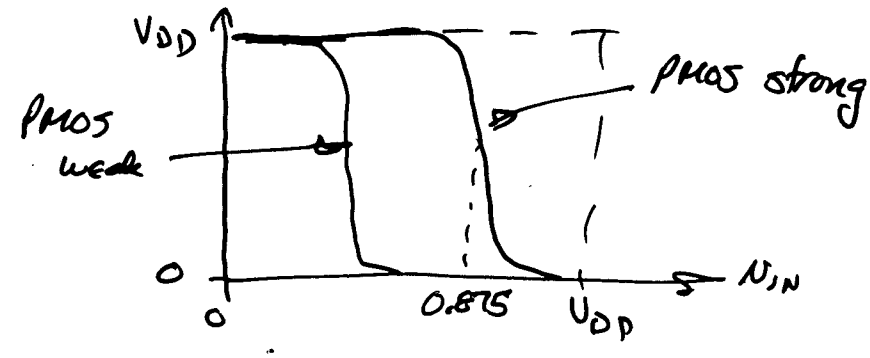
$\Rightarrow$

$$V_S = \frac{V_{DD} - |V_{TP}| + X V_{TN}}{1 + X}$$

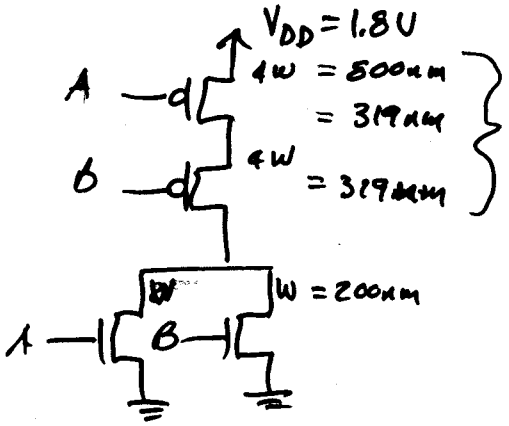
$$X = \sqrt{\frac{\mu_n W_n}{\mu_p W_p}} = 1.134$$

$V_S(1.8) = \underline{0.875V}$

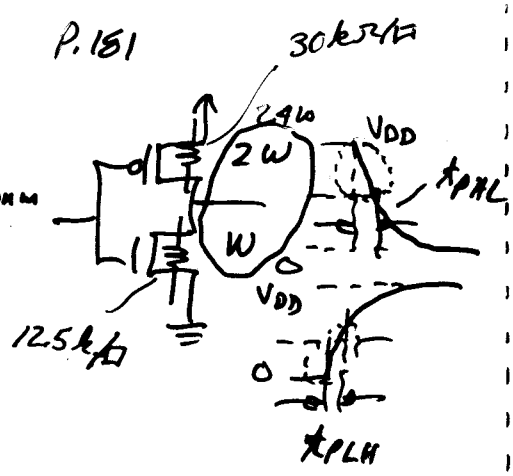
$V_S = \frac{1}{2} V_{DD} \rightarrow \sqrt{\frac{\mu_n W_n}{\mu_p W_p}} = 1 \rightarrow \frac{W_n}{W_p} = \frac{1}{4}$



Problem 3



P. 151



$\frac{200nm}{1.255} \times 160nm$

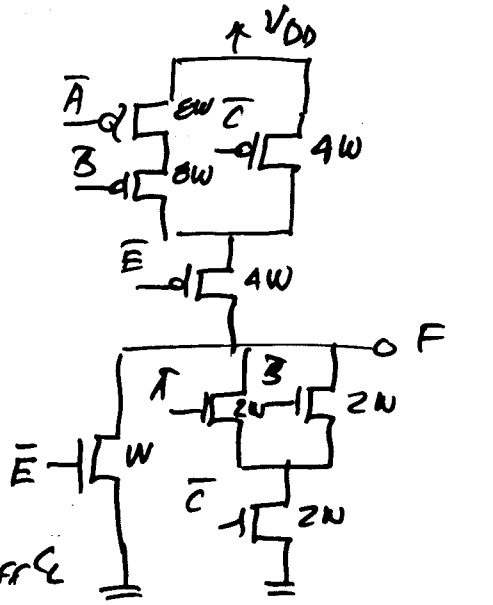
a.) $V_S = 0.75 \longrightarrow \chi = 2.2 \longrightarrow \chi = \sqrt{\frac{\mu_n W_n}{\mu_p W_p}}$

$\frac{W_n}{W_p} = 1.255$ $W_n = 200nm$

$\therefore W_p = \frac{}{1.255} \times 200nm \times 2 = 319nm$

b.) ---

Problem 4



nMOS:

$F = (AB+C)E$

$\bar{F} = (\bar{A}+\bar{B})\bar{C} + \bar{E}$

pMOS:

Dual of $\bar{F} = (A\bar{B}+\bar{C})\bar{E}$

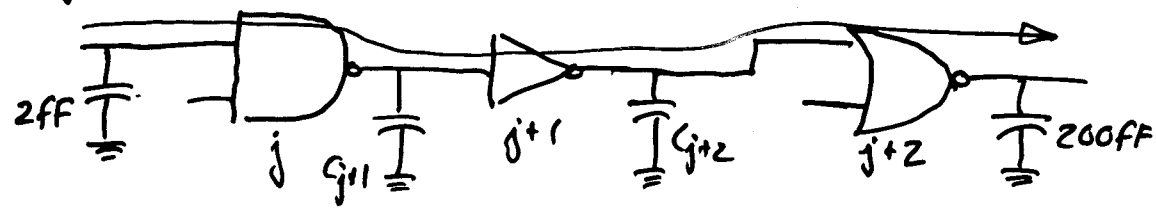
$t_{pHL} = t_{PLH} = 50ps = 0.7 R_{eff} C_L$

$(12.5k\Omega \frac{L_n}{nH})$

$W = 1750nm = \underline{1.75\mu m}$

Example of Computing the Optimal Gate Sizes along a Critical Path

Find the devices that optimize the delay thru the path below using logical effort concepts.



First, equalize the LE×FO components of the delay for all gates.

$$\text{Total path effort} = \underbrace{LE_{nand2}\left(\frac{C_{j+1}}{2ff}\right)}\underbrace{LE_{inv}\left(\frac{C_{j+2}}{C_{j+1}}\right)}LE_{nor2}\left(\frac{200ff}{C_{j+2}}\right)$$

$$= LE_{nand2}\,LE_{inv}\,LE_{nor2}\left(\frac{200}{2}\right) = \left(\frac{4}{3}\right)\left(1\right)\left(\frac{5}{3}\right)(100)$$

$$= 222.2$$

$$\text{Stage} = (222.2)^{1/3} = \underbrace{}_{f} = LE_{gate}\,FO_{gate}$$

$$\text{Normalized Delay} = D = \underbrace{\left(LE_{nand2}\cdot FO + p_{nand2}\right)} + \underbrace{\left(LE_{inv}\cdot FO + p_{inv}\right)}$$
$$+ \left(LE_{nor2}\cdot FO + p_{nor2}\right)$$

$$D = (f + p_{nand2}) + (f + p_{inv}) + (f + p_{nor2}) = 18 + \sum p_j$$

$$D = 18 + 1 + \frac{1}{2} + \frac{5}{2} = 21$$

Minimum path delay $= 21\,\tau_{inv} = 21 \times 7.5ps = 157.5ps$

Working backwards we can size the gates –

$LE_{nor2}\left(\frac{C_{out}}{C_{j+2}}\right) = 6 \rightarrow C_{j+2} = \frac{5}{3} \times \frac{200ff}{6} = 55ff \rightarrow$ $W_n = 55\mu m$, $W_p = 22\mu m$

$LE_{inv}\left(\frac{C_{j+2}}{C_{j+1}}\right) = 6 \rightarrow C_{j+1} = 1 \times \frac{55ff}{6} = 9.1ff \rightarrow$ $W_n = 1.5\mu m$, $W_p = 3\mu m$

$LE_{nand2}\left(\frac{C_{j+1}}{C_{in}}\right) = 6 \rightarrow C_{in} = \frac{4}{3}\,\frac{9.1ff}{6} = 2ff \rightarrow$ $W_n = 0.5\mu m$, $W_p = 0.5\mu m$