Example of Path Optimization on Fig. 5.8

(a.) Nand4 - Inv - Nand2 - Inv — $C_{in} = 20ff$ & $C_L = 200ff$

$$D = 4(\text{Path effort})^{1/4} + \sum p = 4\left[\left(\tfrac{6}{3}\right)(1)\left(\tfrac{4}{3}\right)(1)\right]^{1/4} + \left[2+\tfrac{1}{2}+1+\tfrac{1}{2}\right]$$

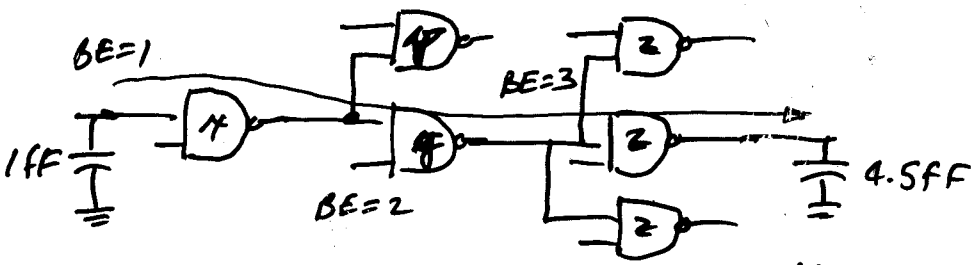
$$= 9+4 = 13$$

(b.) Nand2 - Nor2 - Nand2 - Inv:

$$D = 4\left[\left(\tfrac{4}{3}\right)\left(\tfrac{5}{3}\right)\left(\tfrac{4}{3}\right)(1)\right]^{1/4} + \left[1+\tfrac{3}{2}+1+\tfrac{1}{2}\right] = 13.33$$

(a.) is faster than (b.)

Branching Effort and Sideloads



For similar branches, we write that,

$$\text{Total path effort} = \Pi(LE \times FO \times BE) = \Pi(LE \times BE) \times \frac{C_{load}}{C_{in}}$$

BE = branching factor (no. of similar branches)

Example:

Select the gate sizes, x, y & z to minimize the delay in the path shown above.

$$\text{Logical Effort} = LE_p = \left(\tfrac{4}{3}\right)^3 = 2.37$$

$$\text{Electrical Effort} = FO_p = \frac{C_{load}}{C_{in}} = 4.5$$

$$\text{Branching Effort} = BE_p = (2)(3) = 6$$

$$\text{Path effort} = PE = (LE_p)(FO_p)(BE_p) = 64$$

$$\text{Optimal stage effort} = SE^* = (PE)^{1/3} = 4$$ ← Geometric Mean

Example - Cont'd

$$\text{Delay} = D = N(SE^*) + \text{Parasitics} = 3(4) + 3(1) = 15$$

Using $(LE_j)(BE_j)\left(\frac{C_{j+1}}{C_j}\right) = 4$ → Solve C_z, C_y, C_x

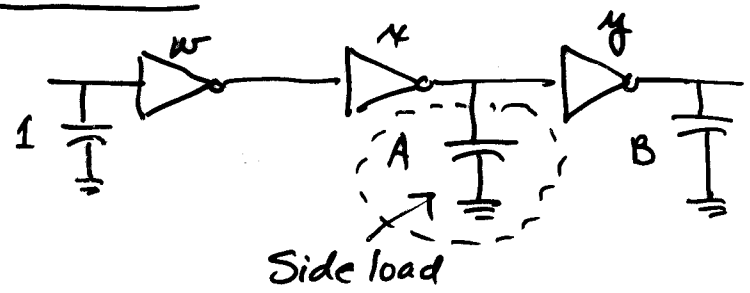
z:
$$\left(\frac{4}{3}\right)(1)\left(\frac{4.5fF}{C_z}\right) = 4 \rightarrow C_z = \left(\frac{4}{3}\right)\left(\frac{4.5fF}{4}\right) = 1.5fF$$

y:
$$\left(\frac{4}{3}\right)(3)\left(\frac{1.5fF}{C_y}\right) = 4 \rightarrow C_y = \left(\frac{4}{3}\right)(3)\left(\frac{1.5fF}{4}\right) = 1.5fF$$

x:
$$\left(\frac{4}{3}\right)(2)\left(\frac{1.5fF}{C_x}\right) = 4 \rightarrow C_x = \left(\frac{4}{3}\right)(2)\left(\frac{1.5fF}{4}\right) = 1fF$$

Rest example follows previous examples.

Side loads



Approach:

1.) Solve w/o the sideload

2.) Add the sideload and remove the gates beyond the sideload but including their load effects.

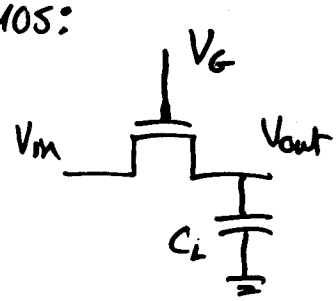
3.) Solve the sub problem and combine the two solutions

Ex. 6.16

CHAPTER 7 - TRANSFER GATE AND DYNAMIC LOGIC DESIGN

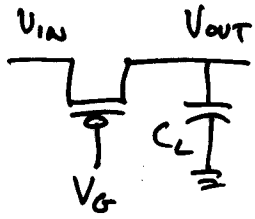
Pass Transistors (switches)

NMOS:



V_G	V_{IN}	V_{OUT}
0	0	Hi z
0	V_{DD}	Hi z
V_{DD}	0	0
V_{DD}	V_{DD}	$V_{DD}-V_{TN}$

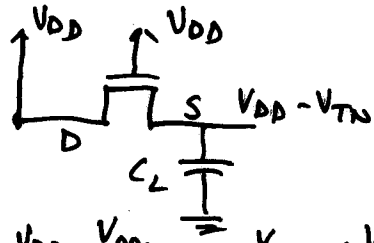
PMOS:



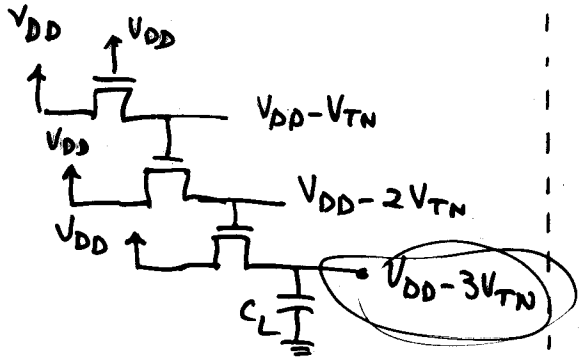
V_G	V_{IN}	V_{OUT}
0	0	$\|V_{TP}\|$
0	V_{DD}	V_{DD}
V_{DD}	0	Hi z
V_{DD}	V_{DD}	Hi z

Three Examples:

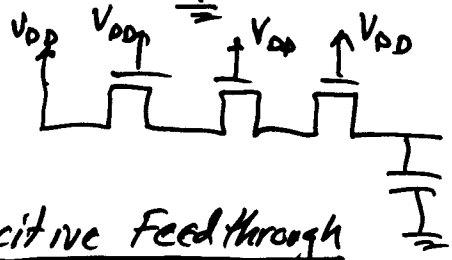
1.)



2.)



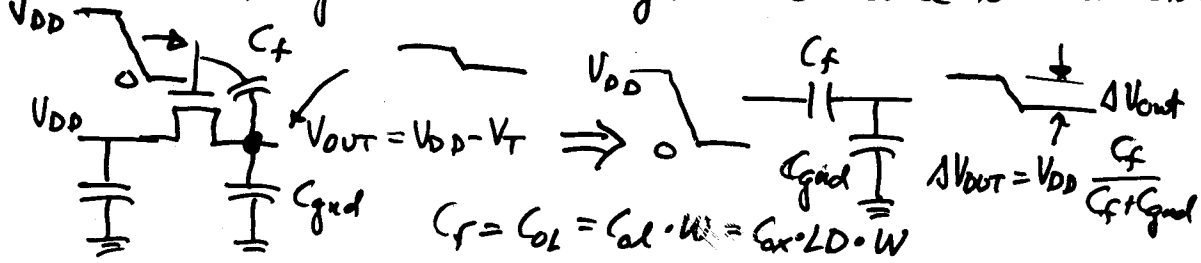
3.)



(All ignore bulk effects)

Capacitive Feedthrough

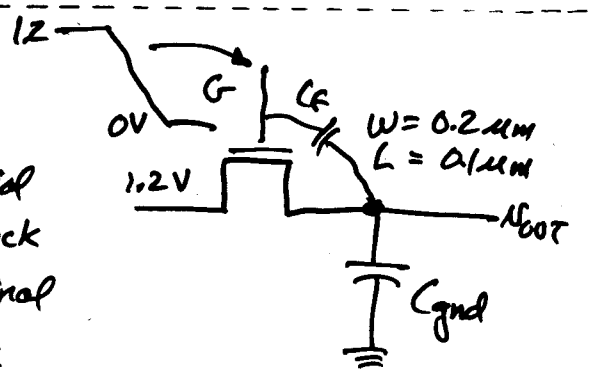
Capacitive feedthru (clock feedthru) occurs when the clock on the gate is switching the MOS device to the hi z state



$C_f = C_{OL} = C_{ol} \cdot W = C_{ox} \cdot LD \cdot W$

Example of Feedthru

In the circuit shown with the input at 1.2V, what is the initial value of the output when the clock (gate) is 1.2V. Estimate the final value at the output after clock goes low. Use 0.13μm technology.



Solution

$$V_{TN} = 0.4 + 0.2\sqrt{0.88 + V_{OUT}} - 0.2\sqrt{V_{out}}$$

but $V_{OUT} = 1.2 - V_{TN}$

} Iterate to get $V_{TN} = 0.483V$

∴ V_{out} (initial) = 0.72 V

To be continued