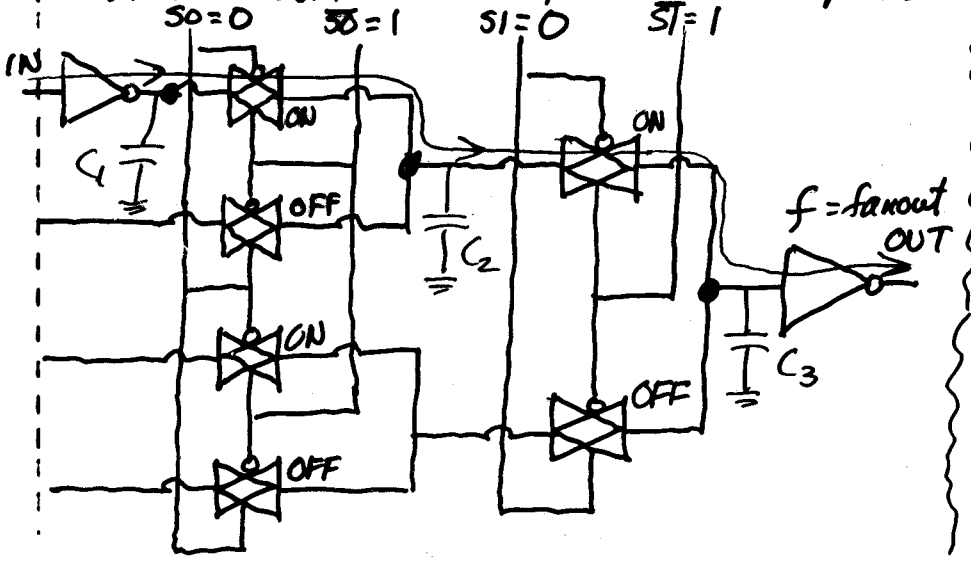
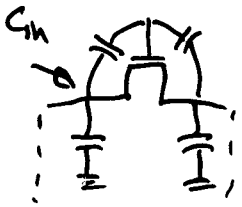
Example 7.4

Find the Elmore delay for the path shown where the fanout of the invert at the output of the multiplexer is f.



Review of TG Capacitances:



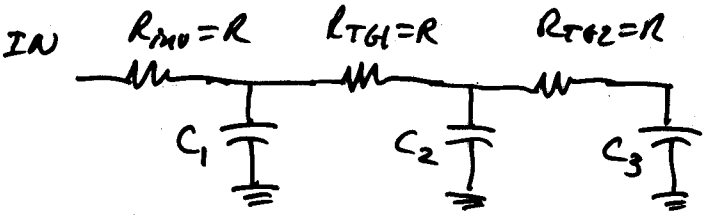
OFF:

$C_{in} = 2WC_{eff}$

ON:

$C_{in} = 2WC_{eff} + C_g W$

RC equivalent:



$$\text{Elmore Delay} = R_{inv} C_1 + (R_{INV} + R_{TG1}) C_2 + (R_{INV} + R_{TG1} + R_{TG2}) C_3$$

$$C_1 = 3WC_{eff} + WC_g + 2C_{eff}W = (5C_{eff} + C_g)W$$

$$C_2 = 6WC_{eff} + 2C_g W$$

$$C_3 = 3WC_g f + 4WC_{eff} + C_g$$

$$\text{Elmore Delay} = RW\left[(5C_{eff} + C_g) + 2(6C_{eff} + 2C_g) + 3(3C_g f + C_g + 4C_{eff})\right]$$

$$= WR\left[29C_{eff} + 8C_g + 9fC_g\right]$$

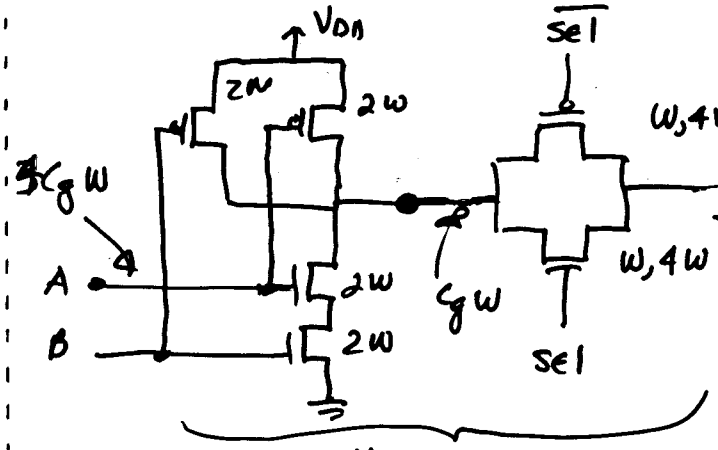
Logical Effort for a Transmission Gate

Recall that $LE = \frac{\tau_{gate}}{\tau_{inv}} = \frac{\tau_{gate}}{3RWC_g}$

τ = (Pull resistance of gate)(Input C of gate)

Example 7.5

Compute the LE_A and LE_{sel} for the NAND gate shown which drives a TG with a width W and 4W.

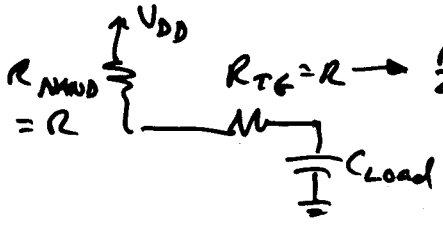


Width of TG = W

$$LE_A = \frac{\tau_{gate}}{3WC_gR} = \frac{4WC_g(2R)}{3WC_gR} = \frac{8}{3}$$

$$LE_{sel} = \frac{WC_g(2R)}{3WC_gR} = \frac{2}{3}$$

Width of TG = 4W



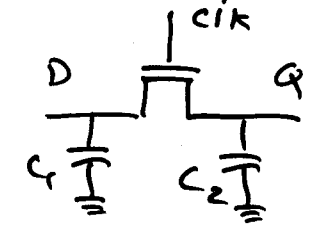
$$LE_A = \frac{4WC_g\left(\frac{5}{4}R\right)}{3WC_gR} = \frac{5}{3}$$

$$LE_{sel} = \frac{4WC_g\left(\frac{5}{4}R\right)}{3WC_gR} = \frac{5}{3}$$

DYNAMIC D-LATCHES AND D-FLIP-FLOPS

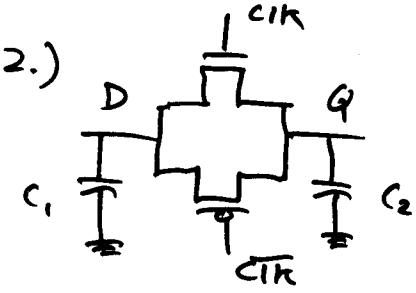
Evolution of Simple D-Latches using TG's —

1.)



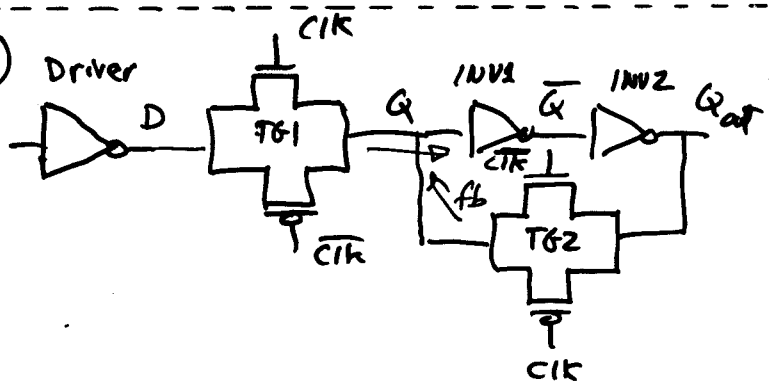
Problems: Propagation of V_{DD}
Clock feedthrough
No $\bar{Q}$ available
Output becomes hi-Z when the clock is low.

2.)



Solves:
Propagation of V_{DD}
Helps to reduce clock feedthrough

3.) Driver

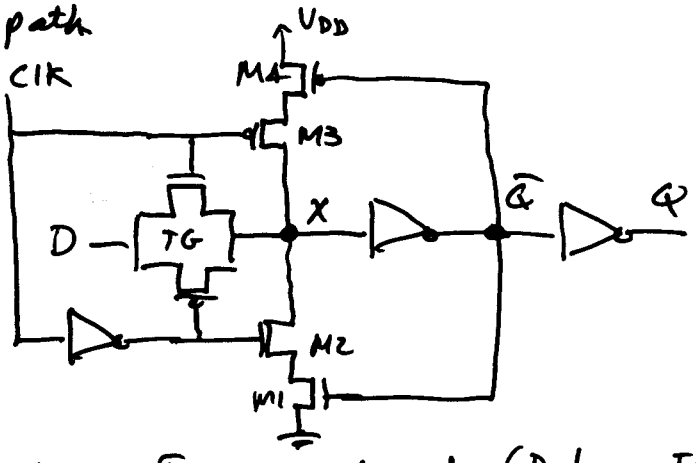


New problem: When the clk goes high, the delay before $\overline{clk}$ goes low can cause a conflict at Q between TG1 & TG2

Solution:

a.) Size INV2, TG2 and TG1 and the driving gate D so that the forward path is stronger than the feedback path

b.)



CLK=1: Transparent mode (Delay = TG + 2 INV)

If D=0 → $\bar{Q}$=1 (M1=ON, M2=OFF, M3=OFF, M4=OFF)

If D=1 → $\bar{Q}$=0 (M1=OFF, M2=OFF, M3=OFF, M4=ON)

CLK=0 Latch Mode

If D=1 → $\bar{Q}$=0 (M1=OFF, M2=ON, M3=ON, M4=ON)

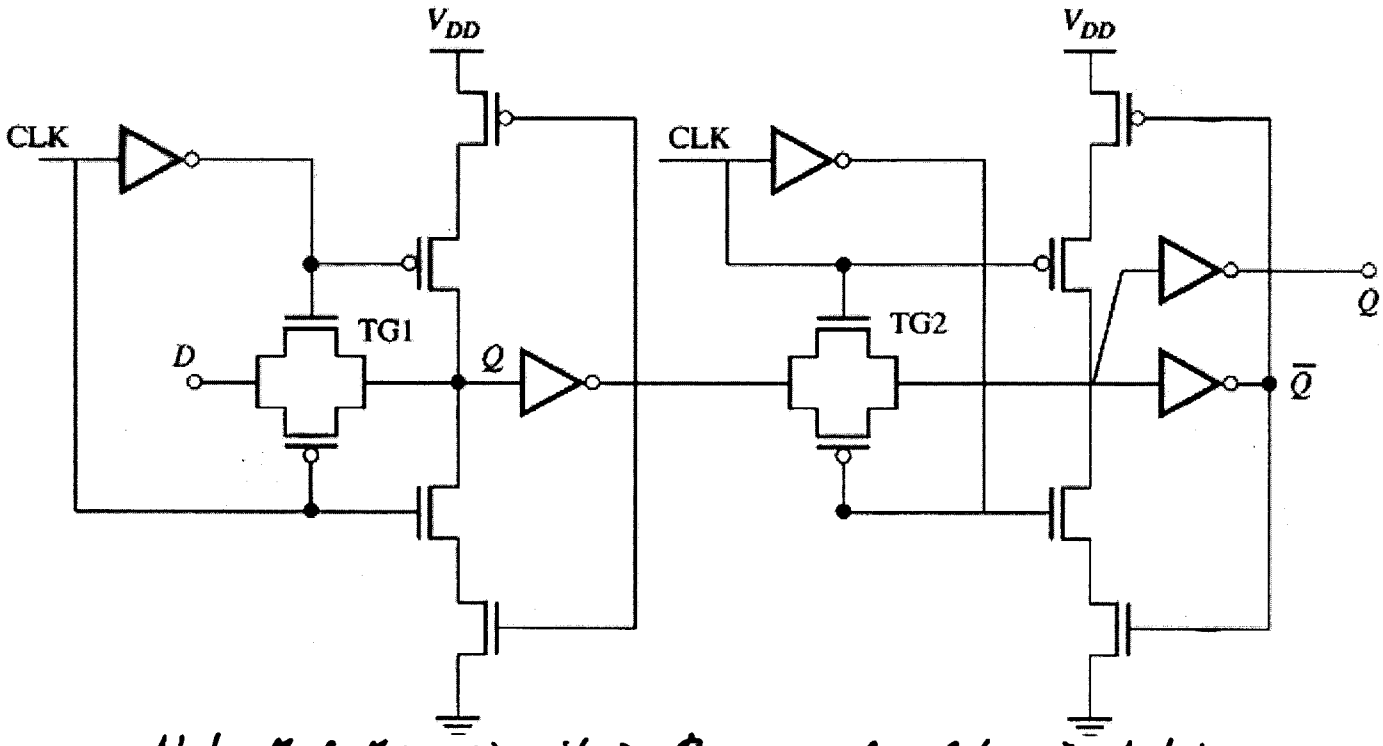
If D=0 → $\bar{Q}$=1 (M1=ON, M2=ON, M3=ON, M4=OFF)

Master-Slave D Flip-Flops

(See slide)

3/30/05

Figure 7.24 – Positive edge-triggered D-type flip-flop



Note that this circuit is the cascade of two D-Latches

The positive edge of the Clk shuts off the first latch and enables the second.

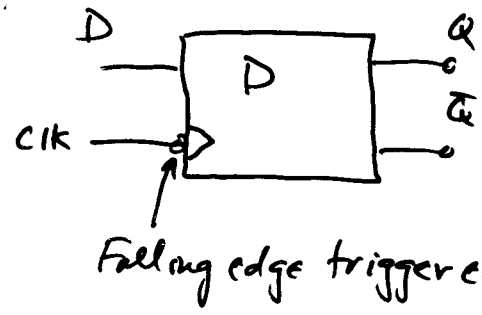
Clk = 0 :

1st latch is transparent
2nd latch is disabled

Clk = 1 :

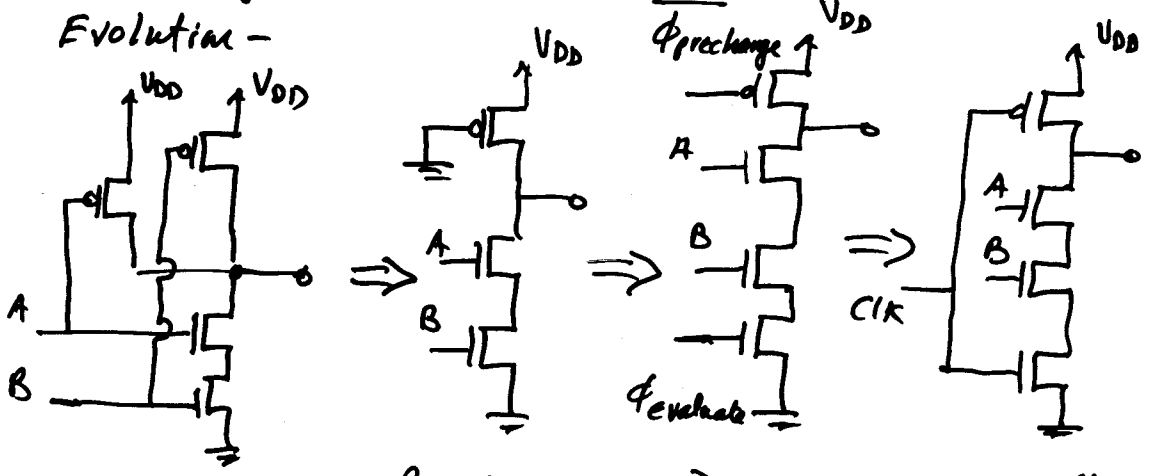
TG1 shuts off and holds D at its output (1st latch)
TG2 allows Q to flow to the output

Since D is only transmitted to the output on the rising edge of the clock, this flip-flop is called edge triggered.



Domino Logic

Evolution –



CMOS Pseudo-NMOS Dynamic Single-Clock Dynamic

3-input dynamic NOR gate next —