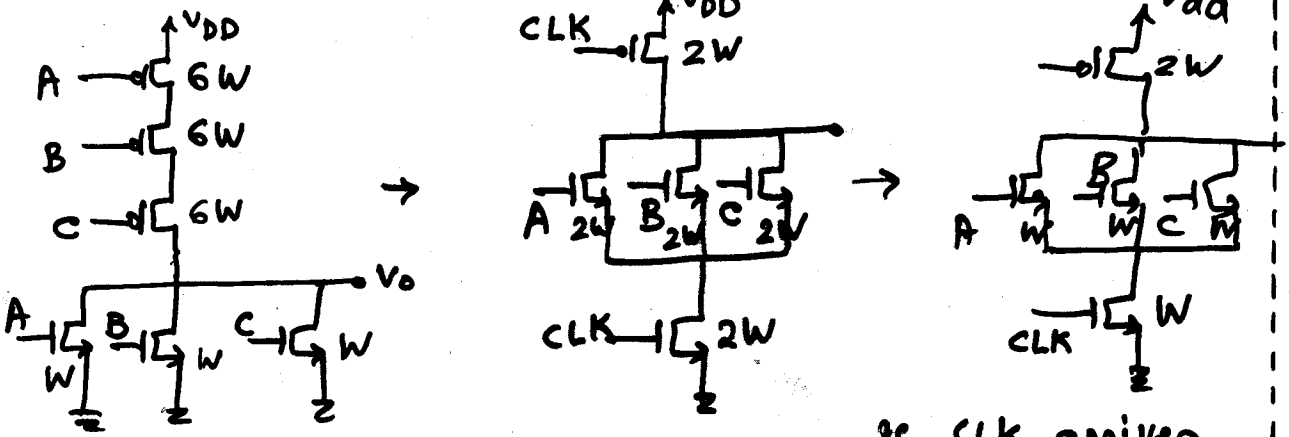
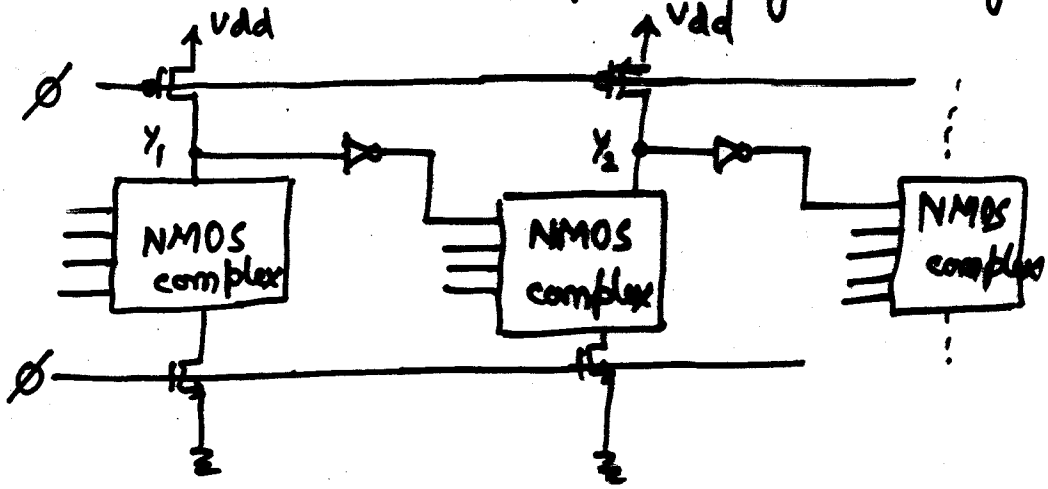
3 input Dynamic NOR Gate

Static



If CLK arrives before A, B, C.

General structure of a dynamic gate



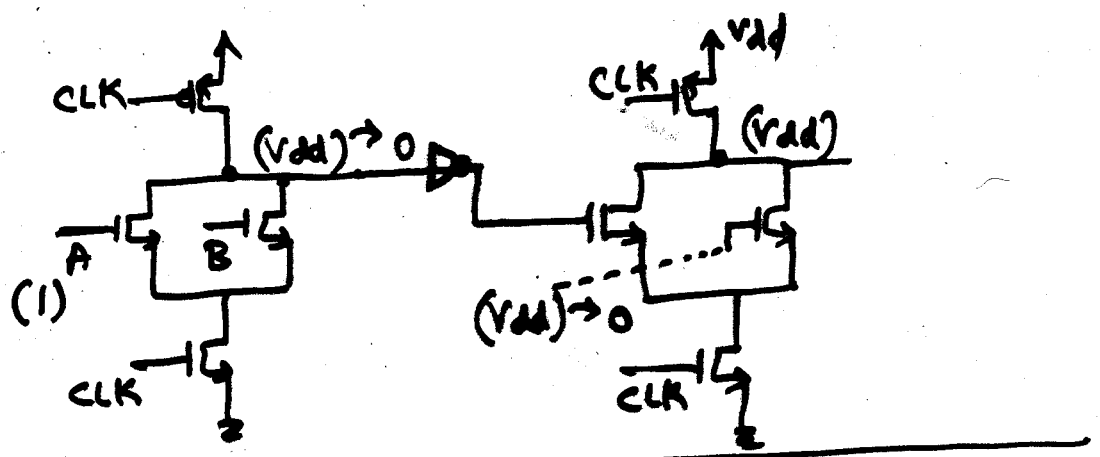
Domino Logic – some observations

1) Since the output is already high, we can speed up the gate by increasing the sizes of NMOS transistors.

2) Since there is no pull up fighting the pull down → switch faster.

3) Power savings.

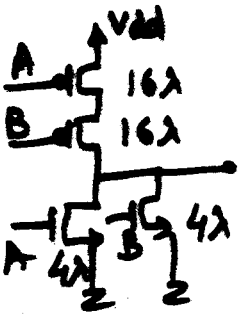
4) Domino logic → only implement non-inverting logic function.



Logic Effort for Domino Logic

NOR2

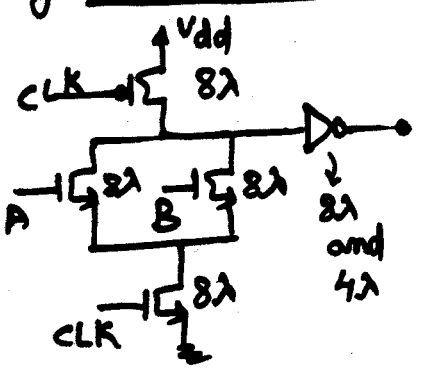
Static



$L = 2\lambda$

$$LE_{NOR} = \frac{\text{NOR input cap.}}{\text{INV input cap}} = \frac{16\lambda + 4\lambda}{8\lambda + 4\lambda} = \frac{5}{3} = 1.67$$

Dynamic NOR2



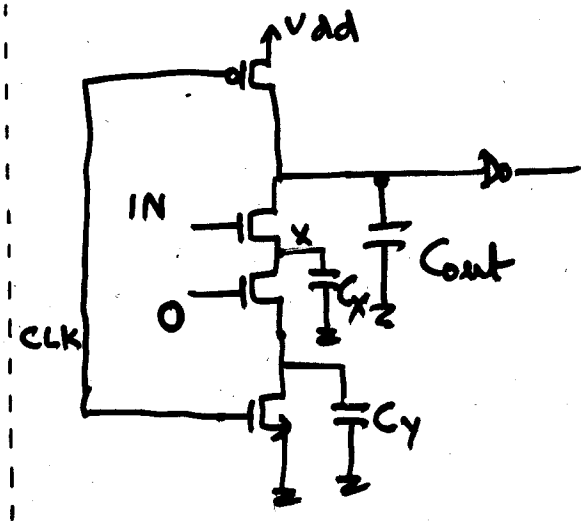
$$LE_{Dyn.NOR} = \frac{8\lambda}{12\lambda} = \frac{2}{3}$$

$$LE_{INV} = 1$$

$$LE_{Domino} = \sqrt{(LE_{Dyn.NOR})(LE_{INV})} = 0.8$$

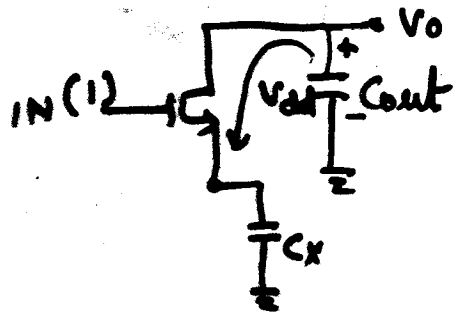
Limitations of Domino Logic

① Charge sharing.



① Precharge Cout to V_{DD}

② IN → goes from 0 to 1.
and CLK → 1.



$$V_o = \left\{ \frac{C_{out}}{C_x + C_{out}} \right\} V_{DD}$$

If, $C_x = C_{out}$, $V_o = \frac{V_{DD}}{2}$

Solutions

1) Increase Cout → Speed ↓↓
2) Precharge X to V_{DD}.
3) Use Keepers.