Dynamic NOR Gate

Static

General structure of a dynamic gate

Domino Logic - some observations

1) Since the output is already high, we can speed up the gate by increasing the sizes of NMOS transistors.
2) Since there is no pull up fighting the pull down → switch faster.

3) Power savings.

4) Domino logic → only implement non-inverting logic function.

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Logic Effort for Domino Logic

\[ \text{NOR2} \]

\[ \text{Static} \quad \frac{A}{B} = 16\lambda \]

\[ L = 2\lambda \]

\[ \text{LE}_{\text{NOR}} = \frac{\text{NOR input cap.}}{2\text{INV input cap}} \]

\[ = \frac{16\lambda + 4\lambda}{8\lambda + 4\lambda} = \frac{5}{3} \]

\[ = 1.67 \]

\[ \text{Dynamic} \quad \text{NOR2} \]

\[ \text{LE}_{\text{Dyn-NOR}} = \frac{8\lambda}{12\lambda} = \frac{2}{3} \]

\[ \text{LE}_{\text{INV}} = 1 \]

\[ \text{LE}_{\text{Domino}} = \sqrt{\text{LE}_{\text{Dyn-NOR}} \cdot \text{LE}_{\text{INV}}} \]

\[ = 0.8 \]
**Limitations of Domino Logic**

1. Change sharing.

   ![Domino Circuit Diagram]

   ① Precharge Cout to $V_{DD}$
   ② $IN$ goes from 0 to 1, and $CLK$ → 1.

   $$V_0 = \left\{ \frac{C_{out}}{C_X + C_{out}} \right\} V_{DD}$$

   If $C_X = C_{out}$, $V_0 = \frac{V_{DD}}{2}$

**Solutions**

1. Increase $C_{out}$ → Speed up
2. Precharge $X$ to $V_{DD}$
3. Use Keepers.