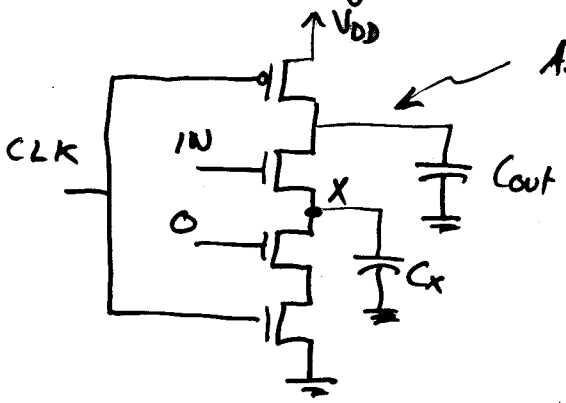
Limitations of Domino Logic

1.) Charge sharing



As IN goes from 0 to 1, $N_{out} \approx \frac{C_{out}}{C_x + C_{out}} V_{DD}$

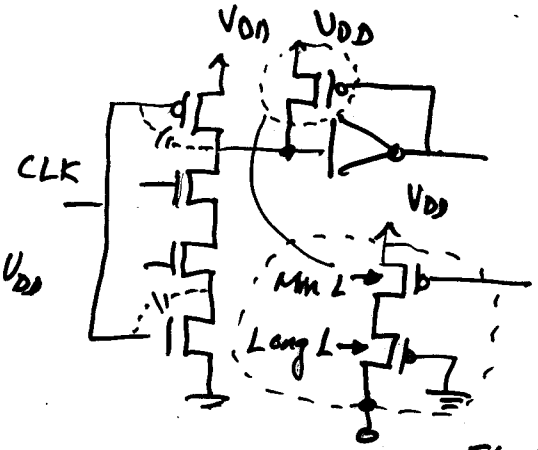
If $C_x = C_{out}$, then $N_{out} = \frac{V_{DD}}{2}$

Solutions:

1.) Increase C_{out}

2) Precharge node X to V_{DD}

3.) Use keepers

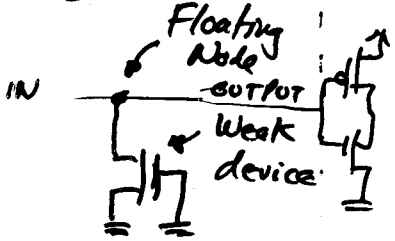


2) Leakage

Solutions:

1.) Increase the size of capacitors

2) Use keepers (passive biasing)



3.) Clock feedthrough from the clk.

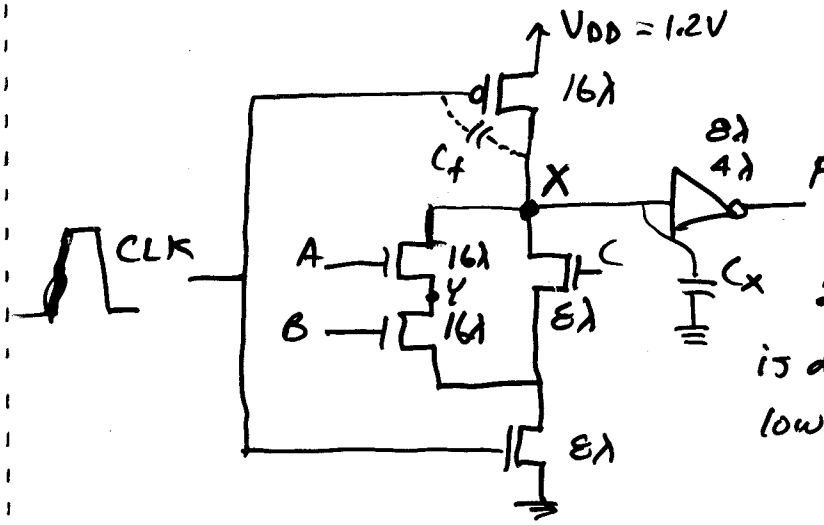
Example 7.8

For the domino logic function shown, assume 0.13 μm technology and find:

1.) What logic function does the gate perform?

2.) How much clock feedthru is observed at node X.

3.) What is the worst-case charge sharing at node X.



Solutions

1.) $F = AB + C$ (noninverting logic)

2.) The clock feedthru is due to the clock going from low to high

PMOS (linear): $C_f = C_{gd} = \frac{C_g W_p}{2} = \frac{(2fF/\mu m)(16\lambda)(0.05\frac{\mu m}{\lambda})}{2}$

$= 0.8fF$

Capacitance to ground from node X:

$C_x = C_{eff}(16\lambda + 16\lambda + 8\lambda) + C_g(8\lambda + 4\lambda)$

$= 1fF/\mu m\,(40\lambda)(0.05\frac{\mu m}{\lambda}) + 2fF/\mu m\,(12\lambda)(0.05\frac{\mu m}{\lambda}) = 3.2fF$

$\therefore \Delta V_x = \frac{C_f}{C_f + C_x}\Delta V_{clk} = \frac{0.8}{0.8+3.2}(1.2) = \underline{0.24\,V}$

3.) What is the worst case sharing at node X?

The worst case charge sharing occurs for the output at 1.2V, and A=1, B=C=0.

$C_y = (1fF/\mu m)(16\lambda)(0.05\frac{\mu m}{\lambda}) = 0.8fF$

Charge sharing between X & Y:

$V^* = \frac{C_x(1.2V)}{C_x + C_y} = \frac{3.2(1.2V)}{3.2+0.8} = 0.96\,V$

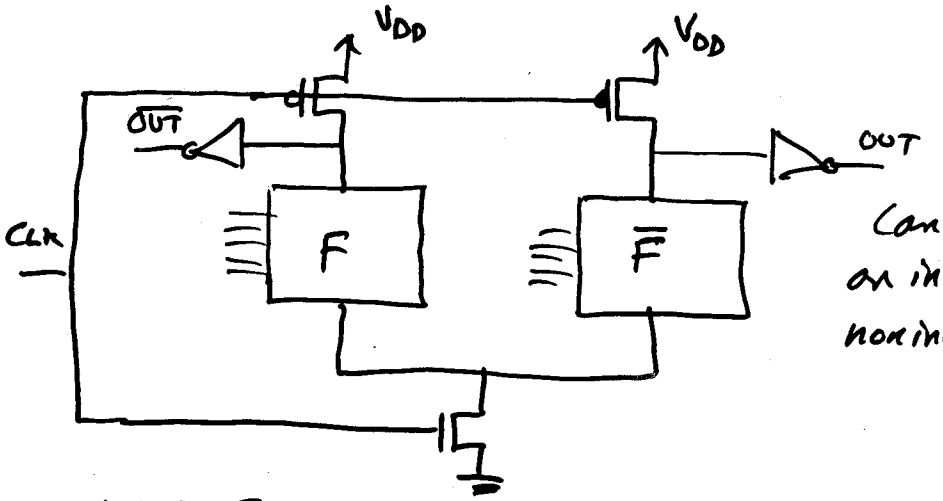
But the maximum voltage at node Y is $V_{DD} - V_{TN} = 1.2 - 0.4 = \underline{0.8\,V}$

The rest of the charge is at node X

$\therefore (3.2fF)(1.2V) - (0.8ff)(0.8V) = 3.84fC - 0.64fC = 3.2fC$

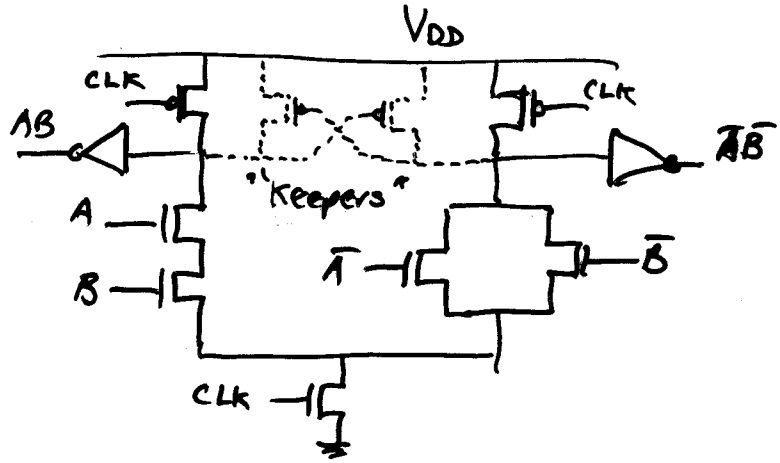
$3.2fC = 3.2fF\,V_x \rightarrow \underline{V_x = 1V}$

Dual-Rail (Differential) Domino Logic

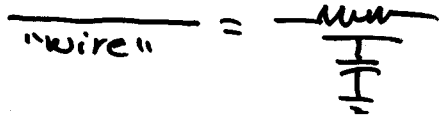


Can achieve both an inverting and noninverting logic

NAND2 Example



Chapter 8 - Semiconductor Memory Design
Chapter 10 - Interconnect Design



CHAPTER 8 - SEMICONDUCTOR MEMORY DESIGN

Memory Classification