SEMICONDUCTOR MEMORY DESIGN - CONT'D

Introduction -

- Memories are circuits or systems that store digital information in large quantities.
- 100 bits < Size of memories < 1GB
- Units of size -

  Bit = Digital "1" or "0" (flip-flop or similar ckt.)

  Byte = 8 bits (a single alphanumeric character)

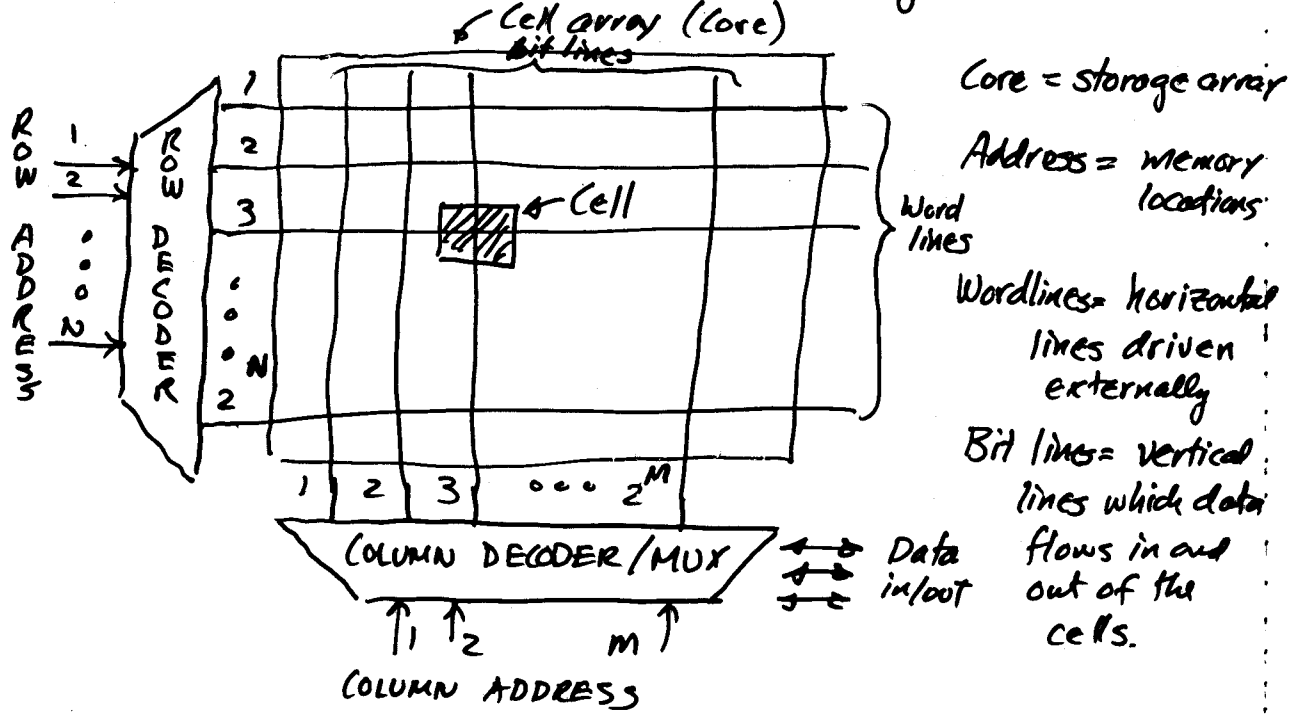
  Word = 32 to 128 bits

  "K" = 2^{10} = 1024

  "M" = 2^{20} = 1,048,576

Memory Organization

- Non-random access - FIFO, LIFO, shift registers, etc.
- Random access - memory locations can be accessed in a random or fixed order independent of the physical location for the purpose of reading & writing.



Core = storage array

Address = memory locations

Wordlines = horizontal lines driven externally

Bit lines = vertical lines which data flows in and out of the cells.

Overall Architecture of a 64Kb RAM

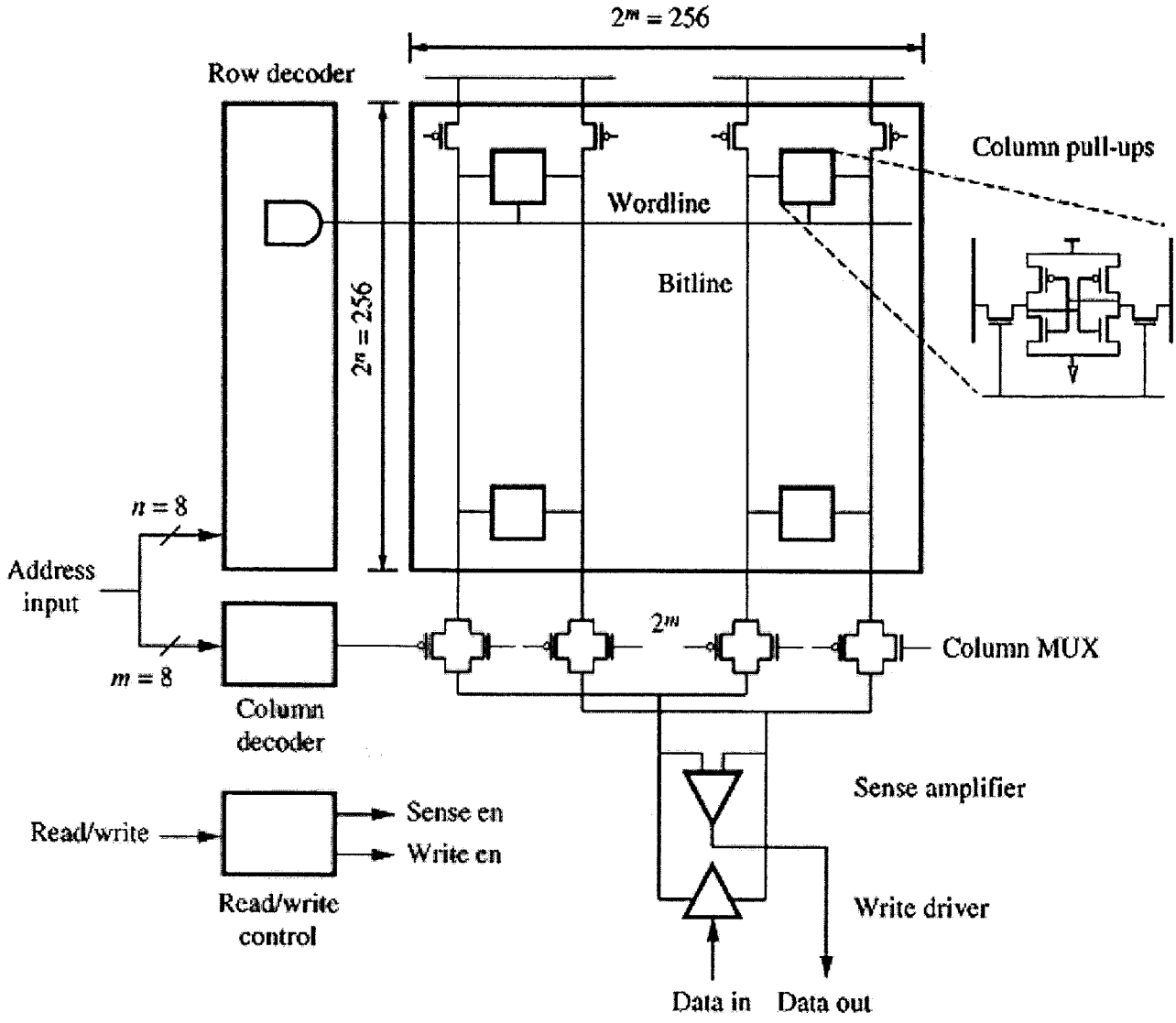
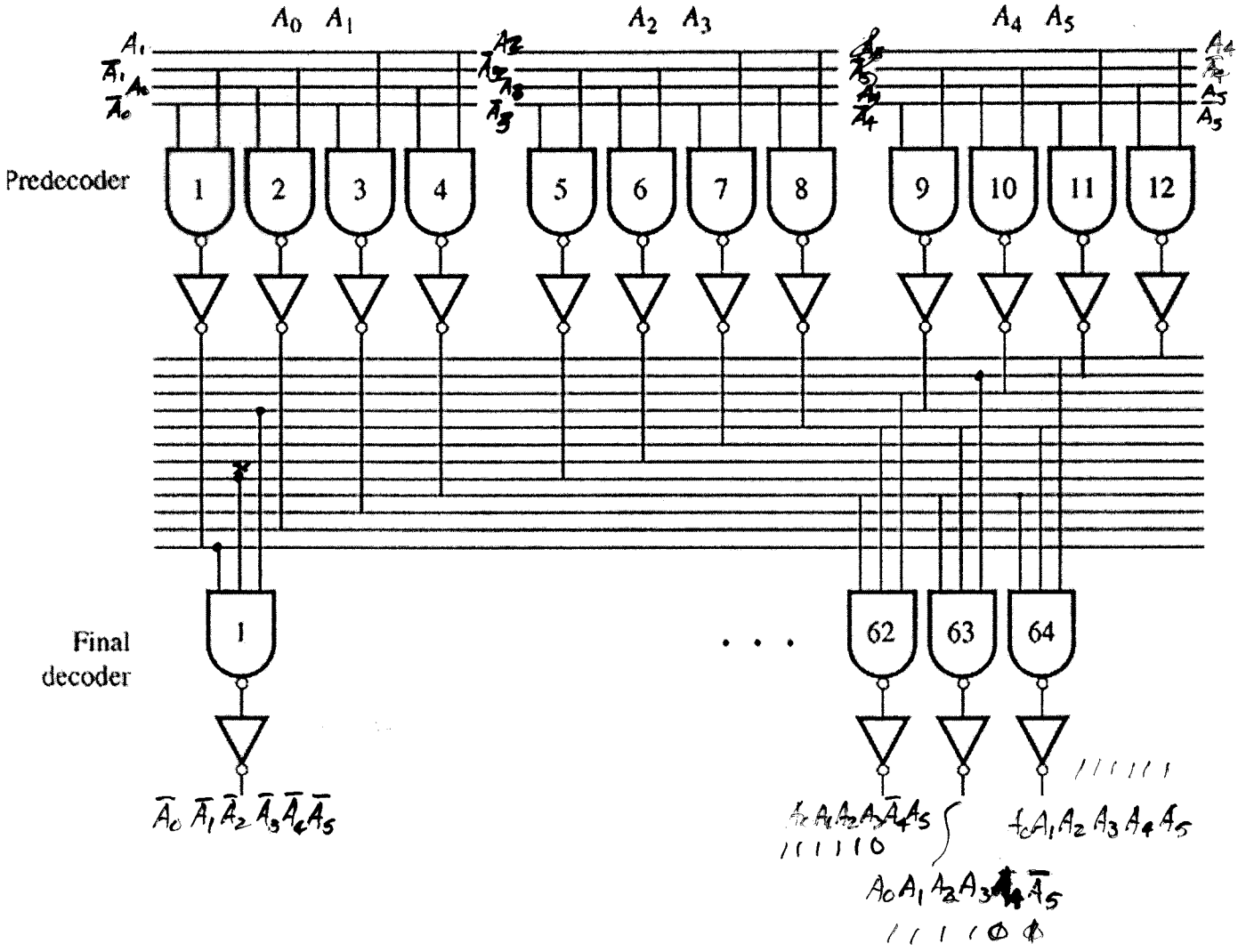
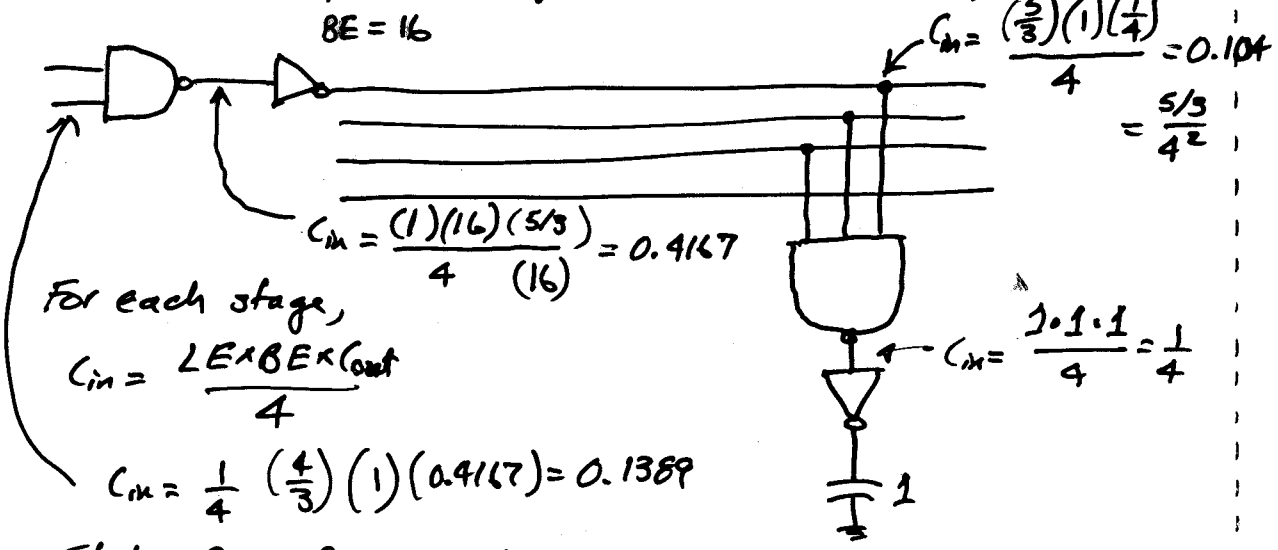


Figure 8.6 – Structure of two-level decoder for 6-bit address



Example 8.1 – Decoder Sizing using LE Techniques

Size the decoder on the previous slide using FO4 rules assuming the the normalized output loading is 1. (FO4 rules imply that the optimal stage effort is equal to 4.)



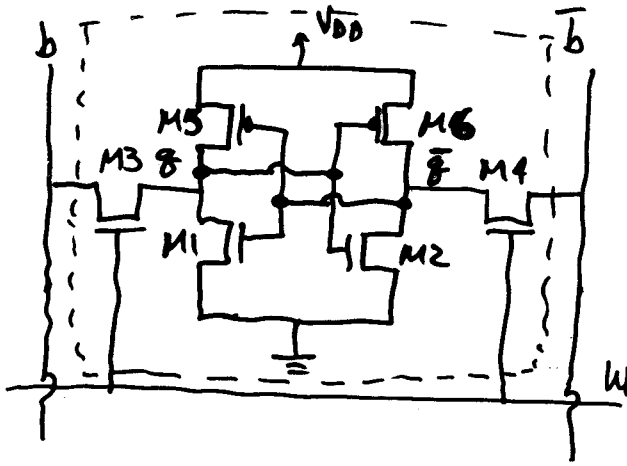
For each stage,

$$C_{in} = \frac{LE \times BE \times C_{out}}{4}$$

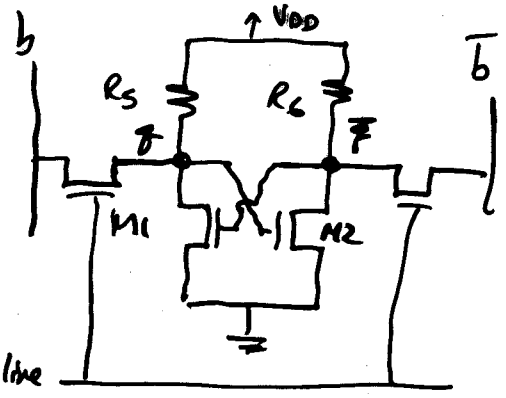
$$C_{in} = \frac{1}{4}\left(\frac{4}{3}\right)(1)(0.4167) = 0.1389$$

Static RAM (SRAM) Cell Design

6 transistor:

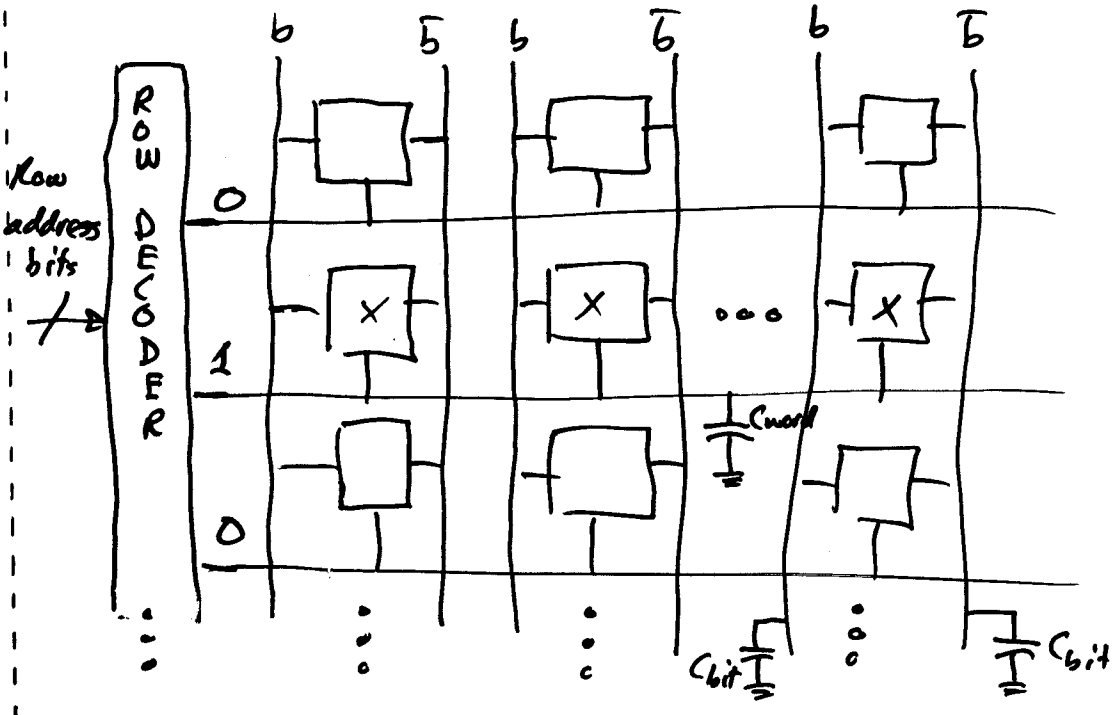


4 transistor:



$R_S = R_L \geq 10M\Omega$
(Lightly doped poly)

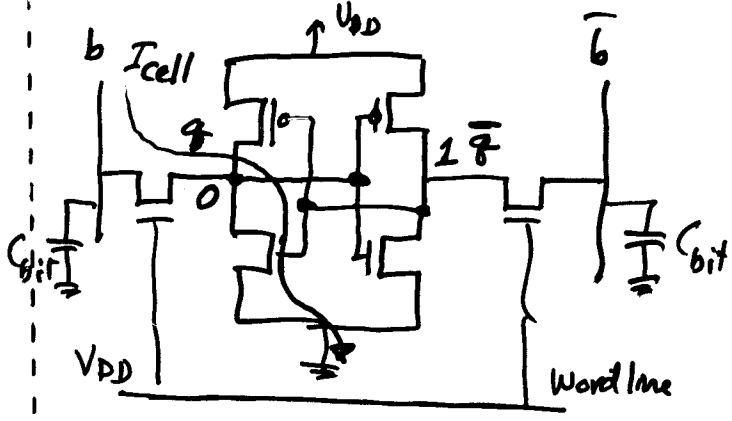
Wordline and Double Bit-line Architecture



C_{word} = (2 x gate capacitance + wire capacitance) x no. of cells in a row

C_{bit} = (Source/drain cap. + wire cap. + contact cap) x no. of cells in a column

Read operation



1.) Assume $q = 0$ and $\bar{q} = 1$

2.) Bit lines are precharged to V_{DD}.

3.) M1 ON and M2 OFF

4.) b drops, $\bar{b}$ stays constant

5.) The difference between b and $\bar{b}$ is applied to the sense amplifier.