1) Assume \( q = 0 \) ; \( \overline{q} = 1 \)

2) Bit lines are precharged to \( V_{DD} \)

3) \( M_1 \) - ON ; \( M_2 \) - OFF

4) \( W_1 \) - ON \( \Rightarrow \) \( M_3 \) and \( M_4 \) - ON

\[ ( b \rightarrow M_3 \rightarrow M_1 \rightarrow \text{gnd}) \]

5) \( b \) drops, but \( \overline{b} \) remains at \( V_{DD} \).

6) Difference between \( b \) and \( \overline{b} \) is applied to a sense amplifier.

\[ I_{emu} = C_{bit} \cdot \frac{DV}{dt} \]

\[ \Delta V = \left\{ \frac{I_{emu} \cdot dt}{C_{bit}} \right\} \]
Ex. 8.2

Compute \( W_1 \) and \( W_3 \) given that q node can change 100 mV during the read operation.
Assume \( C_{\text{bit}} = 2 \, \text{pF} \) and the sense amplifier requires a transition of 200 mV on the bit line in 2 ns. Use 0.13 nm technology.

\[
I_{\text{cell}} = C_{\text{bit}} \times \frac{\Delta V}{\Delta t} = 2 \, \text{pF} \times \frac{200 \, \text{mV}}{2 \, \text{ns}} = 200 \, \text{mA}
\]

\[
\frac{(W_1)}{L_1} \leq \frac{W_3}{L_3} \leq 1.73
\]

\[
200 \, \text{mA} = I_{\text{cell}} = I_3 = \frac{(W_3)}{L_3} \cdot (V_{\text{th}}) \cdot \text{Cox} \cdot (V_{DD} - V_T)^2 \frac{(V_{DD} - V_T - V_{T3})^2}{(V_{DD} - V_T - V_{T3}) + \varepsilon_{CN} L_3}
\]

\[
W_3 = 0.4 \, \mu m
\]
\[
W_1 = 0.7 \, \mu m
\]

Normal practice \( \Rightarrow \frac{W_1}{W_3} \leq 1.5 \)
Write operation for a 6T SRAM cell

Operation to write 1. \( \rightarrow (q=1) \)

1) Precharge \( b \) and \( \bar{b} \) to \( V_{dd} \).
2) Keep \( b = V_{dd} \) but \( \bar{b} = 0 \).
3) \( WL \) is on, both \( M3 \) and \( M4 \) are on.

\( (M6 \text{ and } M4 \rightarrow \text{on}) \)

\( M4 \) needs to be stronger than \( M6 \).

\[
\frac{W4}{W6} = 1.5 = \frac{W3}{W5}
\]

Also,

\[
\frac{W1}{W3} = \frac{W2}{W4} = 1.5
\]

\[
\frac{W1}{W5} = \frac{W2}{W6} = (1.5)^2 = 2.25
\]