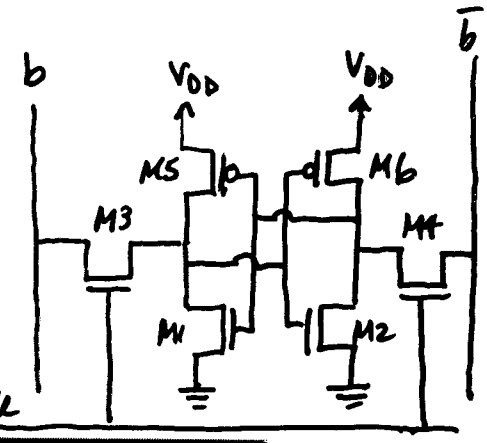
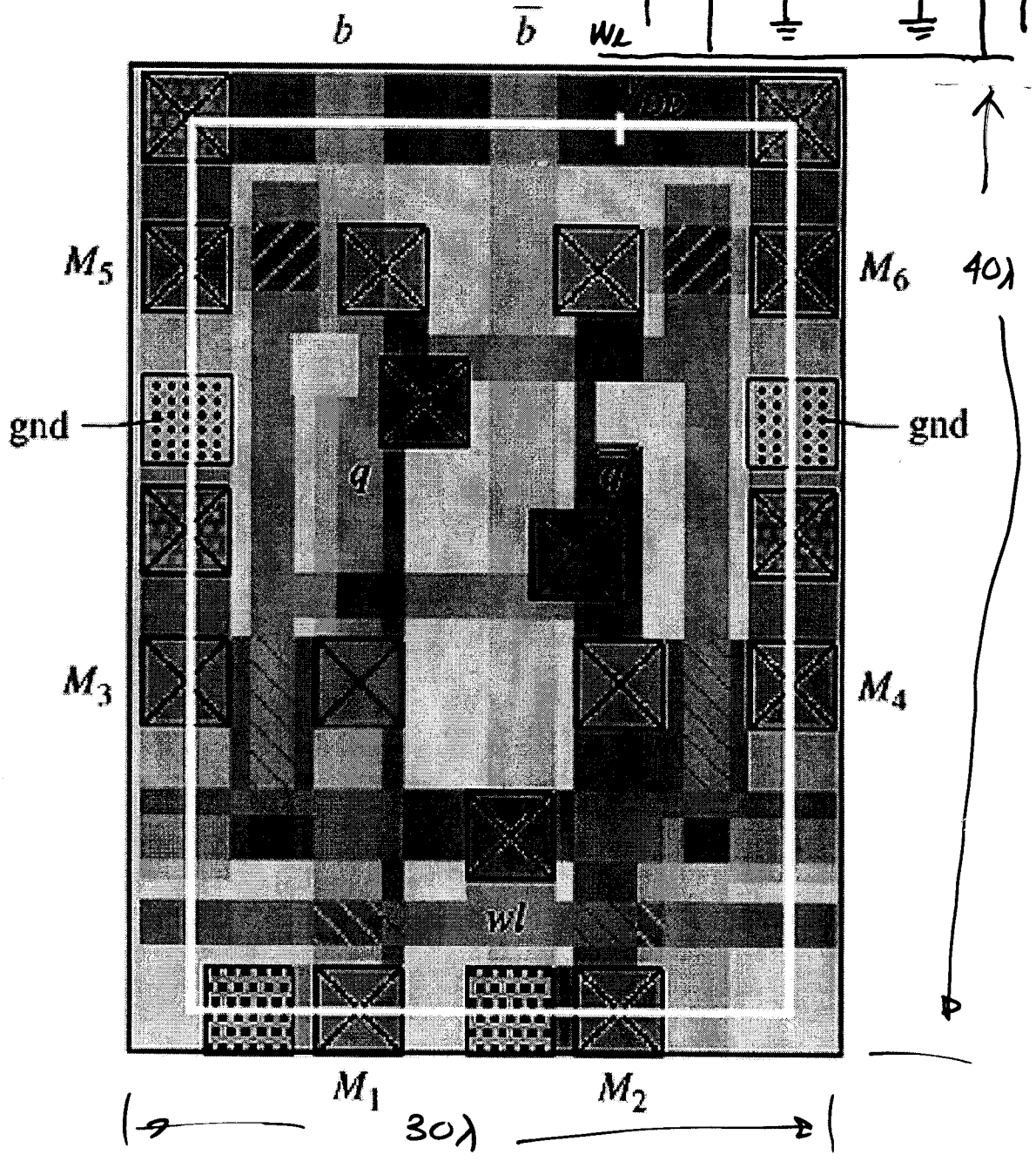
ECE4420 4/11/05

LAYOUT OF SRAM CELL





Example 8.3

What is the C_{word} and C_{bit} for a 64k SRAM using the 6T cell using Fig. 8.12. The access transistors 0.5μm/0.1μm in size. The contacts on the bitlines are shared between pairs of cells and have a capacitance of 0.5fF each. The wire capacitance is 0.2fF/μm. Assume 0.13μm technology. The cell layout is 40λ by 30λ where 1μm = 20λ.

Solution:

The core of the 64k SRAM consists of 256×256 cells.

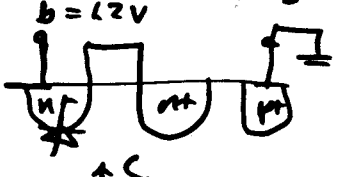
$$C_{word} = \underbrace{2C_g \times 256 \times W}_{\text{Gate cap. of M3 and M4}} + \underbrace{30\lambda \times \frac{1\mu m}{20\lambda} \times 256 \times 0.2fF/\mu m}_{\text{Wiring capacitance}}$$

$$= 2\left(2\frac{fF}{\mu m}\right)(256)(0.5\mu m) + 1.5 \times 256 \times 0.2fF/\mu m$$

$$= 512fF + 76.8fF \cong \underline{589fF}$$

$$C_{bit} = \underbrace{256\,(C_{eff}) \times 0.5\mu m}_{\text{S/D of M3/M4}} + \underbrace{256 \times 40\lambda\left(\frac{1\mu m}{20\lambda}\right)(0.2fF/\mu m)}_{\text{wire cap}} + \underbrace{\frac{1}{2}(0.5ff)256}_{\text{contact capacitance}}$$

$C_{eff} \rightarrow 0.5fF/\mu m$ because S/D-B of M3/M4 is connected to $V_{DD} = 1.2V$

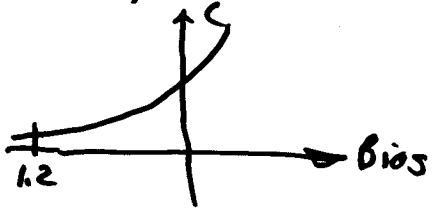


$$= 256\left(0.5\frac{fF}{\mu m}\right)(0.5\mu m)$$

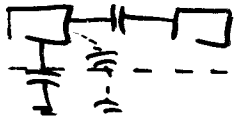
$$+ \frac{256}{20} \times 0.2fF + 64fF$$

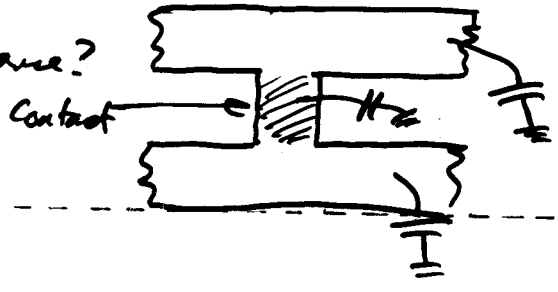
$$= 64fF + 102.4fF + 64fF$$

$$= \underline{230fF}$$



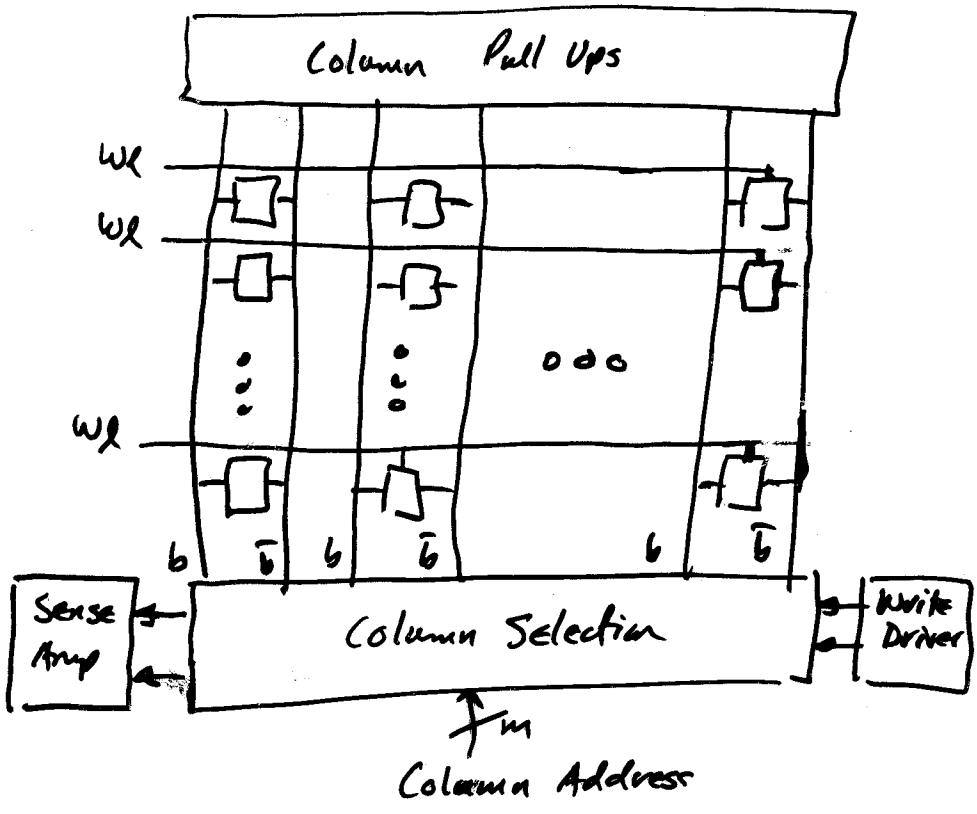
What is contact capacitance?





SRAM COLUMN I/O CIRCUITRY

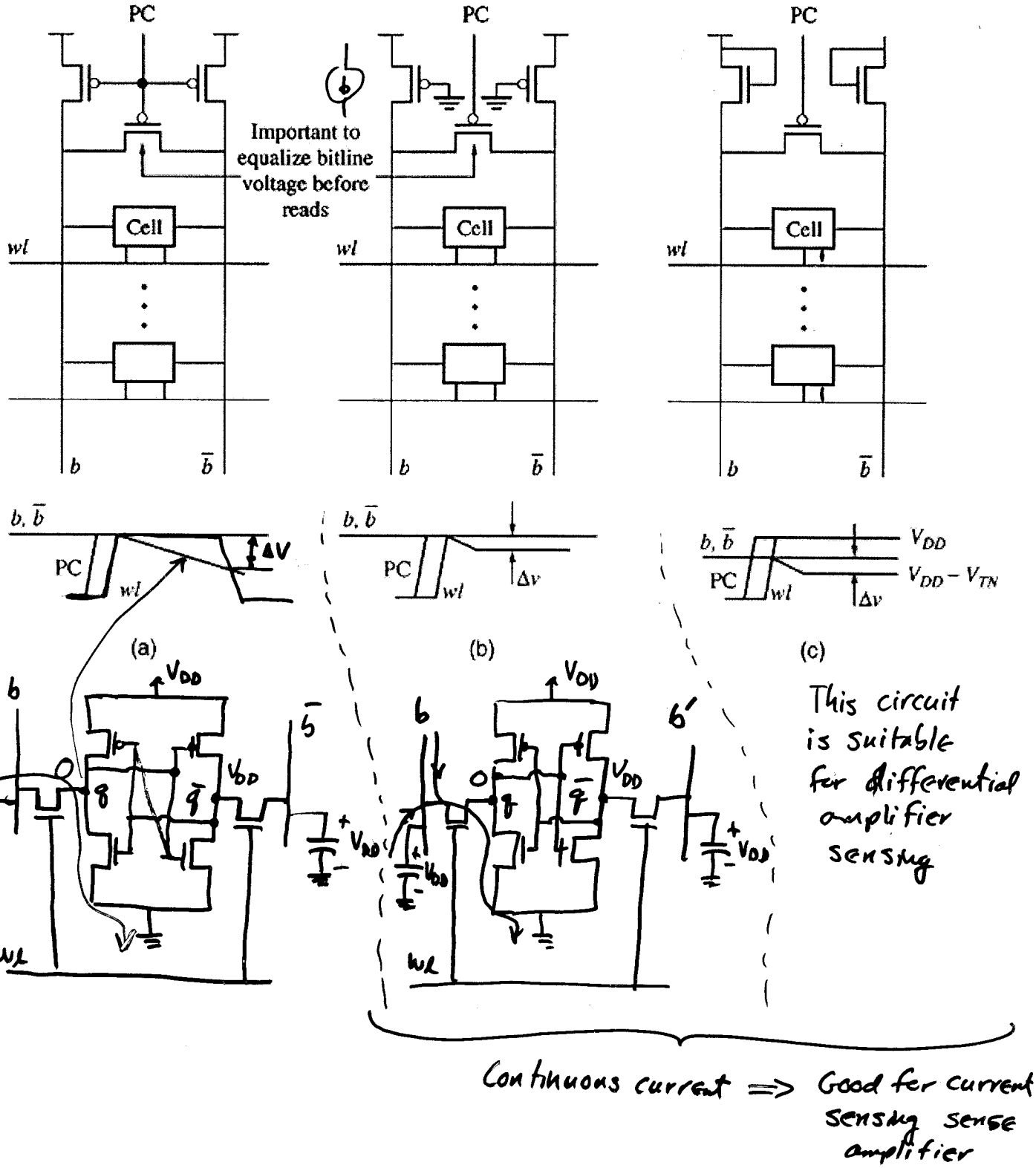
General Architecture



- Column pull-ups

Column Pull-Ups

FIGURE 8.13 – COLUMN PULL-UP CONFIGURATIONS



Column Selection

Figure 8.15 – Column decoding and multiplexing.

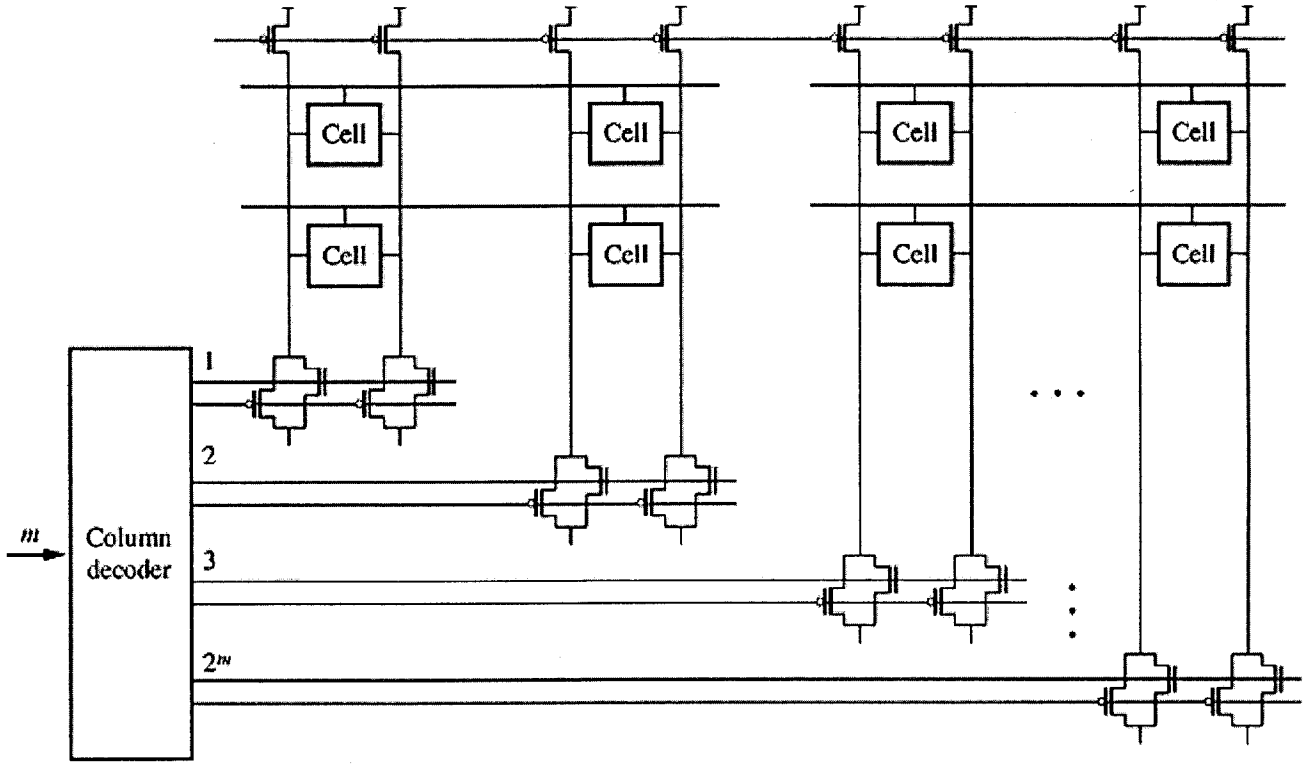


Figure 8.16 – Column selection.

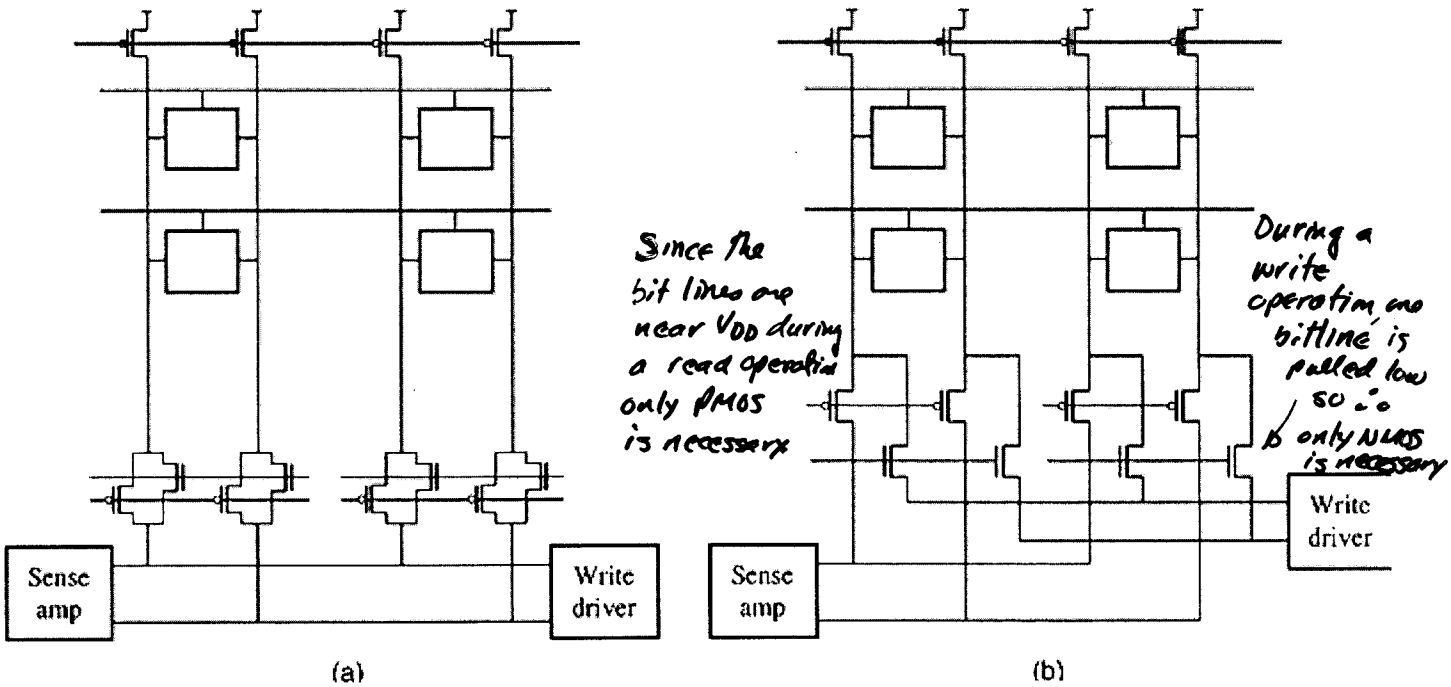
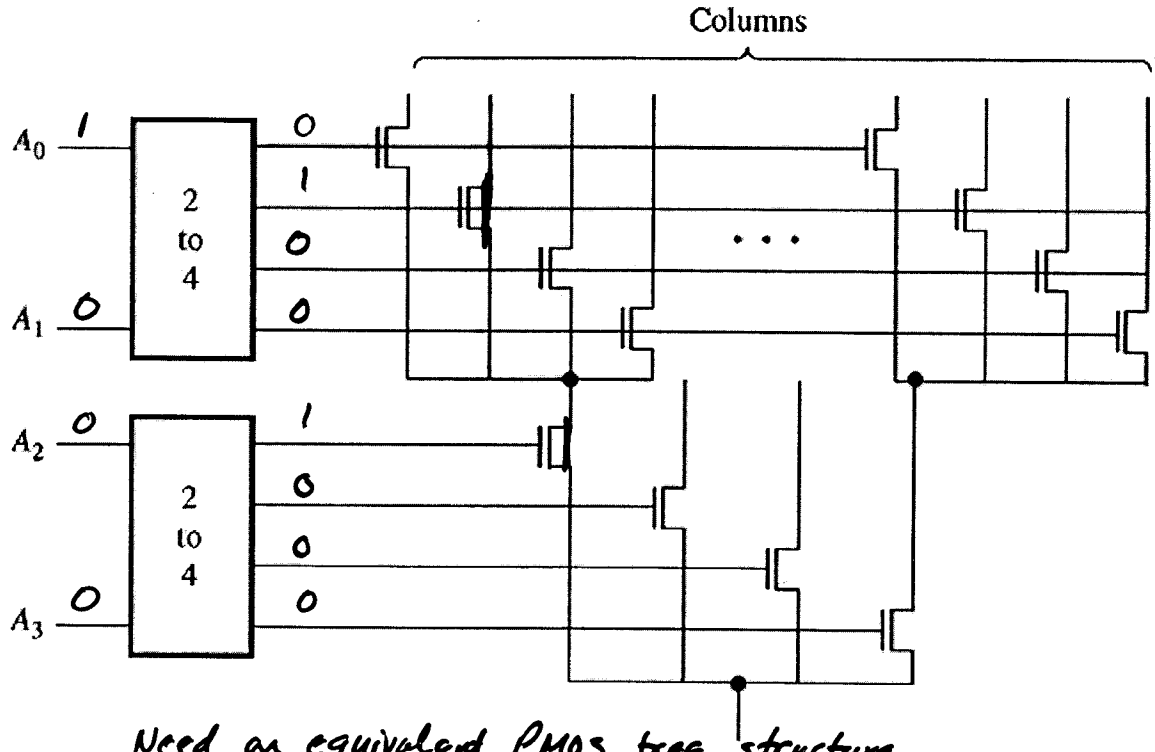


Figure 8.17 – Two-level tree decoder for a 4-bit column address.



Need an equivalent PMOS tree structure

Tradeoffs:

- Less area
- Less power
- Slower