LAYOUT OF SRAM CELL
Example 8.3

What is the Cword and Cbit for a 64k SRAM using the 6T cell using Fig. 8.12. The access transistors 0.5um/0.1um in size. The contacts on the bitlines are shared between pairs of cells and have a capacitance of 0.5fF each. The wire capacitance is 0.2fF/um. Assume 0.13um technology. The cell layout is 40\lambda by 30\lambda where 1\mu m = 20\lambda.

Solution:

The core of the 64k SRAM consists of 256x256 cells.

\[
C_{\text{word}} = 2C_g \times 256 \times W + 30\lambda \times \frac{1\mu m}{20\lambda} \times 256 \times 0.2fF/\mu m
\]

\[
= 2 \left( \frac{2fF}{\mu m} \right) (256) (0.5\mu m) + 1.5 \times 256 \times 0.2fF/\mu m
\]

\[
= 512 fF + 76.8 fF = 588.8 fF
\]

\[
C_{\text{bit}} = 256 \left( C_{\text{eff}} \right) \times 0.5\mu m + 256 \times 40\lambda \left( \frac{1\mu m}{20\lambda} \right) \left( 0.2fF/\mu m \right) + \frac{1}{2} \left( 0.5fF \right) 256
\]

\[
= 256 \left( 0.5fF \right) (0.5\mu m)
\]

\[
+ \frac{256}{20} \times 0.2fF + 64fF
\]

\[
= 64fF + 102.4fF + 64fF
\]

\[
= 230fF
\]

What is contact capacitance?
SRAM COLUMN I/O CIRCUITRY

General Architecture

- Column pull-ups

Column Selection

Sense Amp

Write Driver

Column Address

- Column pull-ups
Column Pull-Ups

FIGURE 8.13 - COLUMN PULL-UP CONFIGURATIONS

Important to equalize bitline voltage before reads

This circuit is suitable for differential amplifier sensing

Continuous current $\Rightarrow$ Good for current sensing amplifier
Column Selection

Figure 8.15 – Column decoding and multiplexing.

Figure 8.16 – Column selection.

Since the bit lines are near VDD during a read operation, only PMOS is necessary.

During a write operation, the bit line is pulled low so only NMOS is necessary.
Figure 8.17 – Two-level tree decoder for a 4-bit column address.

Need an equivalent PMOS tree structure

Tradeoffs:
- Less area
- Less power
- Slower