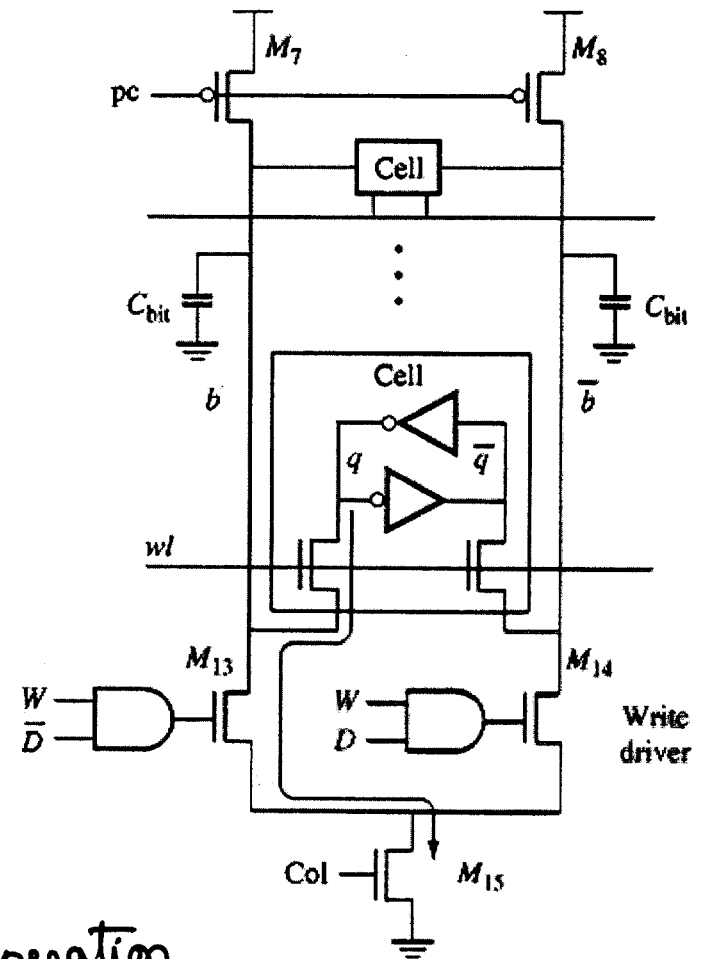
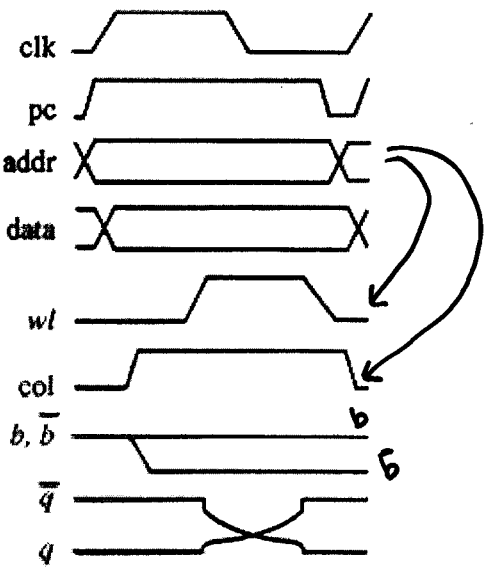
## Write Circuitry

**Figure 8.18 – Write driver circuit.**



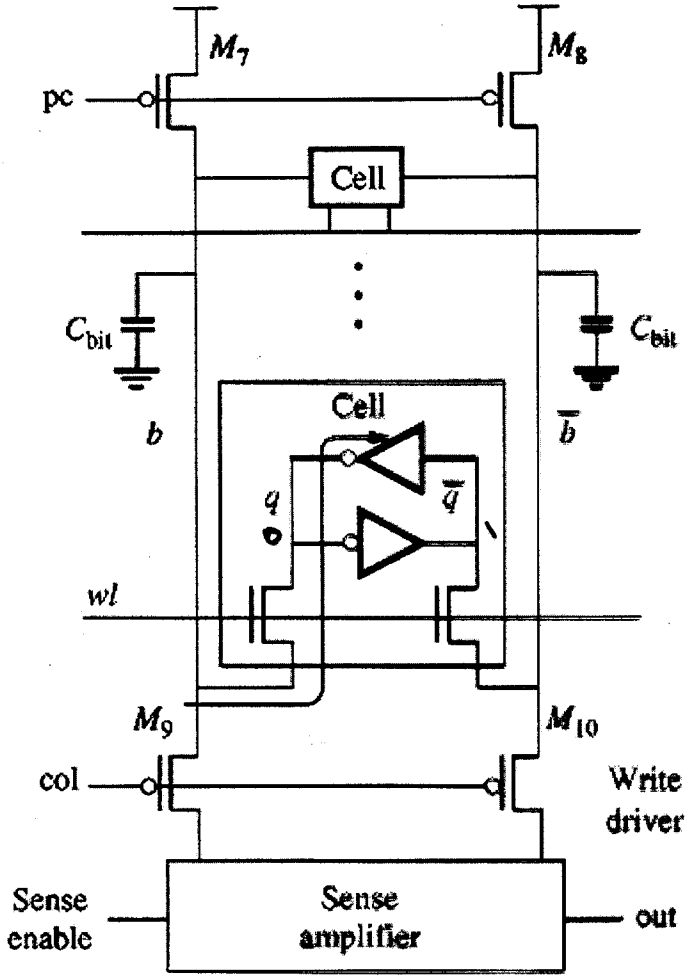

M13, M14, M15 → sized to discharge the column line.

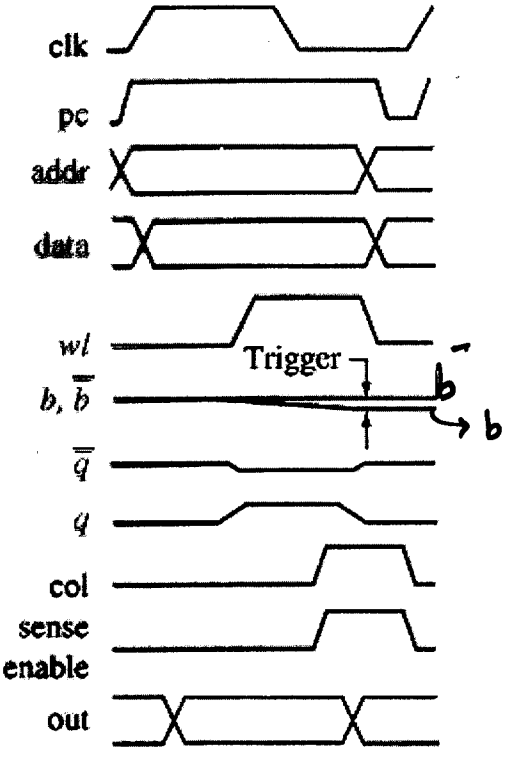
## Operation

1) Columns are precharged to $V_{DD}$.
2) Address and Data – applied and held stable.
3) Clock converts the address signals into column select and "wl" activation signals.
4) Data and write signals are applied to pull one column to ground while leaving the other at $V_{DD}$.
5) When "WL" goes high, current flows out of the cell and flips the sense of the cell.
6) Once the cell flips, "wl" and "Col" select lines go to their standby values.

## Read Circuitry

**Figure 8.19 – Basic read circuit.**



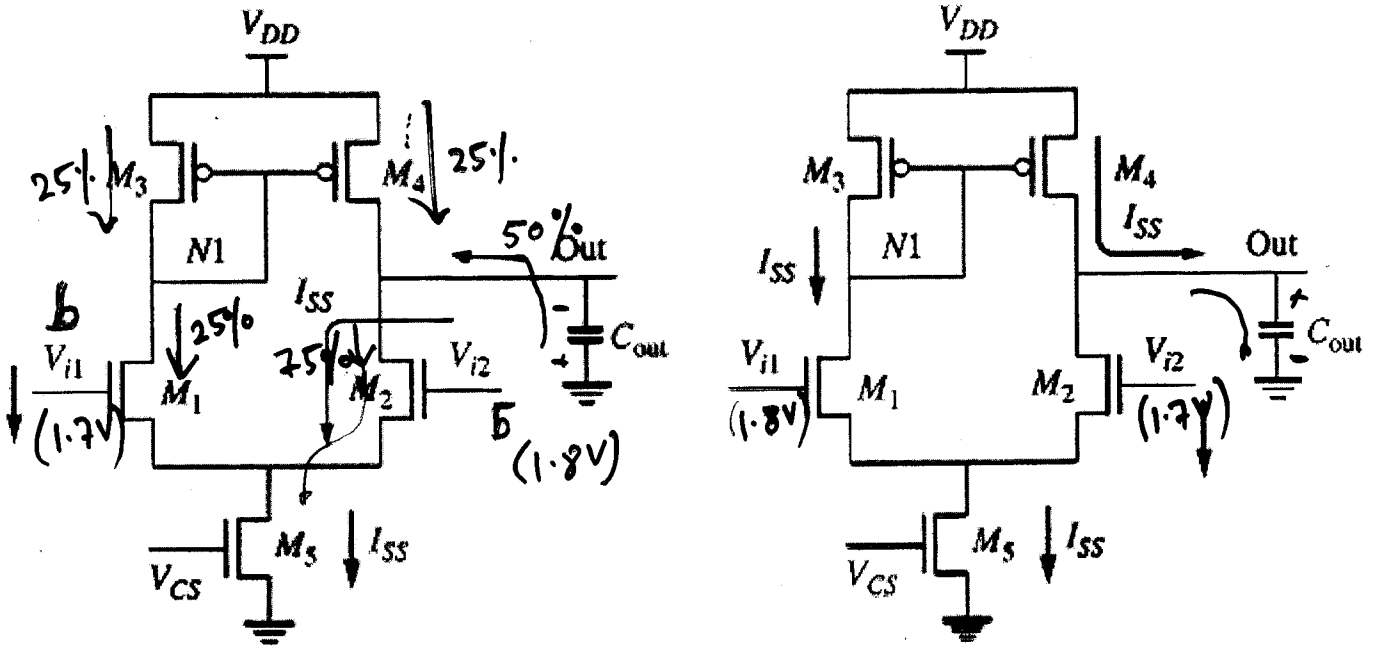




## Operation

1) Precharge column lines to $V_{DD}$.
2) Address, Data, and CLK are applied.
3) Address signals translate into column enable and "WL" activation signals.
4) Bitline (initially precharged to $V_{DD}$) begins to fall.
5) Sense amplifier → amplifies the difference in voltage between b and $\overline{b}$.

## Sense Amplifiers

**Figure 8.21 – Differential sense amplifier.**




(a) Discharging output

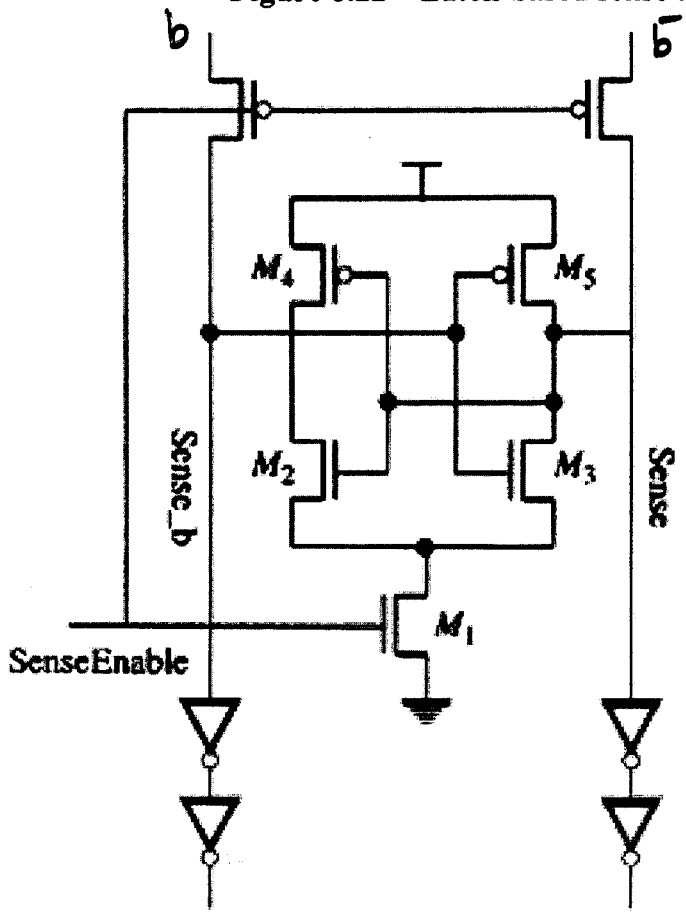
(b) Charging output

- Pull ups must be ~~saturated~~ enhancement loads.
- Need noise immunity (from noise common to $b, \bar{b}$)
- Rejects common-mode signals.
- Amplifies differential signals.
- Precharge $V_{i1}$ and $V_{i2}$ to $(V_{DD} - V_{TN})$.

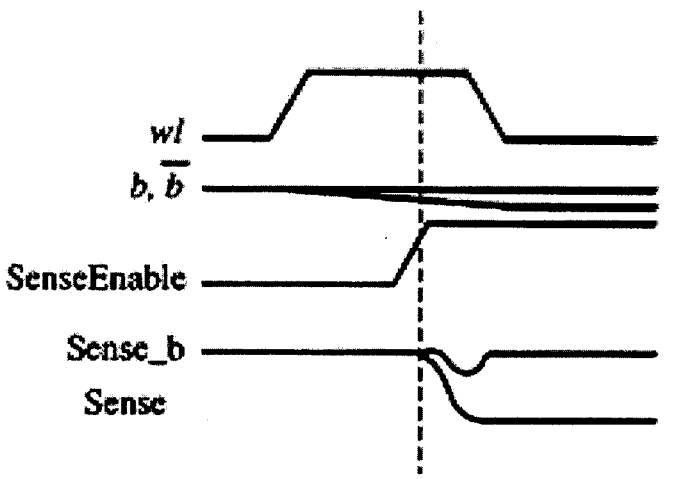
$$P_{diss} = (V_{DD} \cdot I_{SS}).$$

$$\text{Slew rate} = \frac{I_{SS}}{C_{out}} \Rightarrow \Delta\tau = \frac{C_{out}}{I_{SS}} \cdot (\Delta V_{out})$$

**Figure 8.22 – Latch-based sense amplifier.**




- Low power
- Slower
- Sensitive to noise as it needs large input voltage change.



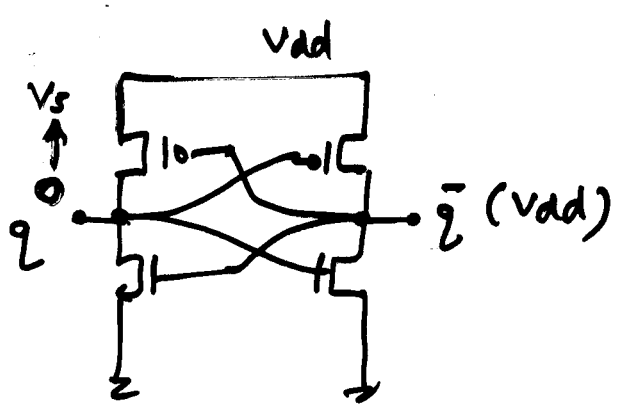



**Figure 8.23 – Replica circuit for sense amplifier clock enable**

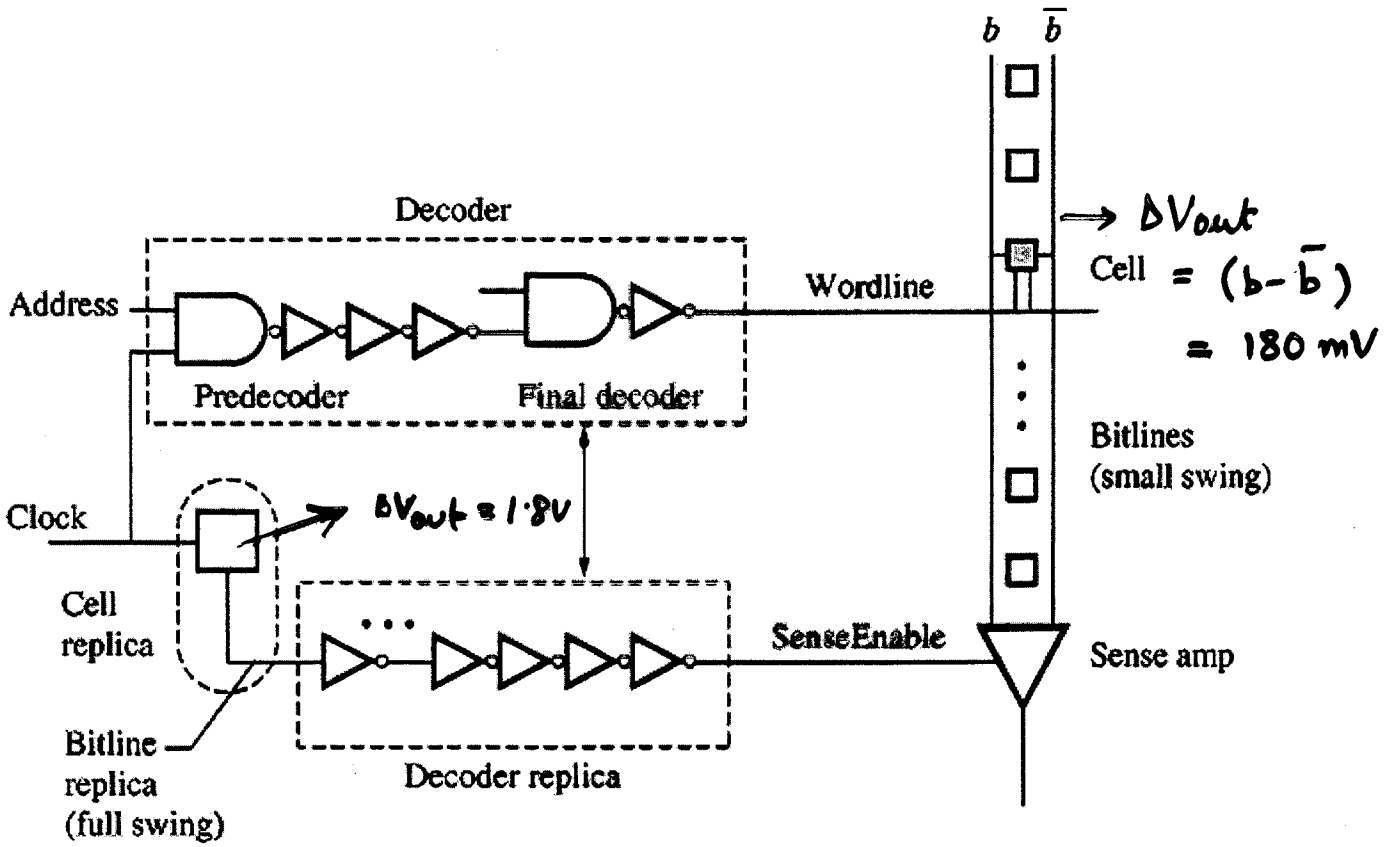


**Figure 8.24 – Replica cell design.**