Write Circuitry

Figure 8.18 – Write driver circuit.

Operation
1) Columns are precharged to VDD.
2) Address and Data – applied and held stable.
3) Clock converts the address signals into column select and “WE” activation signals.
4) Data and write signals are applied to pull one column to ground while leaving the other at VDD.
5) When “WE” goes high, current flows out of the cell and flips the sense of the cell.
6) Once the cell flips, “WE” and “Col” select lines go to their standby values.
Read Circuitry

Figure 8.19 – Basic read circuit.

Operation
1) Precharge column lines to VDD.
2) Address, Data, and clk are applied.
3) Address signals translate into column enable and "wl" activation signals.
4) Bitline (initially precharged to VDD) begins to fall.
5) Sense amplifier → amplifies the difference in voltage between \( b \) and \( \overline{b} \).
Sense Amplifiers

Figure 8.21 – Differential sense amplifier.

- Pull ups must be saturated enhancement loads.
- Need noise immunity (from noise common to \( b, \bar{b} \))
- Rejects common-mode signals.
- Amplifies differential signals.
- Precharge \( V_{i1} \) and \( V_{i2} \) to \( (V_{DD} - V_{TN}) \).

\[
P_{\text{dis}} = (V_{DD} \times I_{SS}).
\]

Slew rate = \( \frac{I_{SS}}{C_{out}} \) \( \Rightarrow \) \( \Delta t = \frac{C_{out} \cdot (\Delta V_{out})}{I_{SS}} \)
Figure 8.22 – Latch-based sense amplifier.

- Low power
- Slower
- Sensitive to noise or it needs large input voltage change.
Figure 8.23 – Replica circuit for sense amplifier clock enable

- Address
- Predecoder
- Final decoder
- Wordline
- Cell $= (b - \overline{b})$
- Bitlines (small swing)
- $\Delta V_{out} = 1.8\text{V}$
- SenseEnable
- Sense amp

$b$ $\overline{b}$
Figure 8.24 – Replica cell design.

Memory block

Replica bitline (cut here)

26

$\left( \Delta V_{\text{out}} \right) = 1.8 \text{V}$

Replica cell

$\left( 0 - \bar{b} = 180 \right) \text{ mV}$

256