Exam #3 – Friday, April 22, 2005

Problem Session – Thursday, 7pm–8pm

Elmore Delay –

$$\tau_i = \sum_k (C_k R_{ik})$$

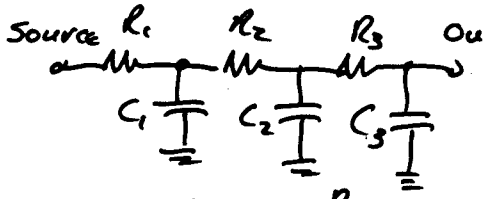
i = node of interest

C_k = capacitance to gnd at node k

R_{ik} = Σ of all R's in common with the path from node i to node k.

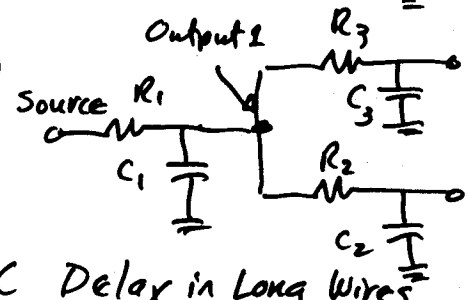
Example

a.)



$$\tau = R_1C_1 + C_2(R_1+R_2) + C_3(R_1+R_2+R_3)$$

b.)



$$\tau_1 = R_1(C_1+C_2+C_3)$$

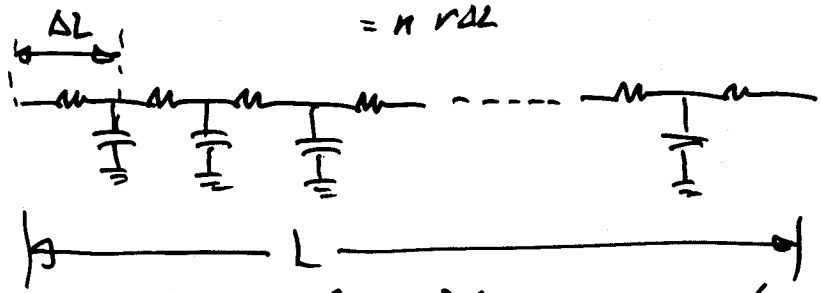
$$\tau_2 = R_1C_1 + R_2C_2 + (R_1+R_2)C_3$$

$$\tau_3 = R_1C_1 + R_2C_2 + (R_1+R_3)C_3$$

RC Delay in Long Wires

Dividing a wire of length L into n sections we get,

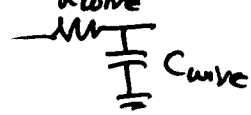
$$\Delta L = \frac{L}{n} \rightarrow R_{wire} = nR_{int} = nr\Delta L \quad \& \quad C_{wire} = nC_{int} = nc\Delta L$$



$$\tau_{Elmore} = (r\Delta L)(c\Delta L) + (2r\Delta L)(c\Delta L) + \cdots + n(r\Delta L)c\Delta L$$

$$= (\Delta L)^2 rc\,[1+2+3+\cdots+n] = (\Delta L)^2 rc\,\frac{n(n+1)}{2}$$

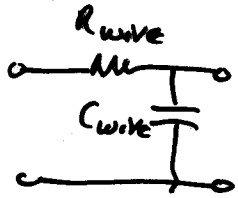
$$\approx (\Delta L)^2 rc\,\frac{n^2}{2} = \frac{R_{wire}C_{wire}}{2}$$



Actual propagation delay is closer to $0.38R_{wire}C_{wire}$.

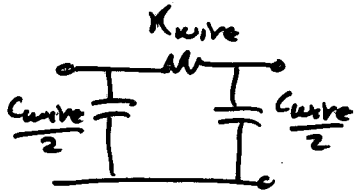
Note that the delay increases with L^2.

Possible lumped models for wires

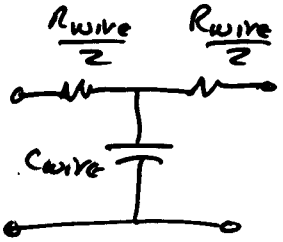


L-model

Delay = $R_{wire} C_{wire}$



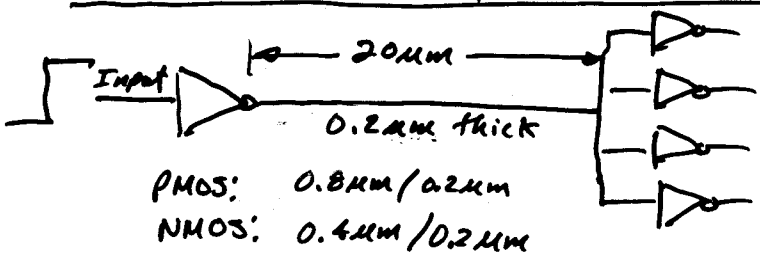
Pi-model



Tee-model

Delay $\approx 0.5\, R_{wire} C_{wire}$

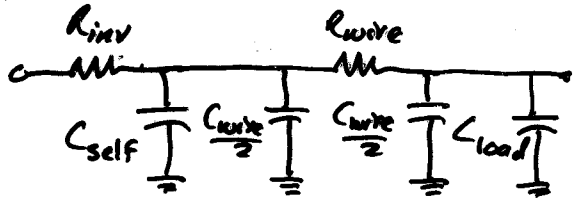
Example 10.2 – Delay with Short Wires



PMOS: 0.8μm/0.2μm
NMOS: 0.4μm/0.2μm

$C_g = 2\,fF/\mu m$
$C_{eff} = 1\,fF/\mu m$
$C_{int} = 0.2\,fF/\mu m$
$R_{int} = 54\,m\Omega/\square$

Find the propagation delay through the first inverter. Assume 0.18 μm CMOS technology.



$C_{load} = 4 \times C_g (W_n + W_p)$
$= 4 \times 2\frac{fF}{\mu m}(1.2\mu m) = 9.6fF$

$C_{self} = C_{eff}(W_n + W_p) = 1\frac{fF}{\mu m}(1.2\mu m) = 1.2fF$

$C_{wire} = C_{int} L_{wire} = 0.2\frac{fF}{\mu m} \times 20\mu m = 4fF$

$R_{wire} = R_{int} \times \frac{20}{0\Omega} = 5.4\Omega$

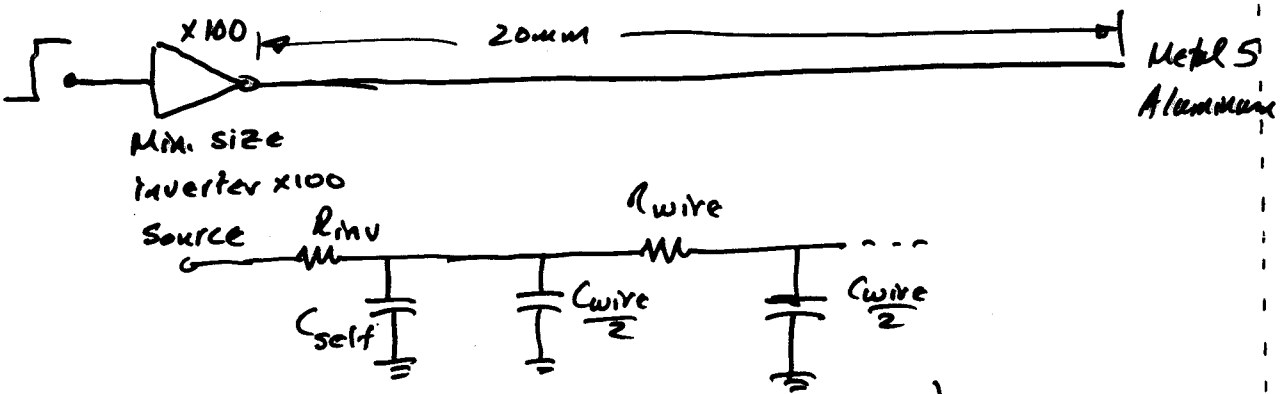
$R_{inv} = 12.5k\left(\frac{0.2}{0.4}\right) = 6.25k\Omega$

$\tau_{delay} = R_{inv}\left(C_{self} + \frac{C_{wire}}{2}\right) + (R_{inv} + R_{wire})\left(C_{load} + \frac{C_{wire}}{2}\right)$
$= (6.25k\Omega)(3.2fF) + (6.25k\Omega + 5.4\Omega)(11.6fF) = 92.6ps$

Note that the interconnect (wire) has little influence.

Example 10.3 – Delay with a long wire

Repeat Ex. 10.2 if $L = 20mm$ and $W = 0.5\mu m$



$$R_{wire} = R_{int} L = (0.027\Omega/\square)\left(\frac{20{,}000\mu m}{0.5\mu m}\right) = 1080\Omega$$

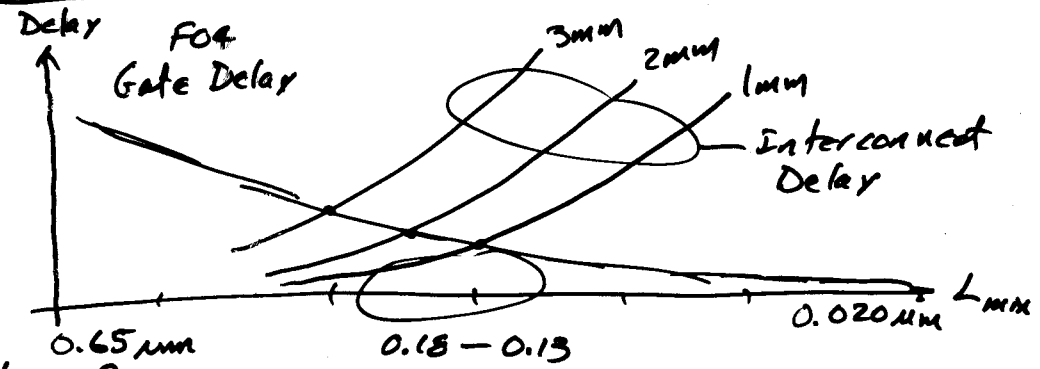
$$R_{inv} \approx \frac{12.5K}{100} = 125\Omega$$

$$C_{self} = C_{eff}(3W)\times 100 = \left(\frac{1fF}{\mu m}\right)(3\times 0.2\mu m)(100) = 60fF$$

$$C_{wire} = C_{int} L = 0.1\frac{fF}{\mu m}\times 20K\mu m = 2pF$$

$$\tau_{delay} \approx (125\Omega)(1pF) + (125+1080)(1pF) = 1.33ns$$

Gate Delay vs. Interconnect Delay



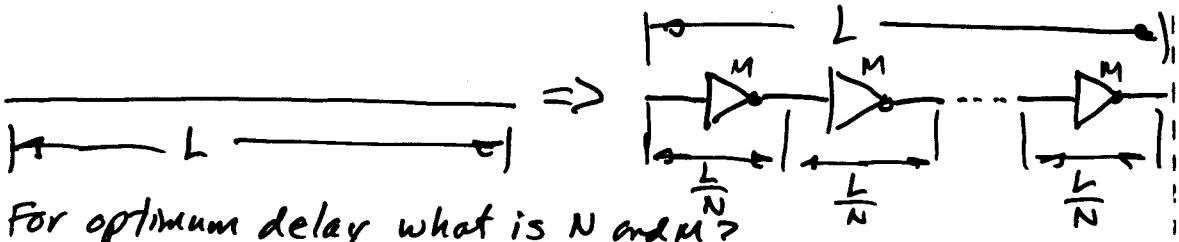
Optimum?

$$FO4\ delay \approx 0.38\, R_{int} C_{int} L_{critical}^2$$

$$L_{critical} = \sqrt{\frac{FO4\ delay}{0.38 R_{int} C_{int}}}$$

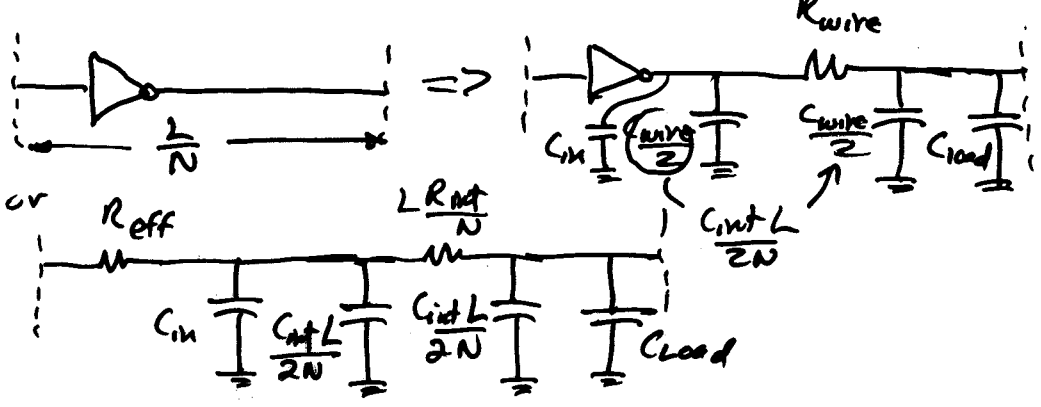
BUFFER INSERTION FOR VERY LONG WIRES

Buffers can be inserted in very long wires to reduce the delay.



For optimum delay what is N and M?

Line segment with a buffer:



$$C_{load} = C_{out} = C_g(W_n + W_p) = C_g(W + BW) = C_G(1+B)$$

where $B = W_p/W_n$

$$C_{in} = C_{eff}(W_n + W_p) = C_{eff}W(1+B) = C_J(1+B)$$

$$R_{eff} = \frac{R_{eqn}}{M}$$ where M = optimal buffer size for the insertion problem

Elmore delay for a segment-

$$\text{Total delay} = N\left(C_G + C_J\right)R_{eqn}(1+B) + \left[C_G(1+B)R_{int}M + \frac{C_{int}R_{eqn}}{M}\right] + \left(\frac{C_{int}R_{int}}{2N^2}\right)L^2$$