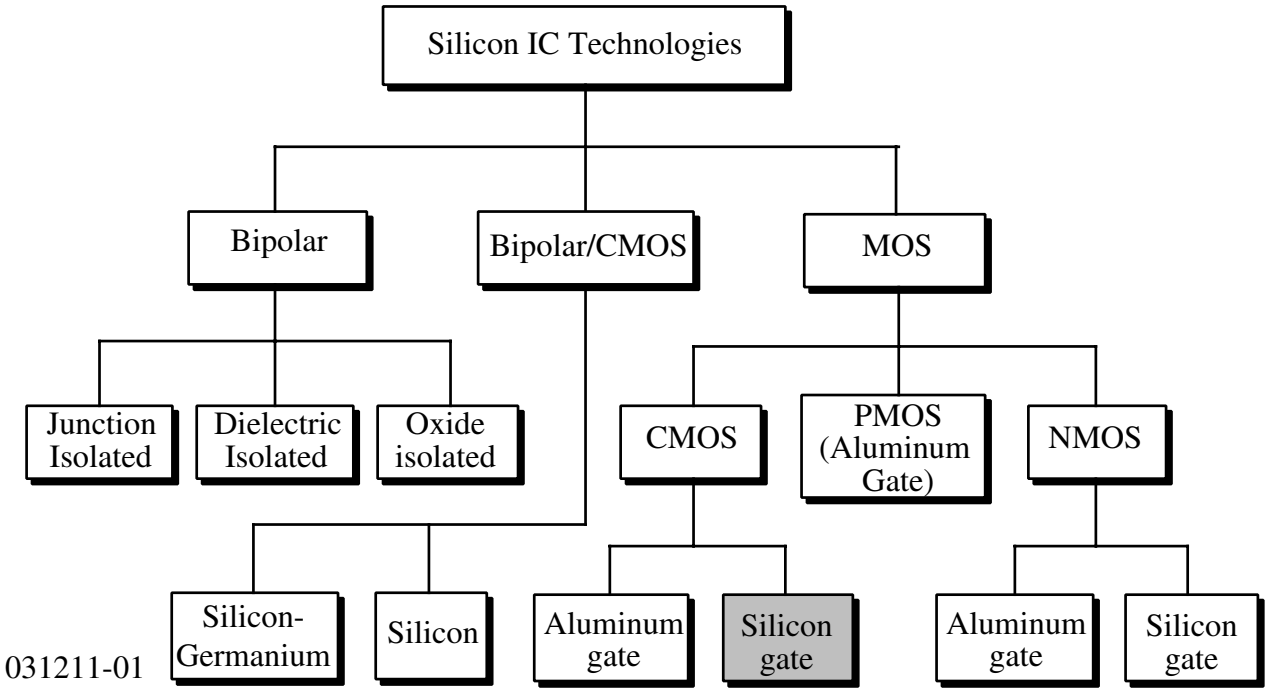
CMOS TECHNOLOGY

INTRODUCTION

Classification of Silicon Technology



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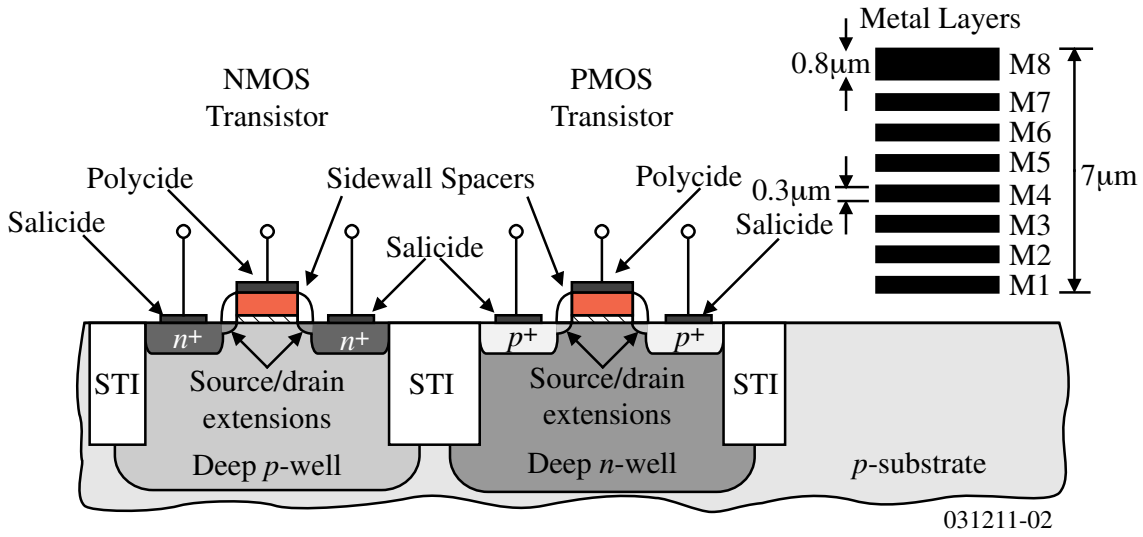
Components of a Modern CMOS Technology

Illustration of a modern CMOS process:



In addition to NMOS and PMOS transistors, the technology provides:

1.) A deep *n*-well that can be utilized to reduce substrate noise coupling.

2.) A MOS varactor that can serve in VCOs

3.) At least 6 levels of metal that can form many useful structures such as inductors, capacitors, and transmission lines.

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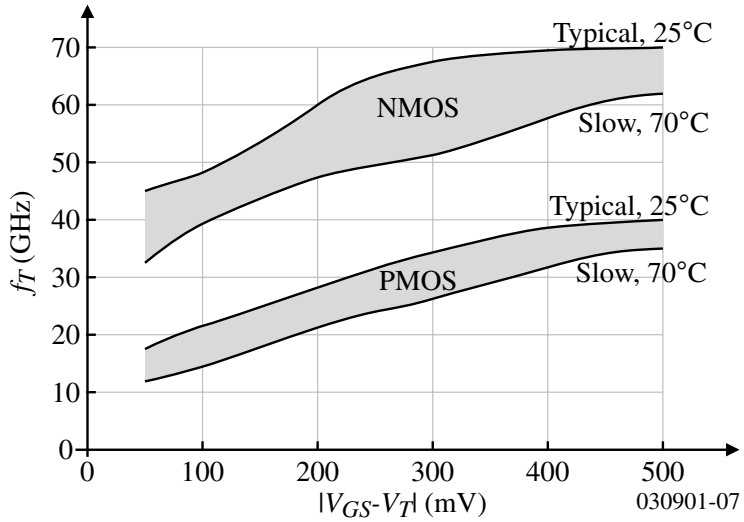
CMOS Components – Transistors

f_T as a function of gate-source overdrive, V_{GS}-V_T (0.13μm):



The upper frequency limit is probably around 40 GHz for NMOS with an f_T in the vicinity of 60GHz with an overdrive of 0.5V and at the slow-high temperature corner.

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TYPICAL DSM CMOS FABRICATION PROCESS

Major Fabrication Steps for a DSM CMOS Process

1.) *p* and *n* wells
2.) Shallow trench isolation
3.) Threshold shift
4.) Thin oxide and gate polysilicon
5.) Lightly doped drains and sources
6.) Sidewall spacer
7.) Heavily doped drains and sources
8.) Siliciding (Salicide and Polycide)
9.) Bottom metal, tungsten plugs, and oxide
10.) Higher level metals, tungsten plugs/vias, and oxide
11.) Top level metal, vias and protective oxide

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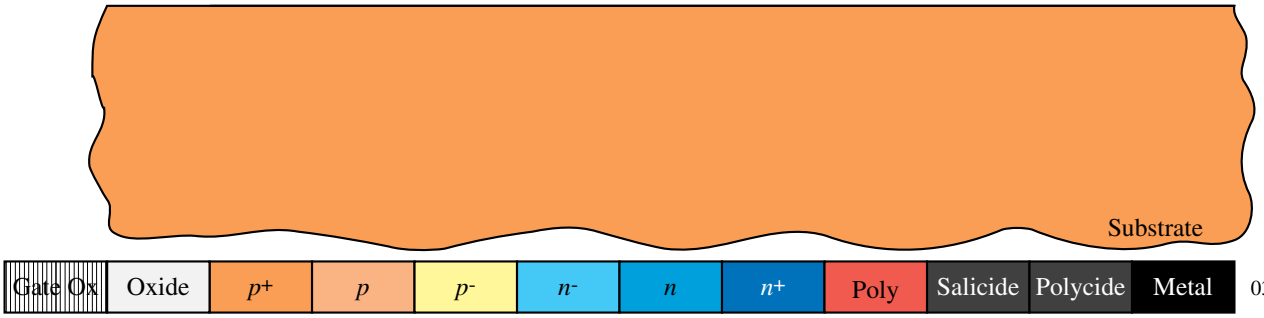
Step 1 – Starting Material

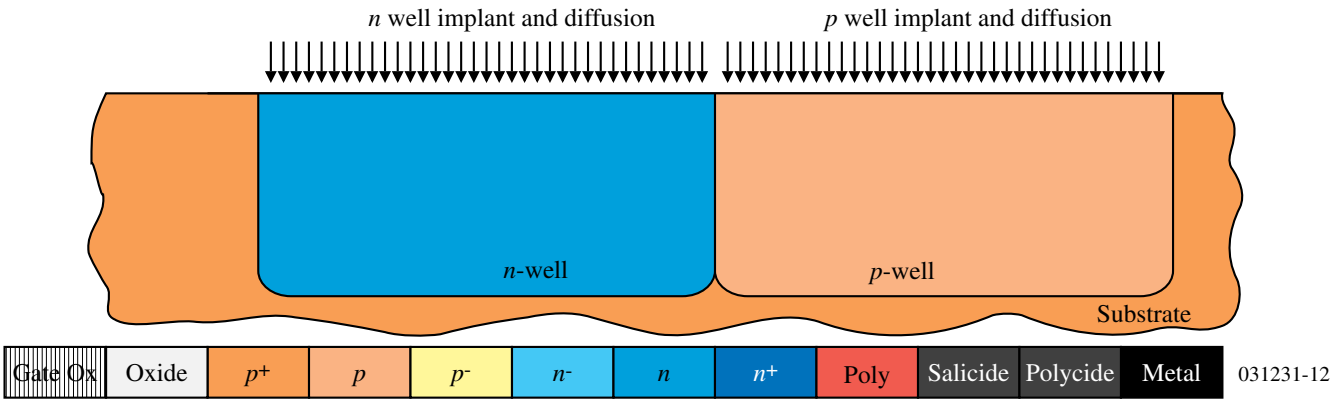
The substrate should be highly doped to act like a good conductor.



Step 2 - *n* and *p* wells

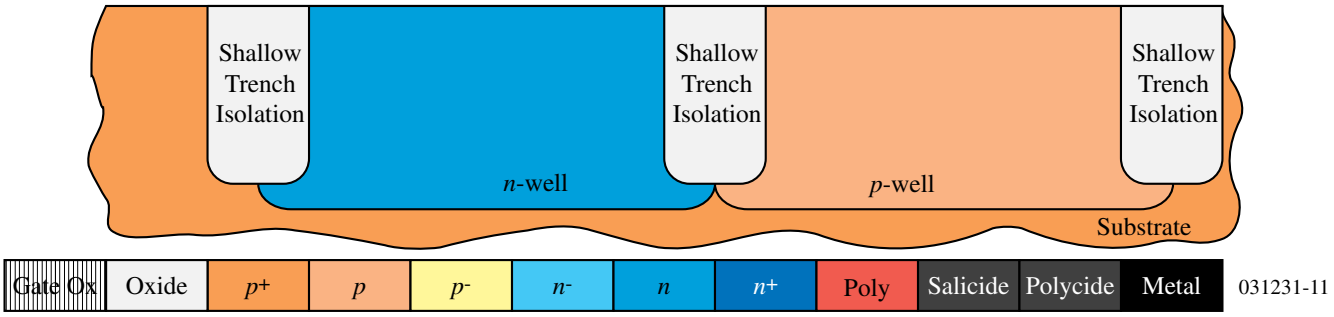
These are the areas where the transistors will be fabricated - NMOS in the *p*-well and PMOS in the *n*-well.

Done by implantation followed by a deep diffusion.



Step 3 – Shallow Trench Isolation

The shallow trench isolation (STI) electrically isolates one region/transistor from another.



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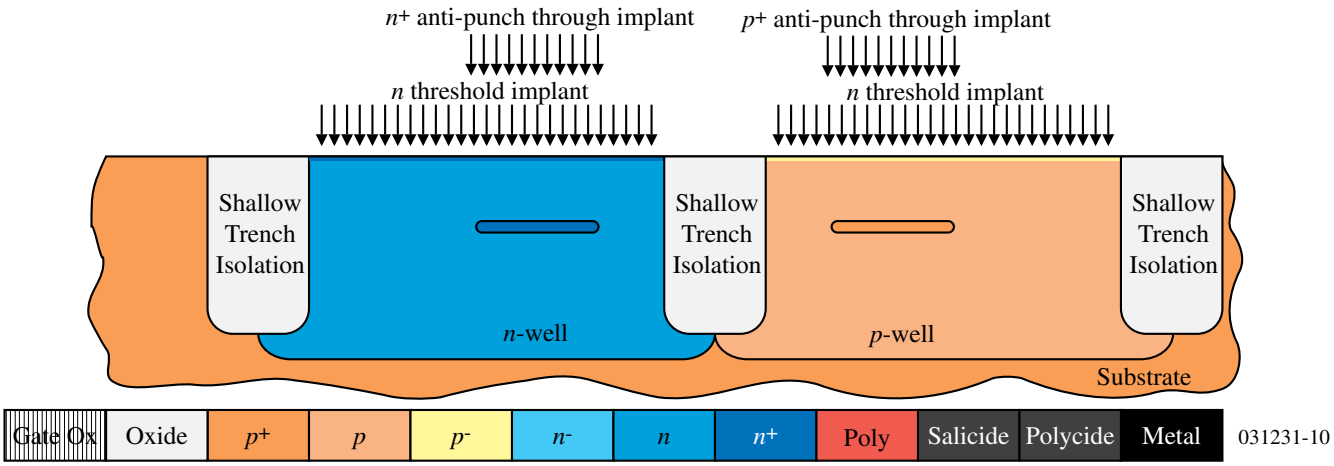
Step 4 – Threshold Shift and Anti-Punch Through Implants

The natural thresholds of the NMOS is about 0V and of the PMOS is about –1.2V. An *n*- implant is used to make the NMOS harder to invert and the PMOS easier resulting in threshold voltages balanced around zero volts.

Also an implant can be applied to create a higher-doped region beneath the channels to prevent punch-through from the drain depletion region extending to source depletion region.



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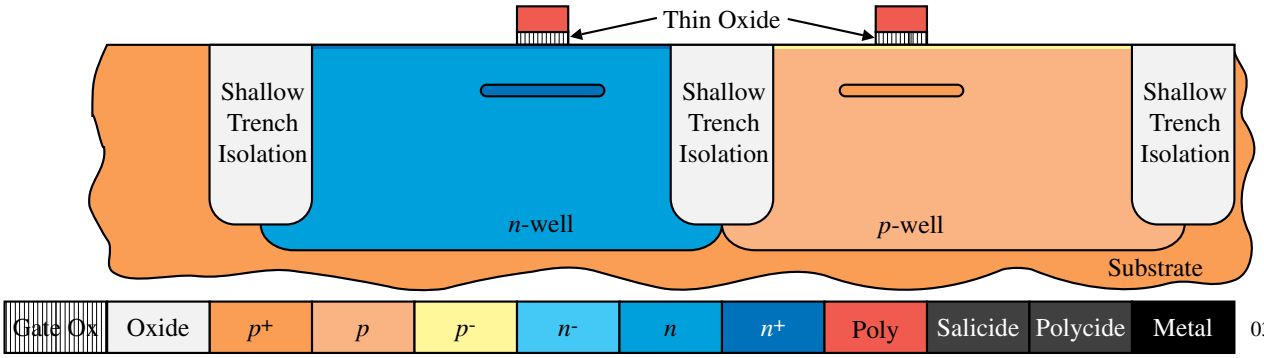
Step 5 – Thin Oxide and Polysilicon Gates

A thin oxide is deposited followed by polysilicon. These layers are removed where they are not wanted.



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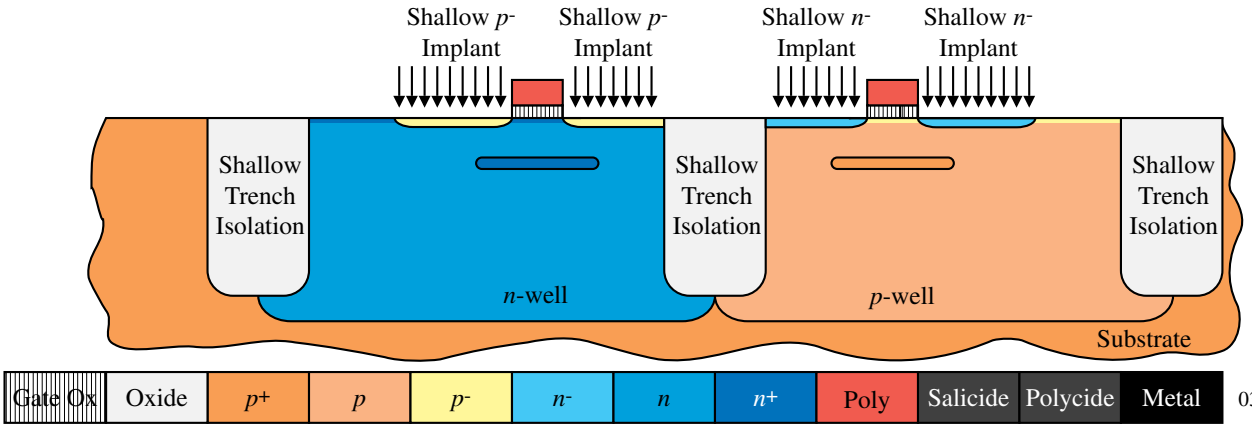
Step 6 – Lightly Doped Drains and Sources

A lightly-doped implant is used to create a lightly-doped source and drain next to the channel of the MOSFETs.



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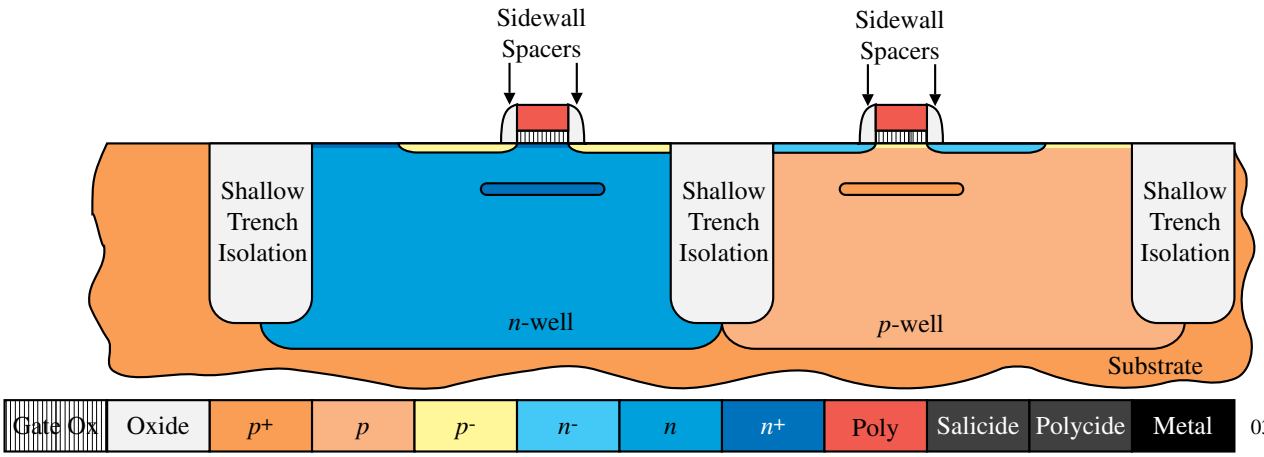
Step 7 – Sidewall Spacers

A layer of dielectric is deposited on the surface and removed in such a way as to leave "sidewall spacers" next to the thin-oxide-polysilicon-polycide sandwich. These sidewall spacers will prevent the part of the source and drain next to the channel from becoming heavily doped.



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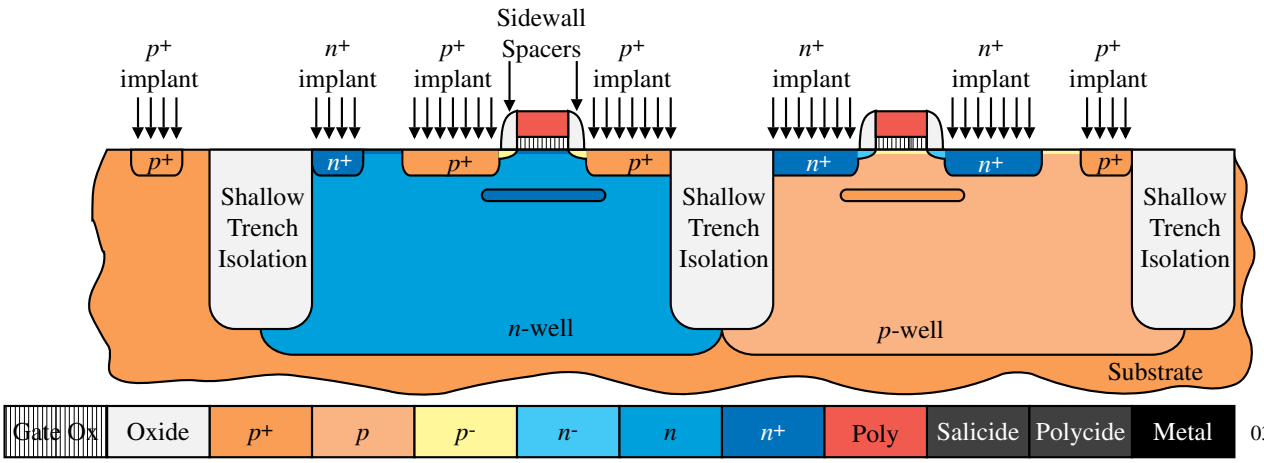
Step 8 – Implantation of the Heavily Doped Sources and Drains

Note that not only does this step provide the completed sources and drains but allows for ohmic contact into the wells and substrate.



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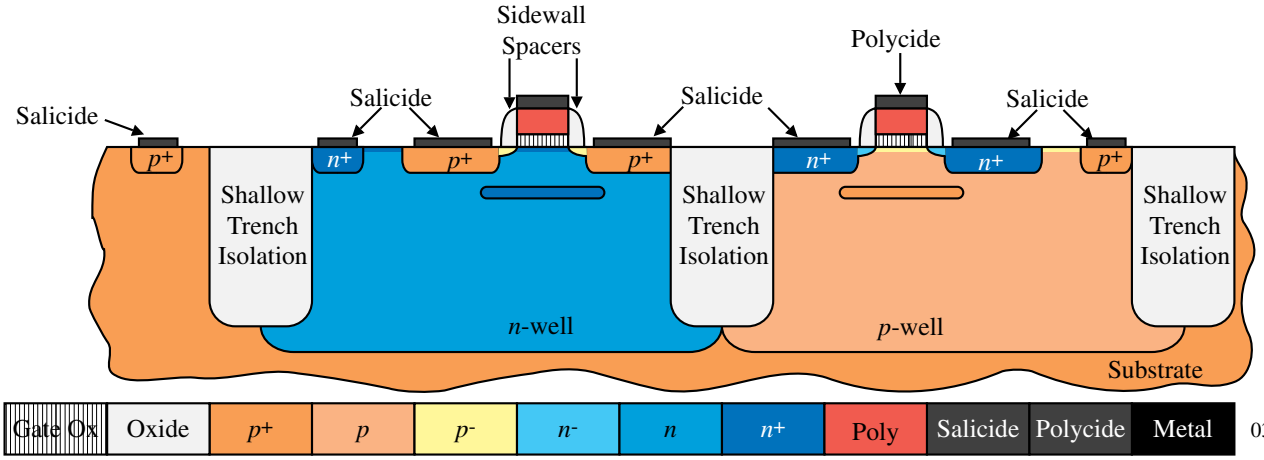
Step 9 – Siliciding

Siliciding and polyciding is used to reduce interconnect resistivity by placing a low-resistance silicide such as $TiSi_2$, WSi_2, $TaSi_2$, etc. on top of the diffusions.



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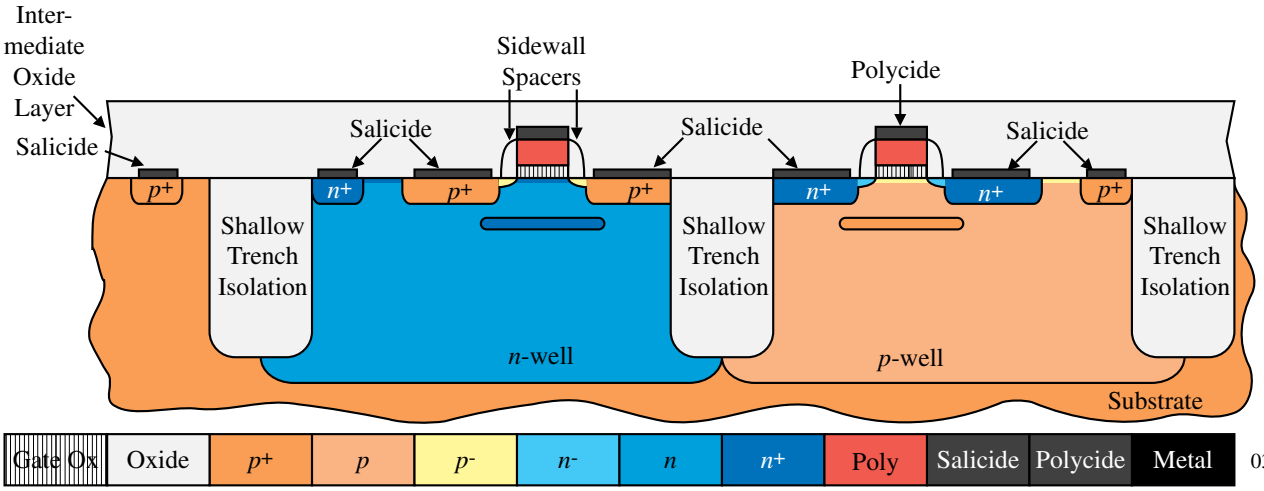
Step 10 – Intermediate Oxide Layer

An oxide layer is used to cover the transistors and to planarize the surface.



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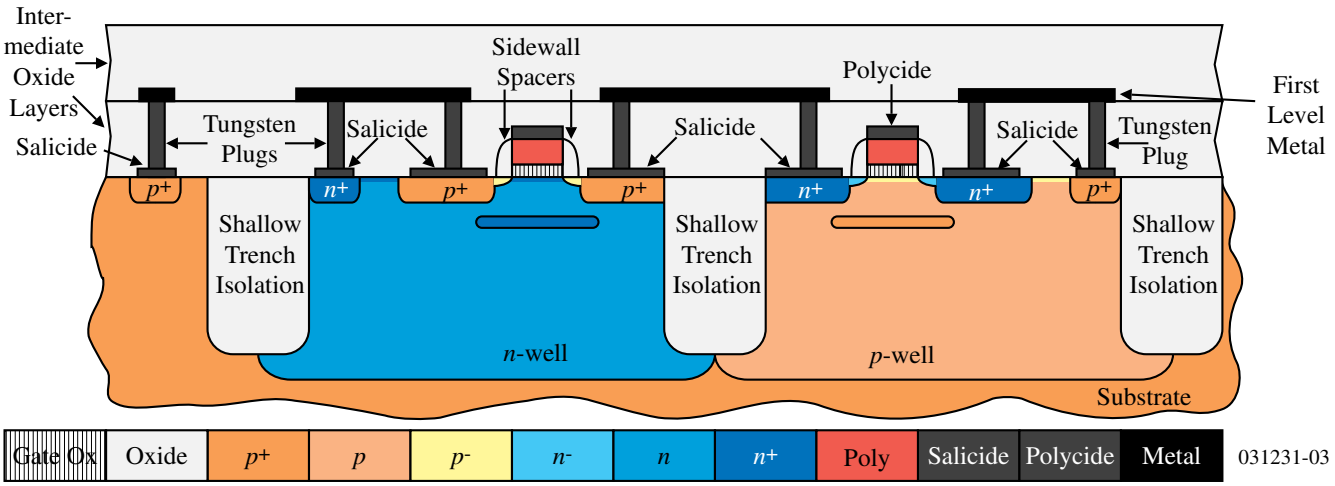
Step 11- First-Level Metal

Tungsten plugs are built through the lower intermediate oxide layer to provide contact between the devices, wells and substrate to the first-level metal.



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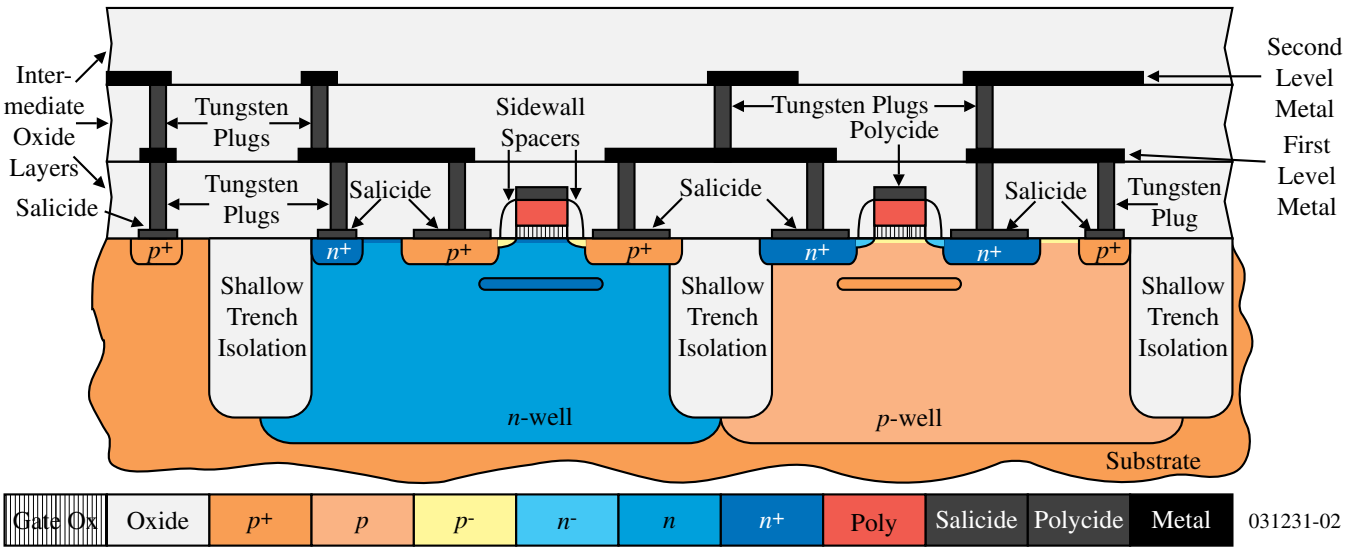
Step 12 – Second-Level Metal

The previous step is repeated to from the second-level metal.



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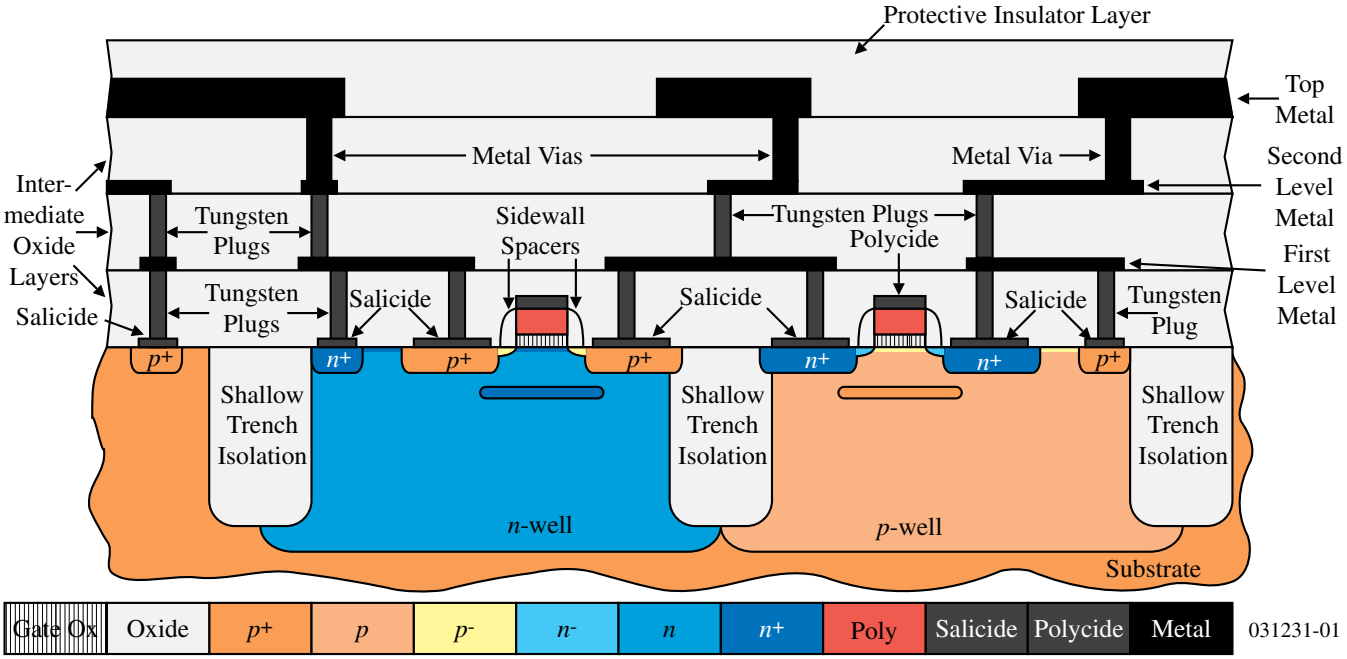
Completed Fabrication

After multiple levels of metal are applied, the fabrication is completed with a thicker top-level metal and a protective layer to hermetically seal the circuit from the environment. Note that metal is used for the upper level metal vias. The chip is electrically connected by removing the protective layer over large bonding pads.



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Scanning Electron Microscope of a MOSFET Cross-section

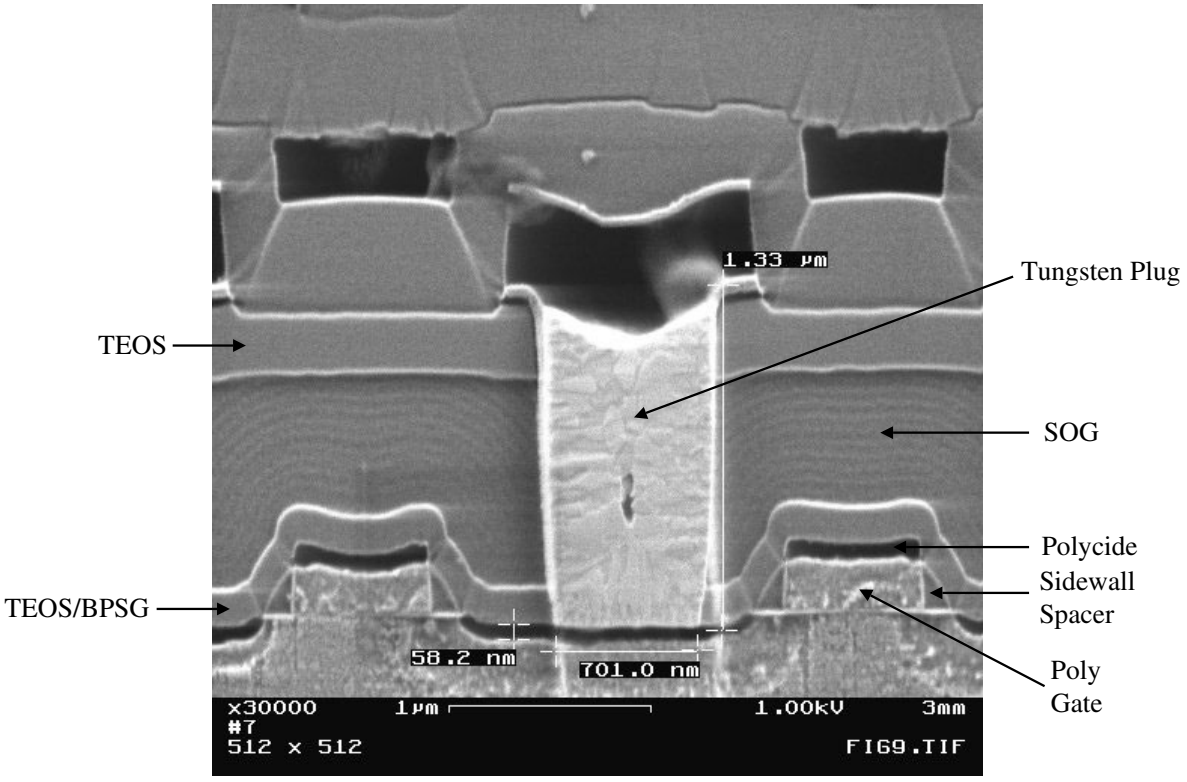

Fig. 2.8-20

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Scanning Electron Microscope Showing Metal Levels and Interconnect

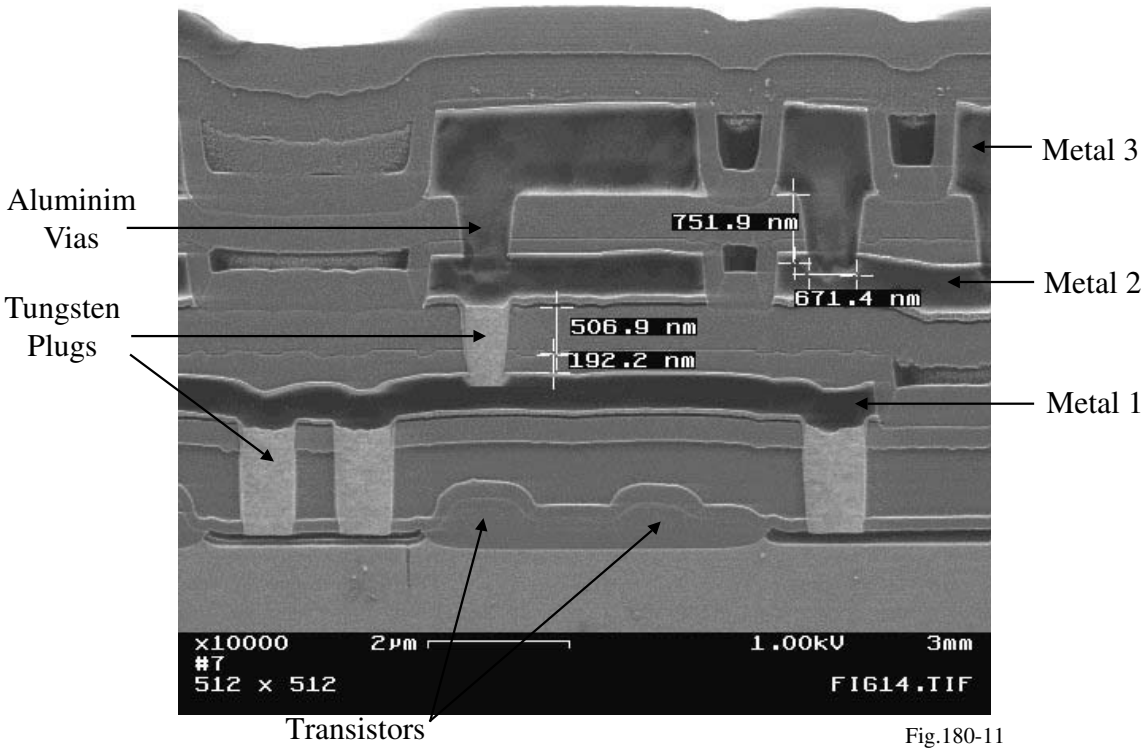

Fig.180-11

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SUMMARY

- Fabrication is the means by which the circuit components, both active and passive, are built as an integrated circuit.
- Basic process steps include:
  1.) Oxide growth 2.) Thermal diffusion 3.) Ion implantation
  4.) Deposition 5.) Etching 6.) Epitaxy
- The complexity of a process can be measured in the terms of the number of masking steps or masks required to implement the process.
- Major Processing Steps for DSM CMOS:
  1.) *p* and *n* wells
  2.) Shallow trench isolation
  3.) Threshold shift
  4.) Thin oxide and gate polysilicon
  5.) Lightly doped drains and sources
  6.) Sidewall spacer
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