EXAMINATION NO. 3

(Average score = 60/100)

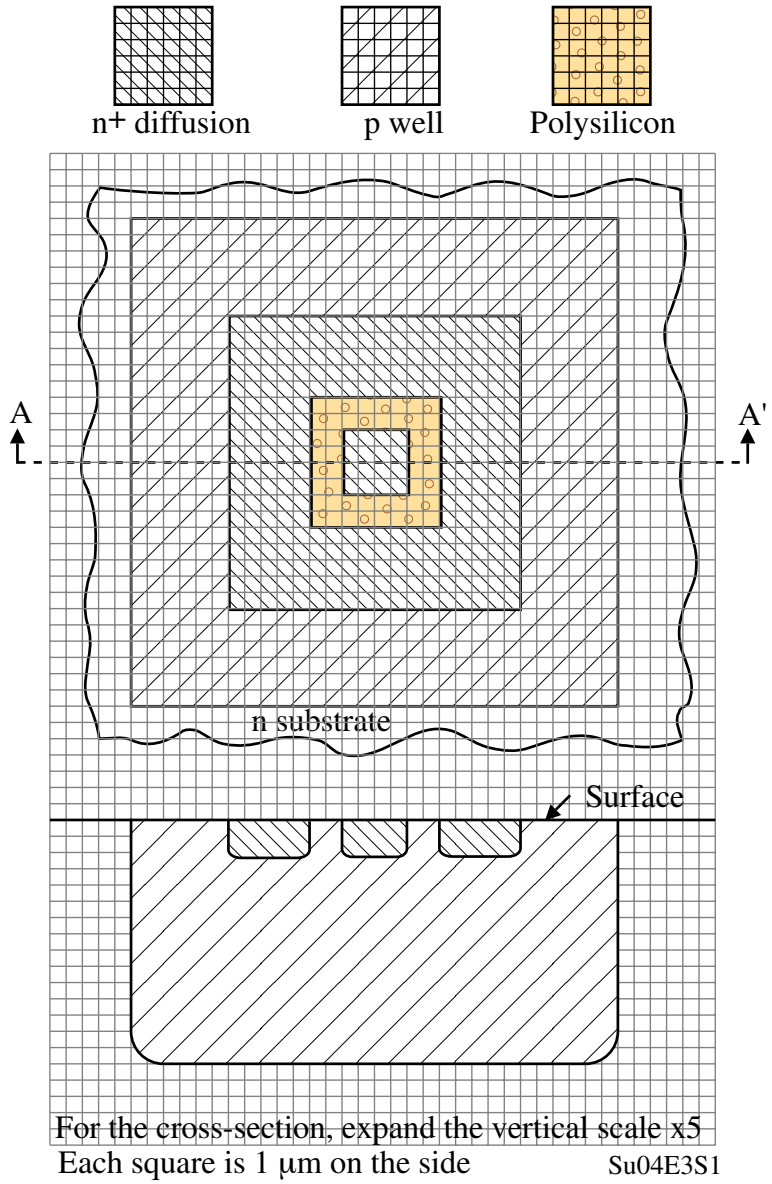
Some process parameters for a typical *p*-well CMOS process.

Physical feature sizes			
T_{ox} (gate oxide thickness)	500	±100	Å
Total lateral diffusion			
n-channel	0.45	±0.15	μm
p-channel	0.6	±0.3	μm
Diffusion depth			
n^+ diffusion	0.45	±0.15	μm
p^+ diffusion	0.6	±0.3	μm
p -well	3.0	±30%	μm
Capacitances			
C_{ox} (gate oxide capacitance, *n*- and *p*-channel)	0.7	±0.1	fF/μm^2
n^+ diffusion to *p*-well (junction, bottom)	0.33	±0.17	fF/μm^2
n^+ diffusion to *p*-well (junction, sidewall)	0.9	±0.45	fF/μm
p^+ diffusion to substrate (junction, bottom)	0.38	±0.12	fF/μm^2
n^+ diffusion to substrate (junction, sidewall)	1.0	±0.5	fF/μm
p-well to substrate (junction, bottom)	0.2	±0.1	fF/μm^2
p-well sidewall (junction, sidewall)	1.6	±1.0	fF/μm
Resistances			
Substrate	25	±20%	Ω-cm
p-well	5000	±2500	Ω/sq.
n^+ diffusion	35	±25	Ω/sq.
p^+ diffusion	80	±55	Ω/sq.
Poly	25	±25%	Ω/sq.
Metal 1 contact to p^+ or n^+ (2μm x 2μm)	4		Ω

Problem 1 - (20 points)

A top view of a npn lateral BJT built in a typical *p*-well CMOS technology is shown. The metal connections have been left out for purposes of clarity. a.) Using the information from the table on the previous page, carefully sketch a cross-section along the indicated line A-A'. Show only the structures that are diffused into the substrate and none of the structures above the substrate. b.) Find the zero-bias depletion capacitors C_{bc0}, C_{be0}, and C_{bs0} using the information on the previous page. c.) If the resistivity of the polysilicon used is $12.5\text{x}10^{-4}$ Ω·cm, what is its thickness?

a.) See plot below.



b.) C_{be0} =

$0.33\text{fF}/\mu\text{m}^2(16\mu\text{m}^2)$

$+0.9\text{fF}/\mu\text{m}(16\mu\text{m})$ =

$5.28\text{fF} + 14.4\text{fF}$

$= \underline{19.7\text{fF}}$

C_{bc0} =

$0.33\text{fF}/\mu\text{m}^2(18^2\mu\text{m}^2 - 8^2\mu\text{m}^2) + 0.9\text{fF}/\mu\text{m}(4\text{x}18\ \mu\text{m} + 4\text{x}8\mu\text{m})$

$= 85.8\text{fF} + 93.6\text{fF}$

$= \underline{179.4\text{fF}}$

C_{bs0} =

$0.2\text{fF}/\mu\text{m}^2(900\mu\text{m}^2)$

$+1.6\text{fF}/\mu\text{m}(120\mu\text{m})$

$= 180\text{fF} + 192\text{fF}$

$= \underline{372\text{fF}}$

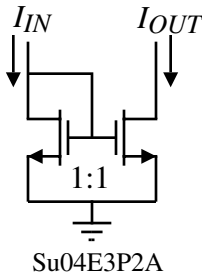
c.) $\frac{\rho}{T} = 25\Omega/\text{sq.}$

$$\therefore T = \frac{\rho}{25\Omega} = \frac{12.5\text{x}10^{-4}}{25\Omega}$$

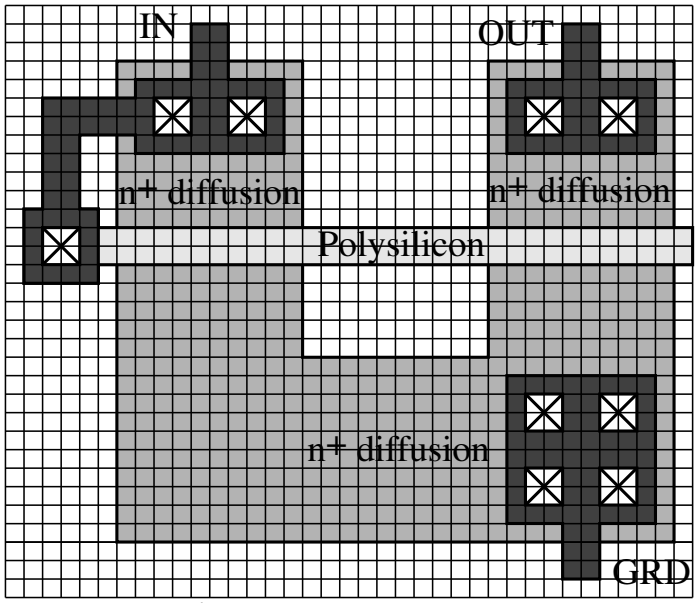
$T = \underline{0.5\mu\text{m}}$

Problem 2 – (20 points)

A CMOS 1:1 current mirror layout is shown. Assuming both transistors are in saturation and that $V_{DS1} = V_{DS2}$. a.) If I_{in} = 100μA, the value of I_{out} should be 100μA. Due to the layout, find the actual value of I_{out}. Use the information in the table for a typical CMOS process on the front page of this exam and assume that K' = 100μA/V^2 and V_T = 0.5V. b.) How would you improve the error caused by the layout?



Su04E3P2A

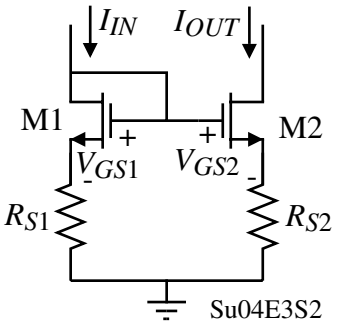


Su04E3P2

a.) We can see from the layout that the source bulk resistances are not equal. Designating these resistors as R_{S1} for M1 and R_{S2} for M2, we can find the values as follows.

$$R_{S1} = 35\Omega/\text{sq.}(0.5 + 0.5 + 1 + 0.2) = 77\Omega \quad \text{and} \quad R_{S2} = 35\Omega/\text{sq.}(0.5 + 0.2) = 24.5\Omega$$

Therefore the current mirror can be modeled as,



Su04E3S2

Thus,

$$\sqrt{\frac{2\cdot 100\mu A}{200\mu A/V^2\cdot 5}} + V_T + 100\mu A(77\Omega)$$

$$= \sqrt{\frac{2\cdot I_{OUT}}{200\mu A/V^2\cdot 5}} + V_T + 24.5\, I_{OUT}$$

Assuming the V_T's cancel, gives

$$0.640156 = 63.2456\sqrt{I_{OUT}} + 24.5\, I_{OUT}$$

or

$$I_{OUT} + 2.58145\sqrt{I_{OUT}} - 0.026129 = 0$$

$$\sqrt{I_{OUT}} = -1.290726 \pm 1.30081 = 0.01008 \quad \rightarrow \quad I_{OUT} = \underline{\underline{102\mu A}}$$

b.) Move the GRD contacts and metal to the left 10 microns so that $R_{S1} = R_{S2}$.

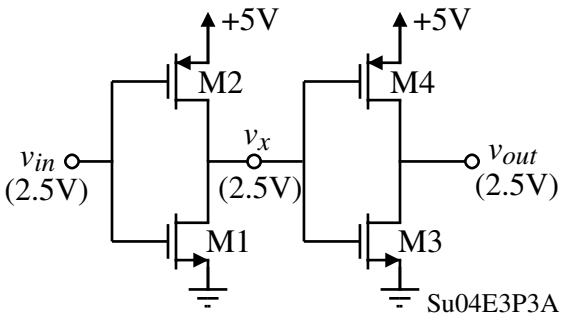
Problem 3 – (15 points)

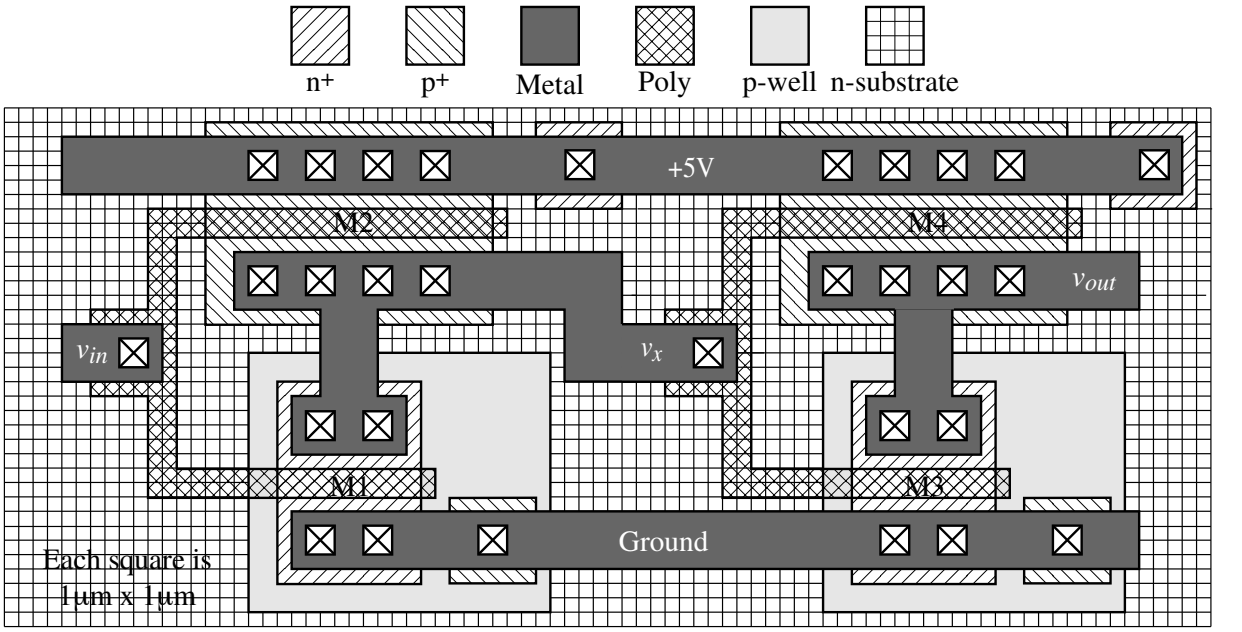
A CMOS inverter is shown along with the top view of the circuit layout assuming a *p*-well CMOS technology. If this inverter is driving and identical inverter with the same layout, find magnitude of the pole at the output of the first inverter (v_x) and the input of the second inverter which is equal to the reciprocal product of the sum of all capacitances connected to this node and the output resistance which is assumed to be 1MΩ. Express this pole magnitude in Hz. Use the table below to calculate the capacitances.

Type	P-Channel	N-Channel	Units
CGSO	220×10^{-12}	220×10^{-12}	F/m
CGDO	220×10^{-12}	220×10^{-12}	F/m
CGBO	700×10^{-12}	700×10^{-12}	F/m
CJ	560×10^{-6}	770×10^{-6}	F/m^2
CJSW	350×10^{-12}	380×10^{-12}	F/m
MJ	0.5	0.5	
MJSW	0.35	0.38	

Based on an oxide thickness of 140 Å or

$Cox = 24.7 \times 10^{-4}$ F/m^2





Su04E3P3B

$\Sigma C_i = C_{gd1} + C_{gd2} + C_{bd1} + C_{bd2} + C_{gs3} + C_{gs4} + C_{gd3} + C_{gd4}$

$C_{gd1} = C_{gd3} = 220\text{x}10^{-12} \cdot 10\text{x}10^{-6} = 2.2\text{fF}$

$C_{gd2} = C_{gd2} = 220\text{x}10^{-12} \cdot 20\text{x}10^{-6} = 4.4\text{fF}$

Next, we must find the area and perimeter of each drain.

AD1 = AD3 = 60μm^2 & PD1 = PD3 = 32μm

AD2 = AD4 = 120μm^2 & PD2 = PD4 = 52μm

Problem 3 – Continued

$$C_{bd1} = \frac{\text{CJ}\cdot\text{AD1}}{\left(1+\frac{2.5\text{V}}{2|\phi\text{F}|}\right)^{\text{MJ}}} + \frac{\text{CJSW}\cdot\text{PD1}}{\left(1+\frac{2.5\text{V}}{2|\phi\text{F}|}\right)^{\text{MJSW}}} = \frac{770\text{x}10^{-6}\cdot 60\text{x}10^{-12}}{\left(1+\frac{2.5\text{V}}{0.8}\right)^{0.5}} + \frac{380\text{x}10^{-12}\cdot 32\text{x}10^{-6}}{\left(1+\frac{2.5\text{V}}{0.8}\right)^{0.38}}$$

$$C_{bd1} = C_{bd3} = 22.75\text{fF} + 7.10\text{fF} = 29.84\text{fF}$$

$$C_{bd2} = \frac{\text{CJ}\cdot\text{AD2}}{\left(1+\frac{2.5\text{V}}{2|\phi_\text{F}|}\right)^{\text{MJ}}} + \frac{\text{CJSW}\cdot\text{PD2}}{\left(1+\frac{2.5\text{V}}{2|\phi_\text{F}|}\right)^{\text{MJSW}}} = \frac{560\text{x}10^{-6}\cdot 120\text{x}10^{-12}}{\left(1+\frac{2.5\text{V}}{0.7}\right)^{0.5}} + \frac{350\text{x}10^{-12}\cdot 52\text{x}10^{-6}}{\left(1+\frac{2.5\text{V}}{0.7}\right)^{0.35}}$$

$$C_{bd2} = C_{bd4} = 31.43\text{fF} + 10.69\text{fF} = 42.12\text{fF}$$

$$C_{gs3} = C_{gd1} + 0.67(C_{ox}\cdot W_3\cdot L_3) = 2.2\text{fF} + 0.67(24.7\text{x}10^{-4}\text{x}20\text{x}10^{-12}) = 35.13\text{fF}$$

$$C_{gs4} = C_{gd2} + 0.67(C_{ox}\cdot W_4\cdot L_4) = 4.4\text{fF} + 0.67(24.7\text{x}10^{-4}\text{x}40\text{x}10^{-12}) = 70.2\text{fF}$$

Now,

$$\Sigma C_i = 2.2\text{fF} + 4.4\text{fF} + 29.84\text{fF} + 42.12\text{fF} + 35.13\text{fF} + 70.2\text{fF} + 2.2\text{fF} + 4.4\text{fF}$$

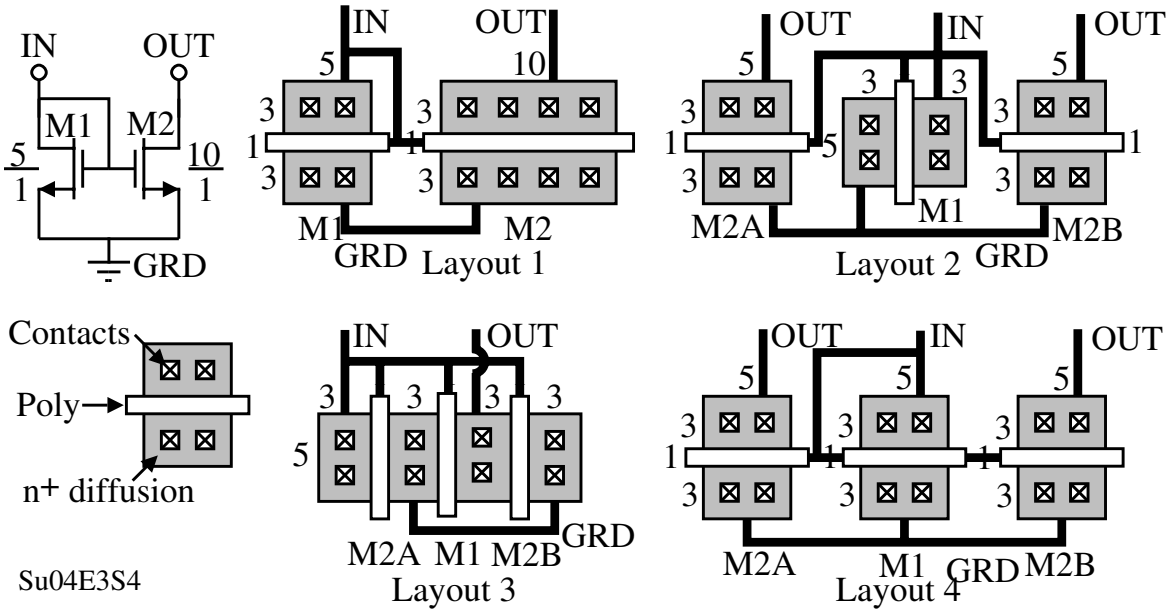
$$= 190.45\text{fF}.$$

$$\therefore \quad |p| = \frac{1}{(\Sigma C_i)}10^6 = \frac{1}{190.45\text{x}10^{-15}10^6} = 5.25\text{x}10^6 \qquad \rightarrow \qquad |p| = \underline{\underline{835.7\text{ kHz}}}$$

Problem 4 – (15 points)

Four different layouts for a CMOS 1:2 current mirror are shown. a.) Show how to connect the n^+ regions and the poly regions to form the current in mirror in each layout. Label the IN, OUT, and GRD nodes. (Just draw a line from the region to wherever to indicate the connection.) b.) Which of the four layouts has the most accurate current gain? Why? c.) Which of the four layouts is has the least accurate current gain from physical parasitic considerations? Why?

a.) See below.



b.) Layout 4 is the most accurate because it uses a common centroid geometry, all gates are oriented in the same direction and it uses the replication principle.

c.) Layout 3 is the least accurate due to physical parasitics. The bulk source resistors of M1 and M2A are different than M2B. Also, the bulk-drain capacitors of M1 and M2B are different than M2A.

Problem 5 – (30 points)

The following questions pertain to a standard npn BJT process.

(3pts) Give the relative doping levels of the emitter, base and collector for the vertical npn transistor.

Emitter doping >> base doping > collector doping

(3pts) Give the relative doping levels of the emitter, base and collector for the lateral pnp transistor.

Emitter doping ≈ Collector doping > base doping

(2pts) How is on vertical npn BJT electrically isolated from another?

By reverse biasing the collector-substrate pn junction

(2pts) What is the purpose of the n^+ buried layer?

To reduce the value of the collector bulk resistance, RC.

(2pts) Why is a p^+ diffusion region used to contact the base?

To form an ohmic contact, otherwise a schottky diode is formed between the metal and the base region.

(2pts) What dimension is important for high β and f_t?

Small base width – the distance from the emitter to the collector

(4pts) Of the parasitic bulk resistances (RE, RB, and RC) for a vertical npn transistor, which is usually the largest? Smallest?

RC is the largest and RE is the smallest

(4pts) Of the depletion capacitors (C_{BE}, C_{BC}, and C_{CS}) for a vertical npn transistor, which is usually the largest? Smallest?

C_{CS} is largest and C_{BE} is the smallest

(4pts) Of the parasitic bulk resistances (RE, RB, and RC) for a lateral pnp transistor, which is usually the largest? Smallest?

RB is the largest and RE is the smallest

(4pts) Of the depletion capacitors (C_{BE}, C_{BC}, and C_{BS}) for a lateral pnp transistor, which is usually the largest? Smallest?

C_{BS} is the largest and C_{BE} is the smallest