EXAMINATION NO. 3

NAME____SCORE________/100

INSTRUCTIONS: This exam is closed text and notes. The exam consists of 5 questions for a total of 100 points. Two pages of handwritten notes are permitted but information such as process data will be reproduced on the exam (you are not permitted to xerox and reduce previous homework or exam questions). Please show your work leading to your answers so that maximum partial credit may be given where appropriate. Be sure to turn in your exam with the problems in numerical order, firmly attached together.

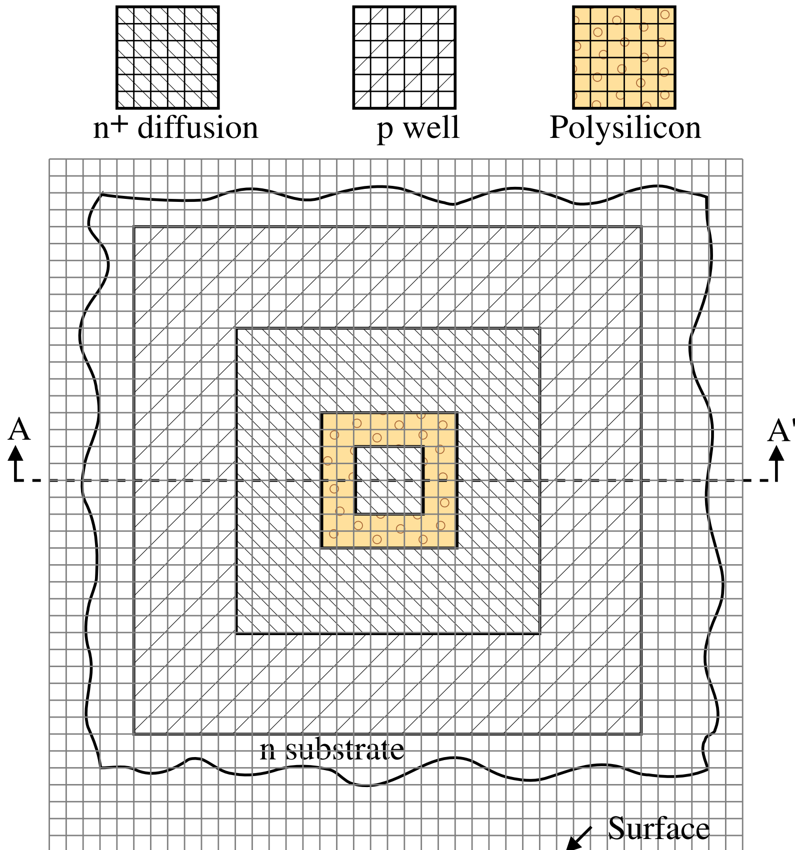
Below are tables with information that may be of use in this exam.

Some process parameters for a typical *p*-well CMOS process.

Physical feature sizes			
T_{ox} (gate oxide thickness)	500	±100	Å
Total lateral diffusion			
n-channel	0.45	±0.15	μm
p-channel	0.6	±0.3	μm
Diffusion depth			
n^+ diffusion	0.45	±0.15	μm
p^+ diffusion	0.6	±0.3	μm
p -well	3.0	±30%	μm
Capacitances			
C_{ox} (gate oxide capacitance, *n*- and *p*-channel)	0.7	±0.1	fF/μm^2
n^+ diffusion to *p*-well (junction, bottom)	0.33	±0.17	fF/μm^2
n^+ diffusion to *p*-well (junction, sidewall)	0.9	±0.45	fF/μm
p^+ diffusion to substrate (junction, bottom)	0.38	±0.12	fF/μm^2
n^+ diffusion to substrate (junction, sidewall)	1.0	±0.5	fF/μm
p-well to substrate (junction, bottom)	0.2	±0.1	fF/μm^2
p-well sidewall (junction, sidewall)	1.6	±1.0	fF/μm
Resistances			
Substrate	25	±20%	Ω-cm
p-well	5000	±2500	Ω/sq.
n^+ diffusion	35	±25	Ω/sq.
p^+ diffusion	80	±55	Ω/sq.
Poly	25	±25%	Ω/sq.
Metal 1 contact to p^+ or n^+ (2μm x 2μm)	4		Ω

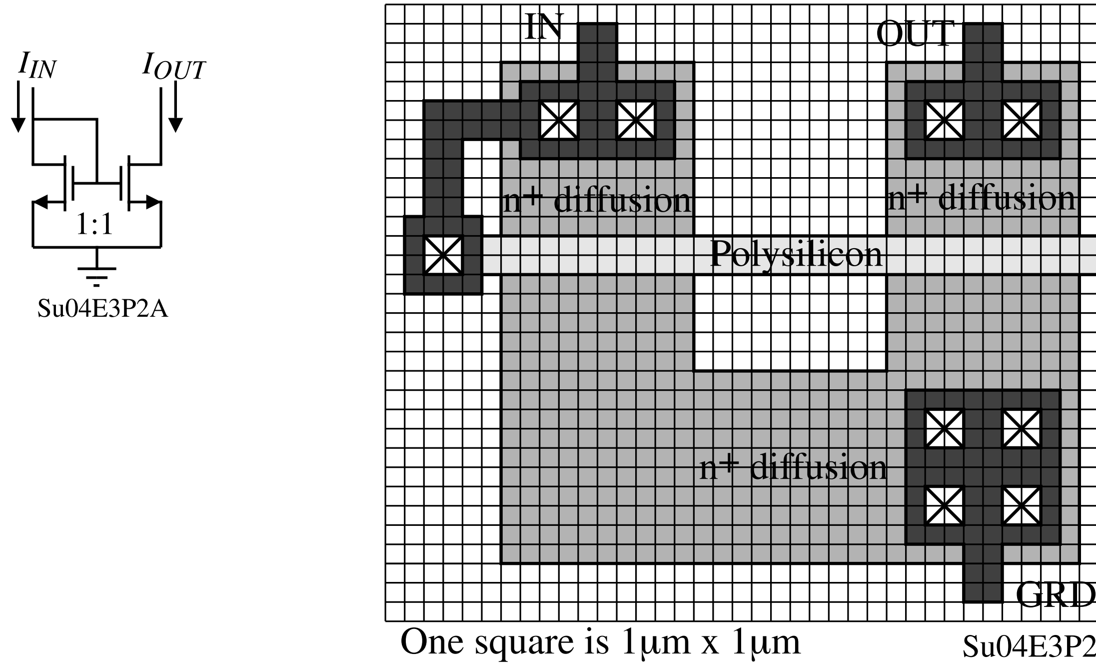
Problem 1 - (20 points)

A top view of a npn lateral BJT built in a typical *p*-well CMOS technology is shown. The metal connections have been left out for purposes of clarity. a.) Using the information from the table on the previous page, carefully sketch a cross-section along the indicated line A-A'. Show only the structures that are diffused into the substrate and none of the structures above the substrate. b.) Find the zero-bias depletion capacitors C_{bc0}, C_{be0}, and C_{bs0} using the information on the previous page. c.) If the resistivity of the polysilicon used is 12.5x10^{-4} Ω·cm, what is its thickness?



Problem 2 – (20 points)

A CMOS 1:1 current mirror layout is shown. Assuming both transistors are in saturation and that $V_{DS1} = V_{DS2}$. a.) If I_{in} = 100µA, the value of I_{out} should be 100µA. Due to the layout, find the actual value of I_{out}. Use the information in the table for a typical CMOS process on the front page of this exam and assume that K' = 100µA/V^2 and V_T = 0.5V. b.) How would you improve the error caused by the layout?



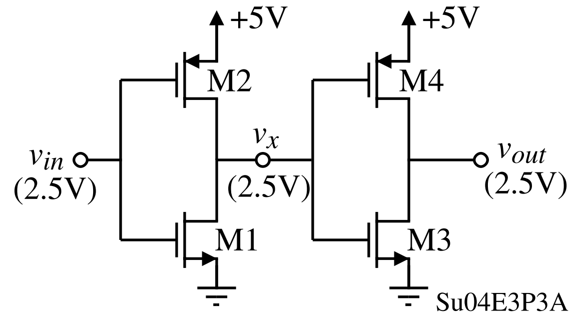
<u>Problem 3 – (15 points)</u>

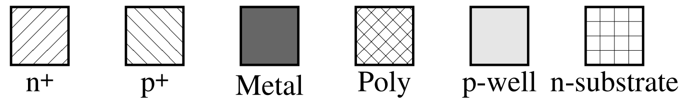
A CMOS inverter is shown along with the top view of the circuit layout assuming a *p*-well CMOS technology. If this inverter is driving and identical inverter with the same layout, find magnitude of the pole at the output of the first inverter (v_x) and the input of the second inverter which is equal to the reciprocal product of the sum of all capacitances connected to this node and the output resistance which is assumed to be 1MΩ. Express this pole magnitude in Hz. Use the table below to calculate the capacitances.

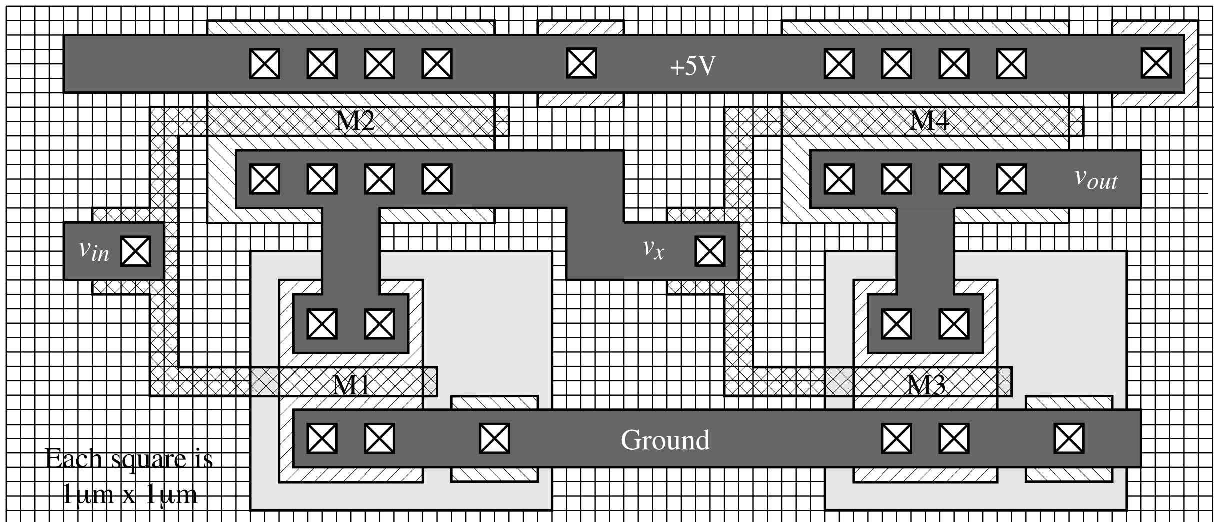
Type	P-Channel	N-Channel	Units
CGSO	220×10^{-12}	220×10^{-12}	F/m
CGDO	220×10^{-12}	220×10^{-12}	F/m
CGBO	700×10^{-12}	700×10^{-12}	F/m
CJ	560×10^{-6}	770×10^{-6}	F/m^2
CJSW	350×10^{-12}	380×10^{-12}	F/m
MJ	0.5	0.5	
MJSW	0.35	0.38	

Based on an oxide thickness of 140 Å or

Cox=24.7×10^{-4} F/m^2







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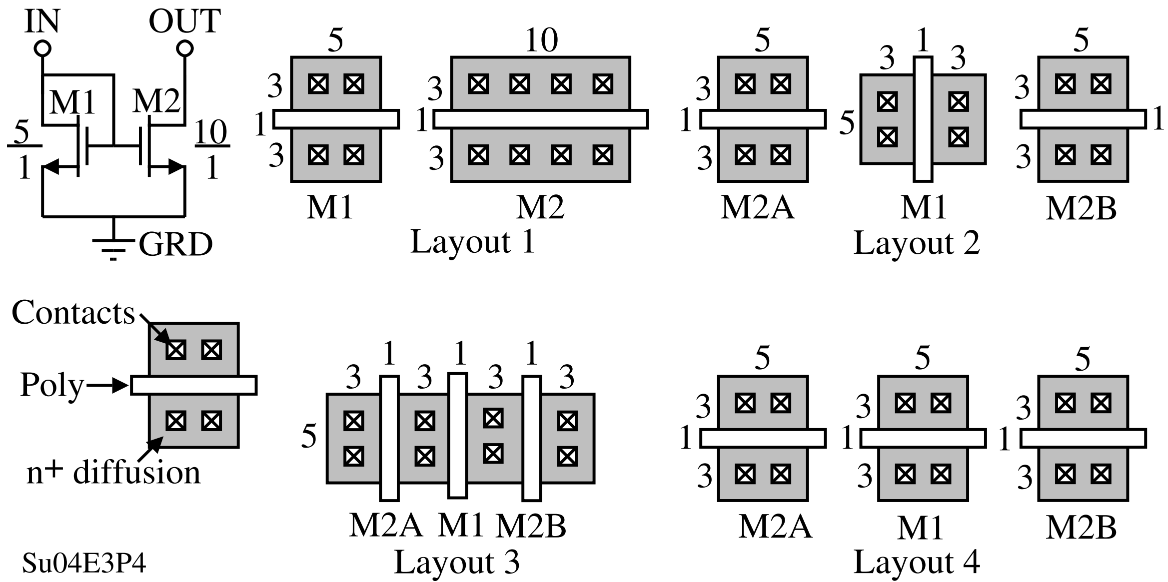
Problem 4 – (15 points)

Four different layouts for a CMOS 1:2 current mirror are shown. a.) Show how to connect the n^+ regions and the poly regions to form the current in mirror in each layout. Label the IN, OUT, and GRD nodes. (Just draw a line from the region to wherever to indicate the connection.) b.) Which of the four layouts has the most accurate current gain? Why? c.) Which of the four layouts is has the least accurate current gain from physical parasitic considerations? Why?



Problem 5 – (30 points)

The following questions pertain to a standard npn BJT process.

(3pts) Give the relative doping levels of the emitter, base and collector for the vertical npn transistor.

(3pts) Give the relative doping levels of the emitter, base and collector for the lateral pnp transistor.

(2pts) How is on vertical npn BJT electrically isolated from another?

(2pts) What is the purpose of the n^+ buried layer?

(2pts) Why is a p^+ diffusion region used to contact the base?

(2pts) What dimension is important for high β and f_t?

(4pts) Of the parasitic bulk resistances (RE, RB, and RC) for a vertical npn transistor, which is usually the largest? Smallest?

(4pts) Of the depletion capacitors (C_{BE}, C_{BC}, and C_{CS}) for a vertical npn transistor, which is usually the largest? Smallest?

(4pts) Of the parasitic bulk resistances (RE, RB, and RC) for a lateral pnp transistor, which is usually the largest? Smallest?

(4pts) Of the depletion capacitors (C_{BE}, C_{BC}, and C_{BS}) for a lateral pnp transistor, which is usually the largest? Smallest?

Extra Sheet