REVIEW FOR EXAMINATION NO.3

Examination No. 3 will be given during the normal class period on Friday, July 16, 2004. It will last for 70 minutes and is closed book. Two pages of handwritten notes are permitted but information such as process data will be reproduced on the exam (you are not permitted to xerox and reduce previous homework or exam questions). The exam will consist of 4 to 5 problems for a total of 100 points. Below is a list of the material for which you are responsible. A straight edge and color pencils are recommended for drawing cross-sections or top views.

IC Technology

- Preparation and definition steps
- Crystal, masking, mask generation, photolithography
- Processing steps: epitaxy, oxidation, etching, diffusion, deposition
- Material characterization: resistivity, sheet resistance, TC, VC
- Familiarity with the cross sections of the MOS and BJT devices - be able to draw roughly to scale and label the various layers
- Purpose of the various layers - Silicon nitride, silicon dioxide, FOX, TOX, IOX, polysilicon, metal, etc.
- Be able to find the parasitic capacitance from a MOSFET or BJT terminal to ground
- Be able to find the bulk resistance between the actual MOSFET or BJT to its external terminals
- Be able to identify a circuit from a layout
- How a passive component is made from MOS or BJT technologies
- Be able to identify the cross-section of a passive component
- Know the typical values and accuracies of passive components
- Purpose and definition of design rules
- Be able to connect the physical aspects of the active and passive components to their performance.

The examples in Lectures 210 and 215 are a good study guide for this exam.

The exam will be proctored by Susanta Sengupta because Dr. Allen will not be in town on the 16th. Office hours for Dr. Allen are Monday 12-1pm and Wednesday 11-12 noon.