# LECTURE 160 – BIPOLAR TECHNOLOGY

## (READING: Text-Sec. 2.4, 2.5)

## INTRODUCTION

### Objective

The objective of this presentation is:

1.) Illustrate the fabrication sequence for a typical bipolar junction transistor

2.) Show the physical aspects of the BJT

### Outline

- *npn* BJT technology
- Compatible *pnp* BJTs
- Modifications to the standard *npn* BJT technology
- Advanced BJT technology
- Summary

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## *npn* BIPOLAR JUNCTION TRANSISTOR TECHNOLOGY

### Major Processing Steps for a Junction Isolated BJT Technology

Start with a *p* substrate.

1. Implantation of the buried $n+$ layer
2. Growth of the epitaxial layer
3. $p+$ isolation diffusion
4. Base *p*-type diffusion
5. Emitter $n+$ diffusion
6. $p+$ ohmic contact
7. Contact etching
8. Metal deposition and etching
9. Passivation and bond pad opening

## Implantation of the Buried Layer (Mask Step 1)

Objective of the buried layer is to reduce the collector resistance.

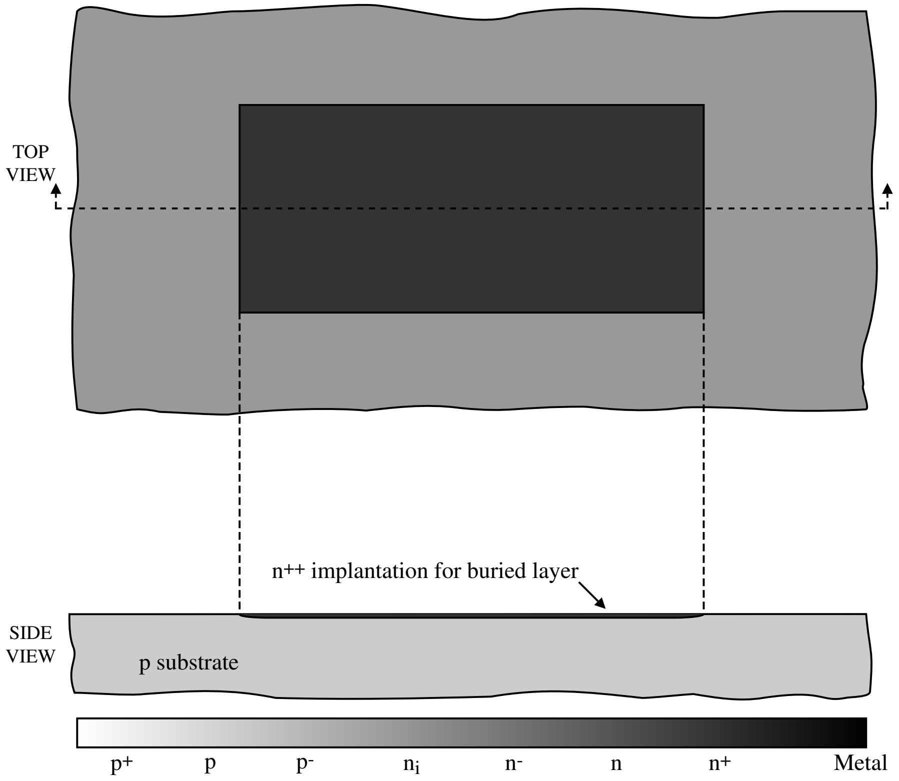

Fig.160-01

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## Epitaxial Layer (No Mask Required)

The objective is to provide the proper *n*-type doping in which to build the *npn* BJT.

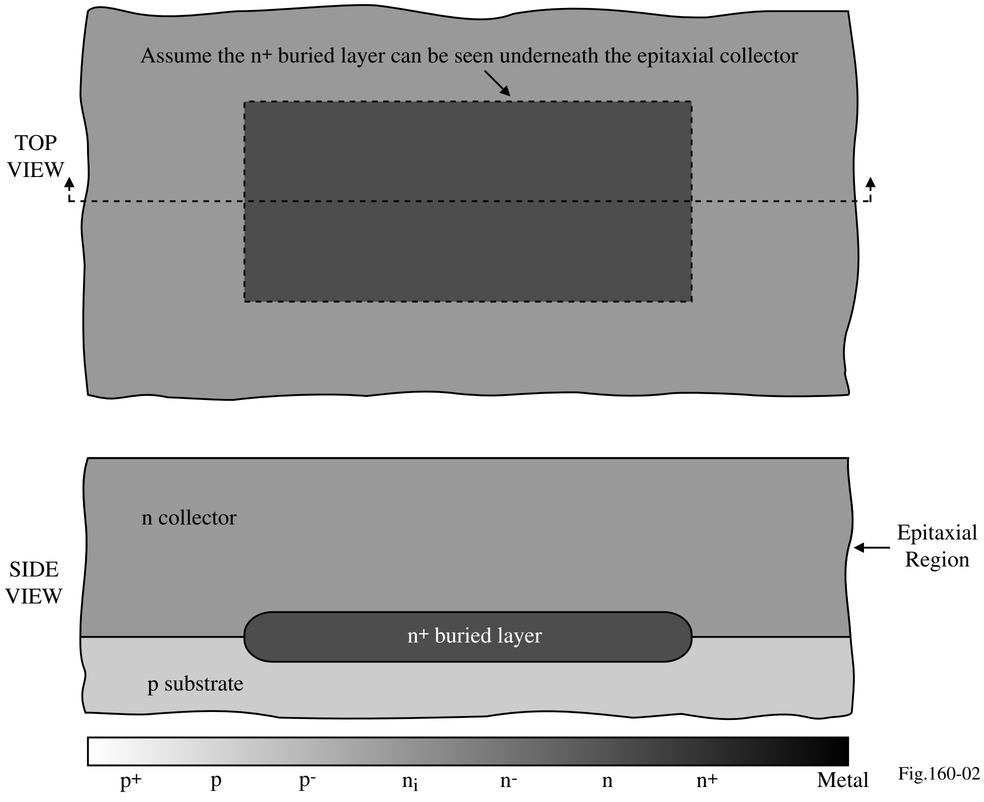

Fig.160-02

## $p^+$ isolation diffusion (Mask Step 2)

The objective of this step is to surround (isolate) the *npn* BJT by a $p^+$ diffusion. These regions also permit contact to the substrate from the surface.

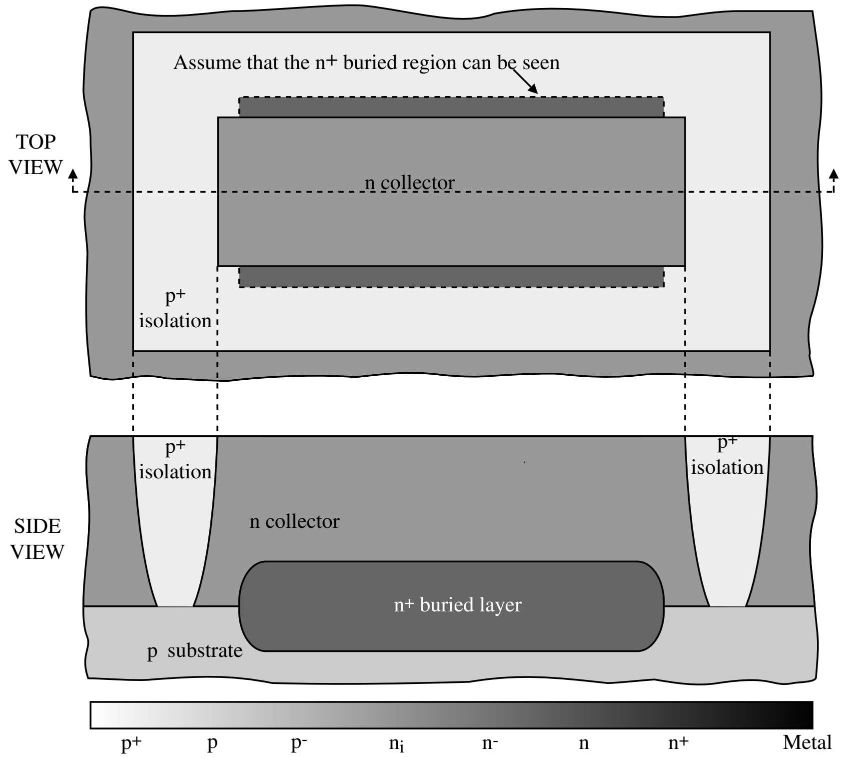

Fig.160-03

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## Base *p*-type diffusion (Mask Step 3)

The step provides the *p*-type base for the *npn* BJT.

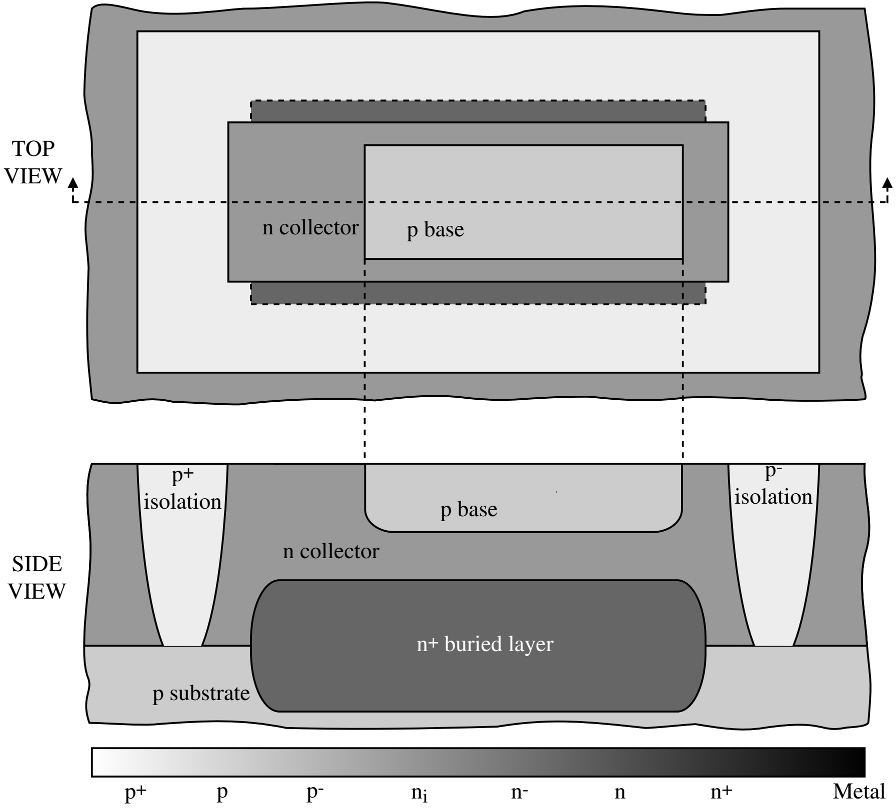

Fig.160-04

## Emitter $n^+$ diffusion (Mask Step 4)

This step implements the $n^+$ emitter of the *npn* BJT and the collector ohmic contact.

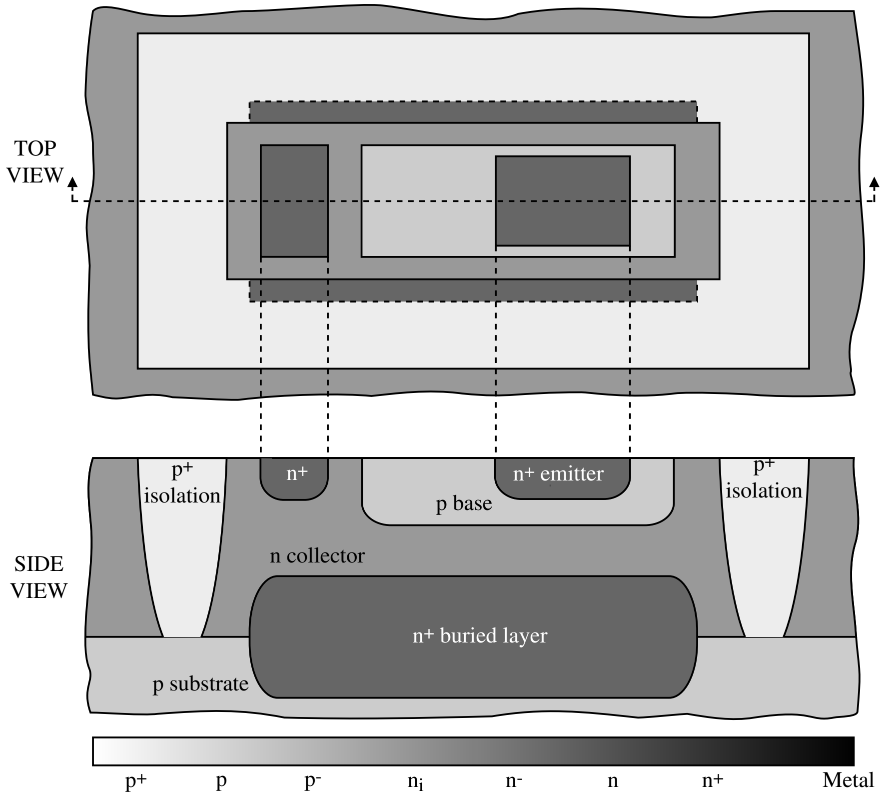

Fig.160-05

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## $p^+$ ohmic contact (Mask Step 5)

This step permits ohmic contact to the base region if it is not doped sufficiently high.

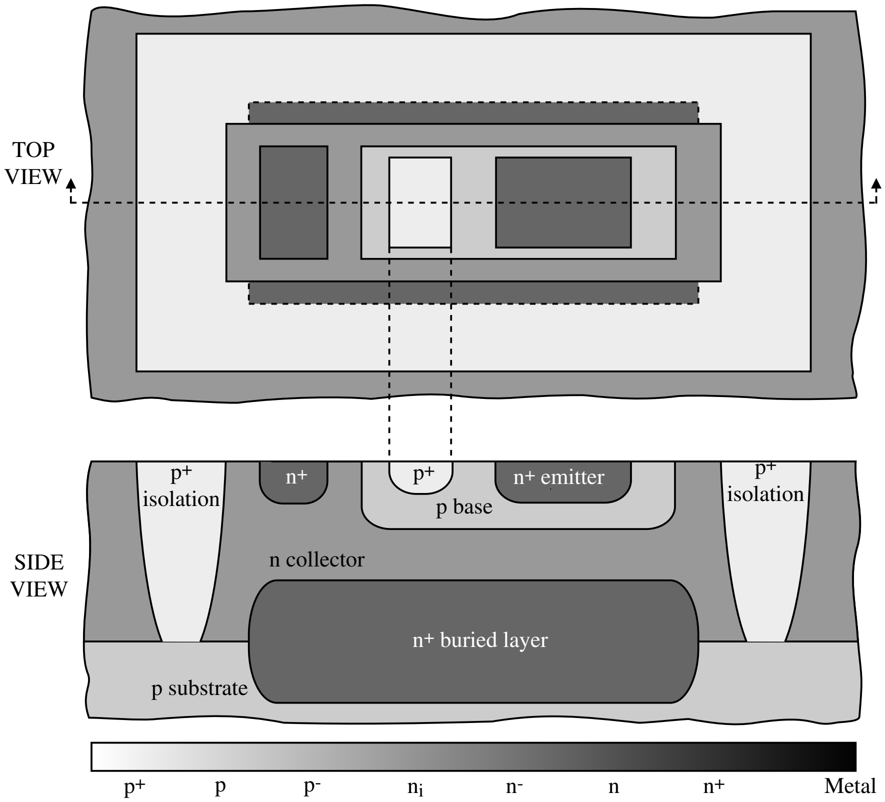

Fig.160-06

## Contact etching (Mask Step 6)

This step opens up the areas in the dielectric area which metal will contact.

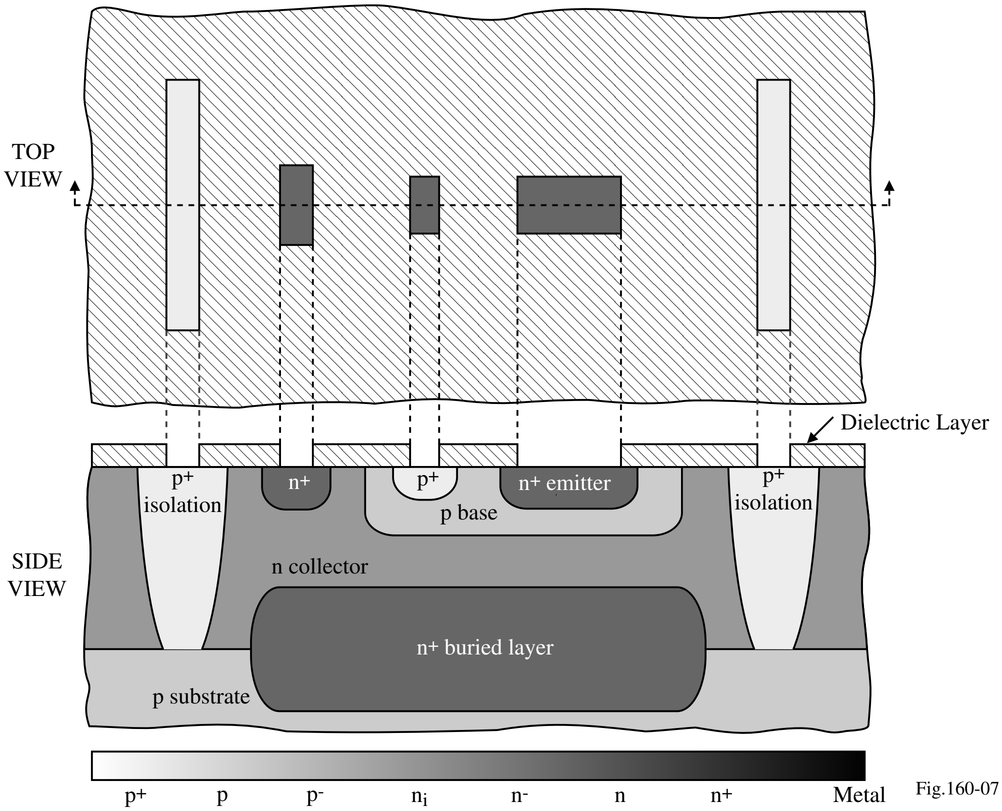

Fig.160-07

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## Metal deposition and etching (Mask Step 7)

In this step, the metal is deposited over the entire wafer and removed where it is not wanted.

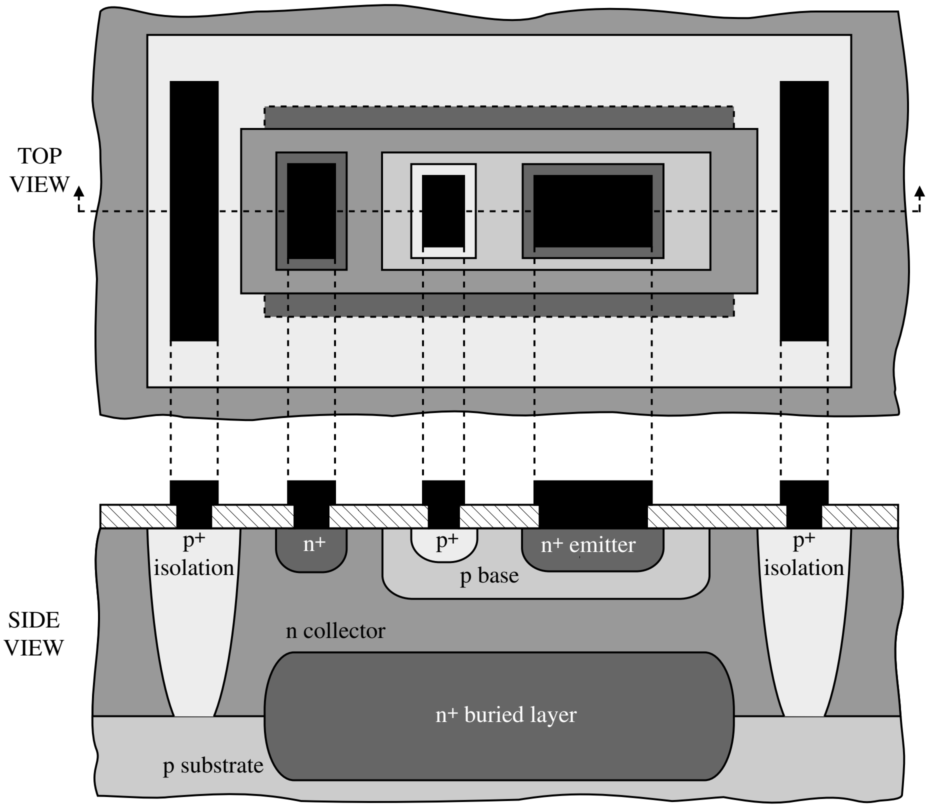

Fig.160-08

## Passivation (Mask Step 8)

Covering the entire wafer with glass and opening the area over bond pads (which requires another mask).

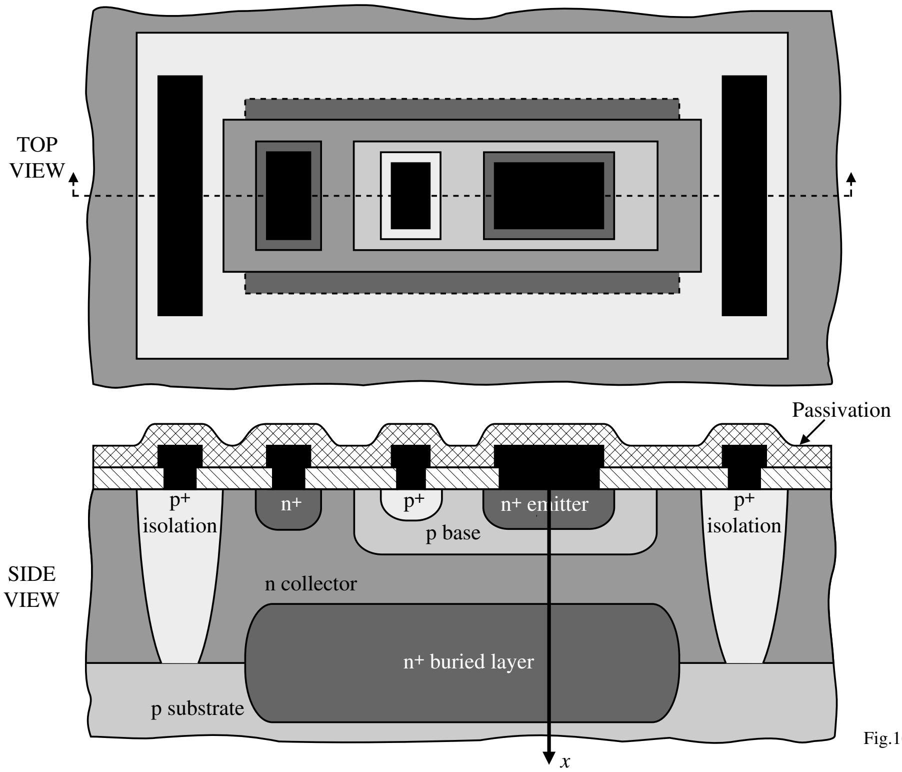

Fig.160-09

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## Typical Impurity Concentration Profile for the *npn* BJT

Taken along the line from the surface indicated in the last slide.

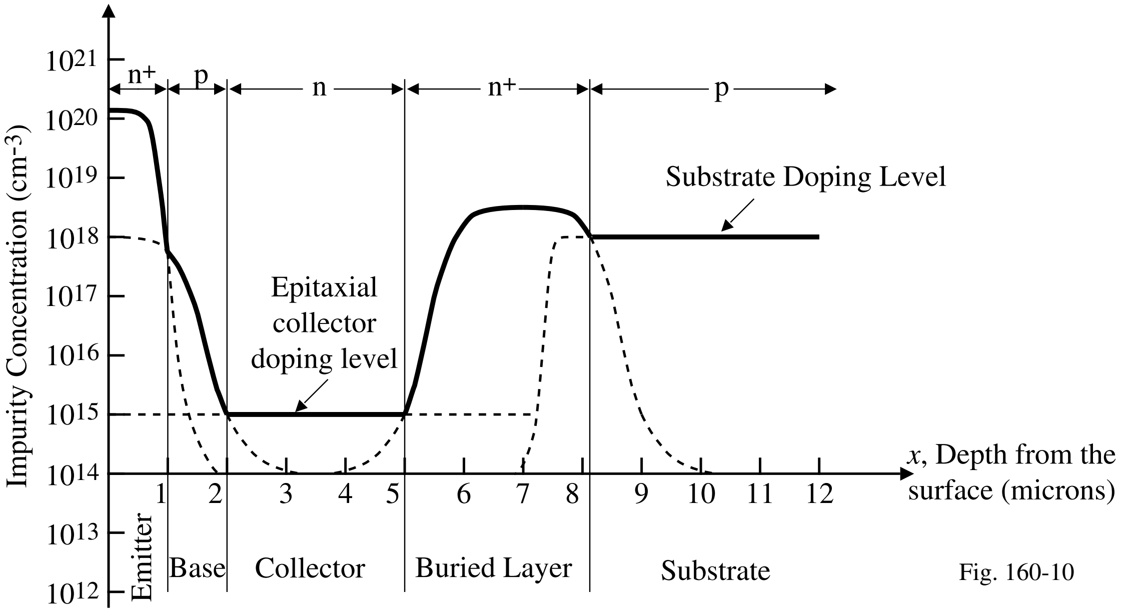

Fig. 160-10

# COMPATIBLE *pnp* BJTS

## Substrate *pnp* BJT

Collector is always connected to the substrate potential which is the most negative DC potential.

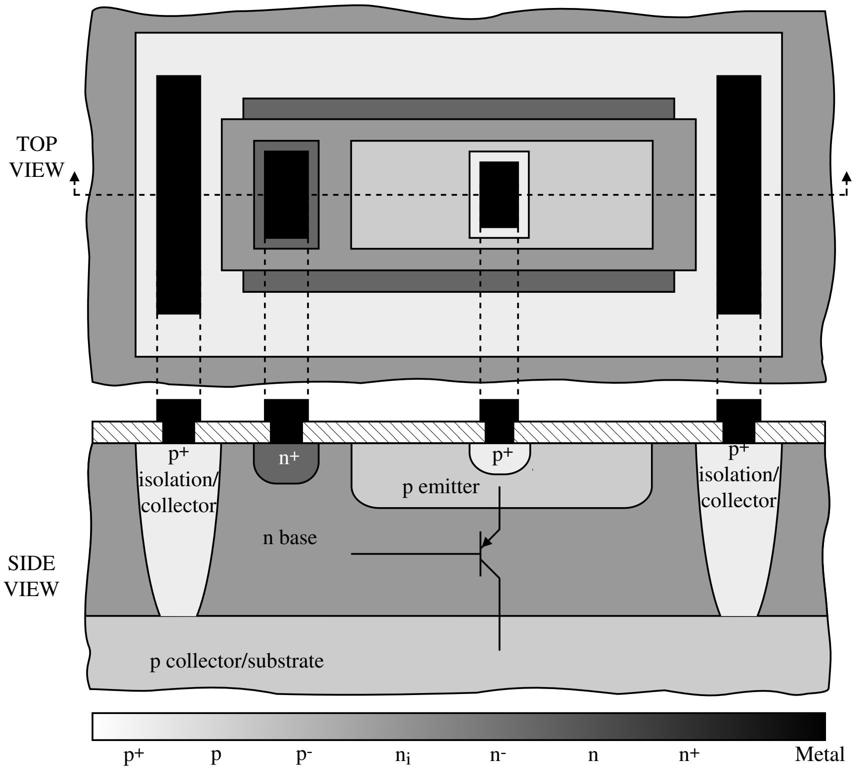

Fig.160-11

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## Lateral *pnp* BJT

Collector is not constrained to a fixed dc potential.

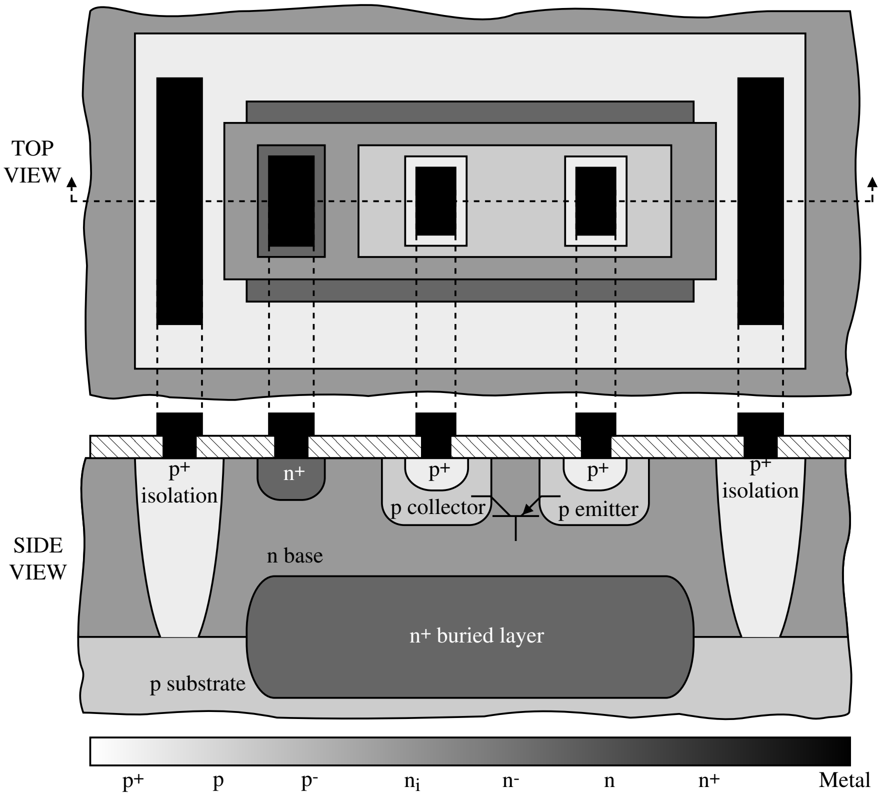

Fig.160-12

# MODIFICATIONS TO THE STANDARD *npn* TECHNOLOGY

## Types of Modifications

1.) Dielectric isolation - Isolation of the transistor from the substrate using an oxide layer.

2.) Double diffusion - A second, deeper n+ emitter diffusion is used to create JFETs.

3.) Ion implanted JFETs - Use of an ion implantation to create the upper gate of a p-channel JFET

4.) Superbeta transistors - Use of a very thin base width to achieve higher values of $\beta_F$.

5.) Double diffused *pnp* BJT - Double diffusion is used to build a vertical *pnp* transistor whose performance more closely approaches that of the *npn* BJT.

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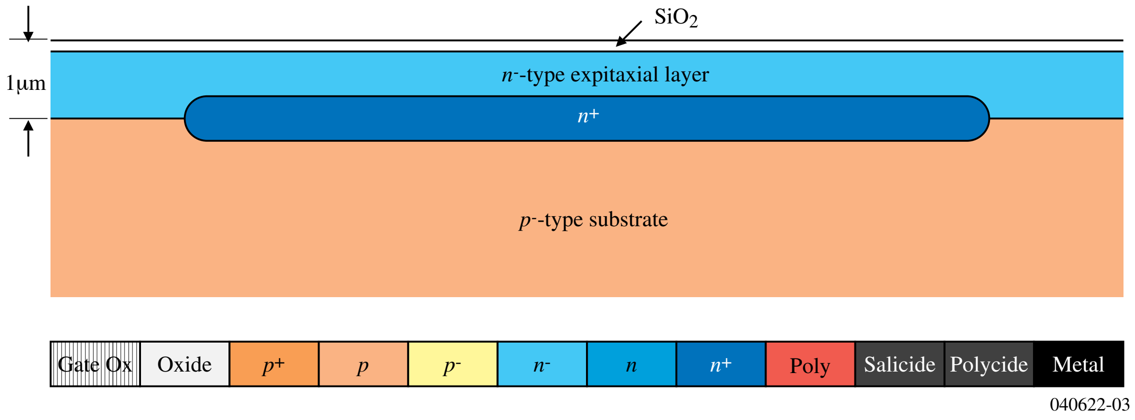
# ADVANCED BIPOLAR IC TECHNOLOGY

## Objective

Newer BJT technologies use polysilicon to form a self-aligned emitter resulting in higher frequency response capability. These technologies attempt to keep the surface of the integrated circuit as flat as possible.

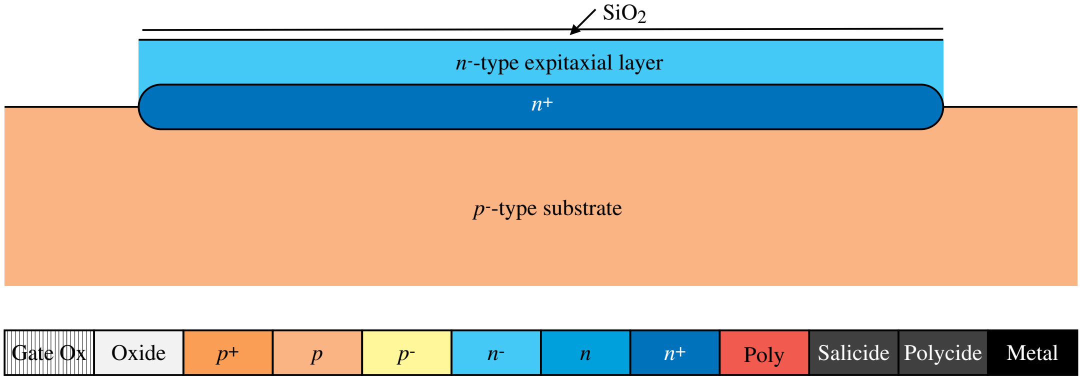
## Process

1.) Buried layer and epitaxial growth.



## Process – Continued

2.) Etching of epitaxial layer.



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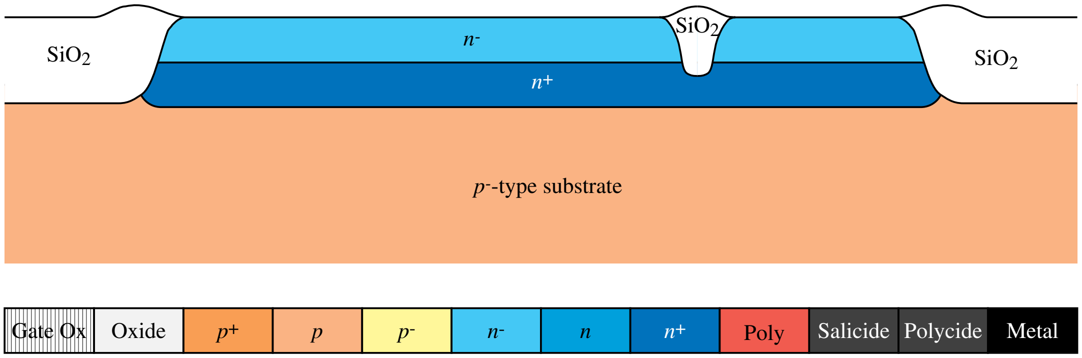
3.) Growth of thick SiO$_2$.



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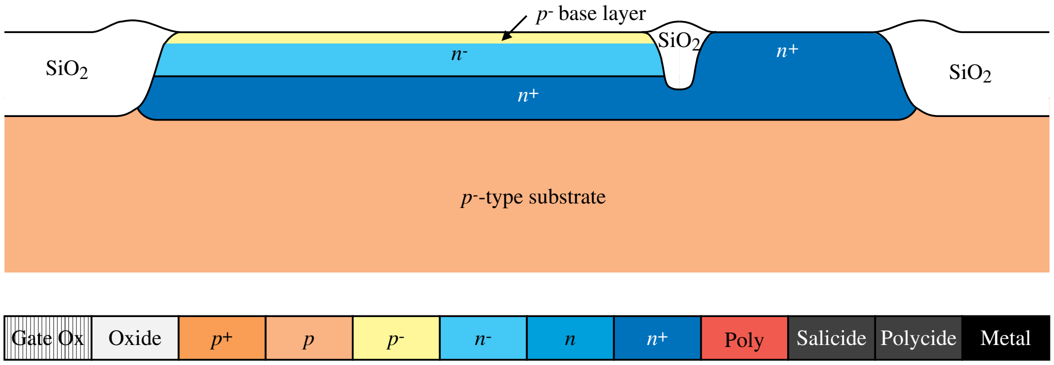
## Process – Continued

4.) Base diffusion and collector sinker ($n^+$ diffusion)



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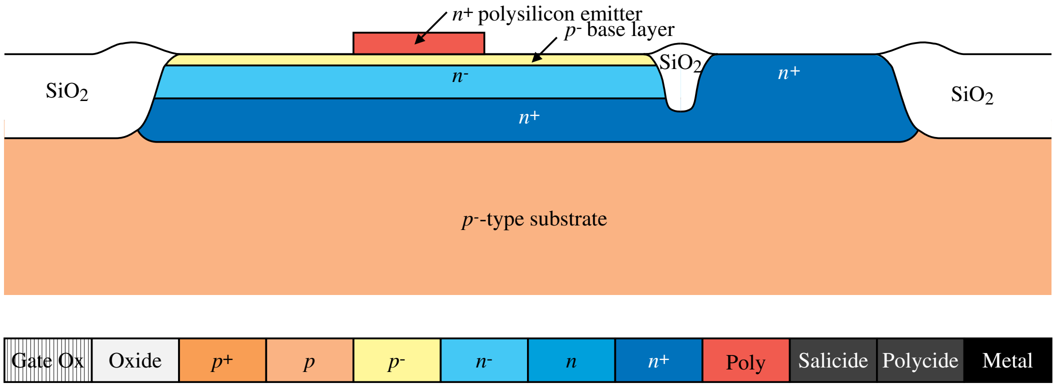
5.) $n^+$ polysilicon emitter



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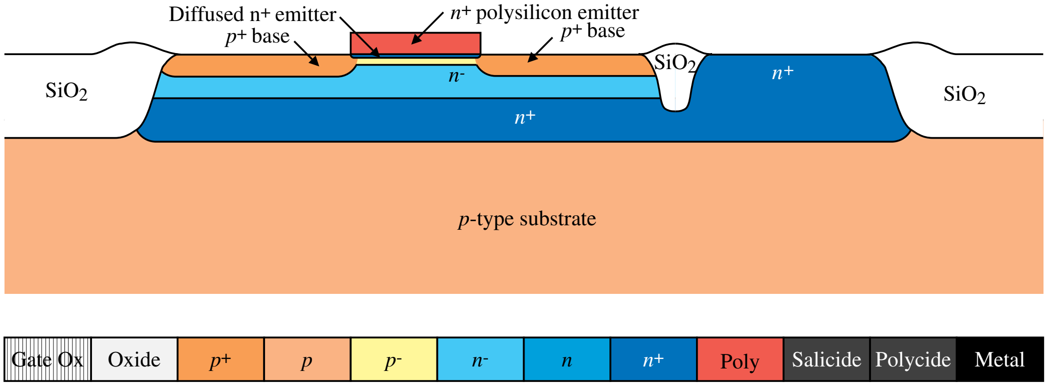
## Process – Continued

6.) $p^+$ base diffusion



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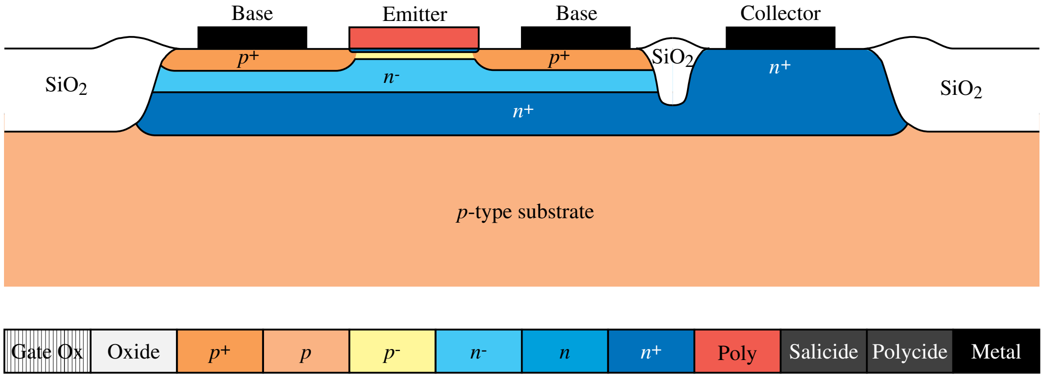
7.) Metal contacts



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## SUMMARY

The objective has been to give a physical understanding of how the *npn* BJT is fabricated.

- The fabrication sequence for a typical *npn* BJT has been illustrated
- Methods of implementing other active devices in the *npn* BJT technology were shown.
- Simple *npn* BJT technology chooses to emphasize the *npn* over the *pnp* because the *npn* BJT performance is always superior to the *pnp* BJT performance. Thus, the philosophy in design is to use the *npn* where ever possible and incorporate the *pnp* only where it has to be used.
- An advanced BJT technology has been illustrated.

We will examine the passive components that can be implemented in a typical *npn* BJT process later.