LECTURE 180 – CMOS TECHNOLOGY

(READING: Text-Sec. 2.8)

INTRODUCTION

Objective

The objective of this presentation is:

1.) Illustrate the fabrication sequence for a typical MOS transistor

2.) Show the physical aspects of the MOSFET

Outline

- CMOS technology
- Summary

CMOS TECHNOLOGY

Fabrication

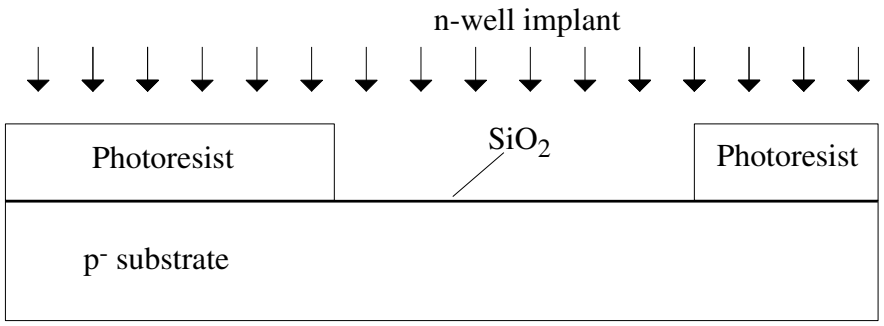
Fabrication involves the implementation of semiconductor processes to build a MOSFET transistor and compatible passive components as an integrated circuit.

N-Well CMOS Fabrication Major Steps

1.) Implant and diffuse the n-well
2.) Deposition of silicon nitride
3.) n-type field (channel stop) implant
4.) p-type field (channel stop) implant
5.) Grow a thick field oxide (FOX)
6.) Grow a thin oxide and deposit polysilicon
7.) Remove poly and form LDD spacers
8.) Implantation of NMOS S/D and n-material contacts
9.) Remove spacers and implant NMOS LDDs
10.) Repeat steps 8.) and 9.) for PMOS
11.) Anneal to activate the implanted ions
12.) Deposit a thick oxide layer (BPSG - borophosphosilicate glass)
13.) Open contacts, deposit first level metal and etch unwanted metal
14.) Deposit another interlayer dielectric (CVD SiO_2), open vias and deposit second level metal
15.) Etch unwanted metal, deposit a passivation layer and open over bonding pads

Major CMOS Process Steps

Step 1 - Implantation and diffusion of the n-wells



Step 2 - Growth of thin oxide and deposition of silicon nitride

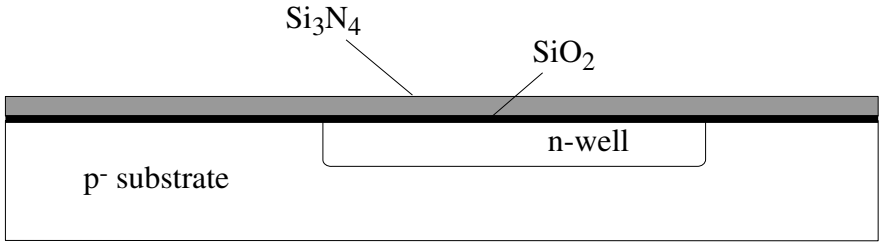
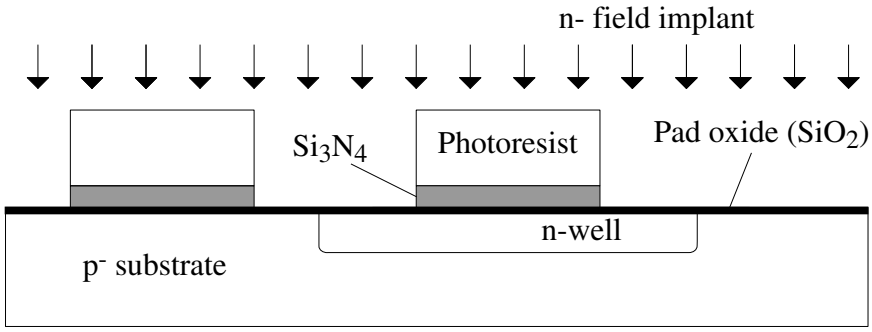


Fig. 180-01

Major CMOS Process Steps - Continued

Step 3.) Implantation of the n-type field channel stop



Step 4.) Implantation of the p-type field channel stop

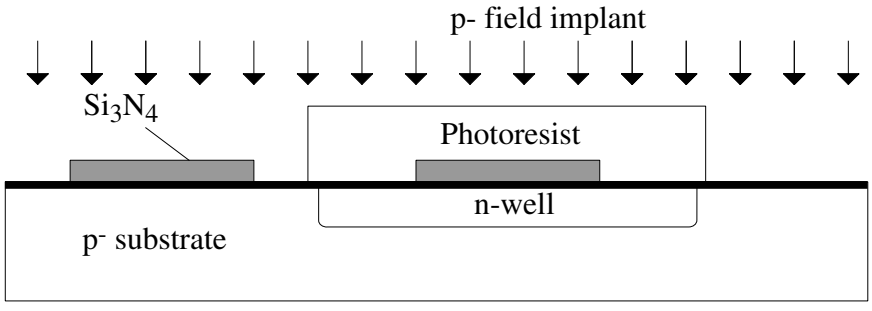
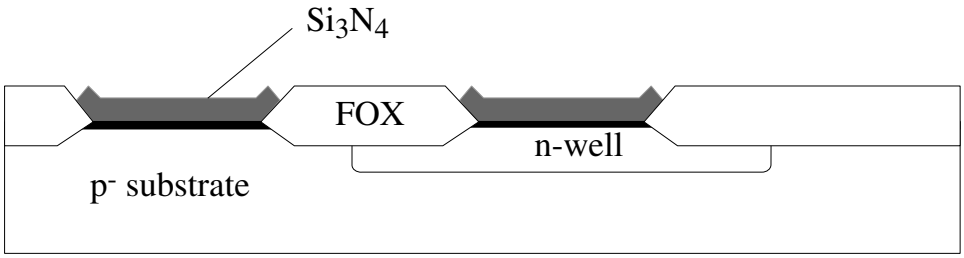


Fig. 180-02

Major CMOS Process Steps – Continued

Step 5.) Growth of the thick field oxide (LOCOS - *loc*alized *o*xidation of *s*ilicon)



Step 6.) Growth of the gate thin oxide and deposition of polysilicon

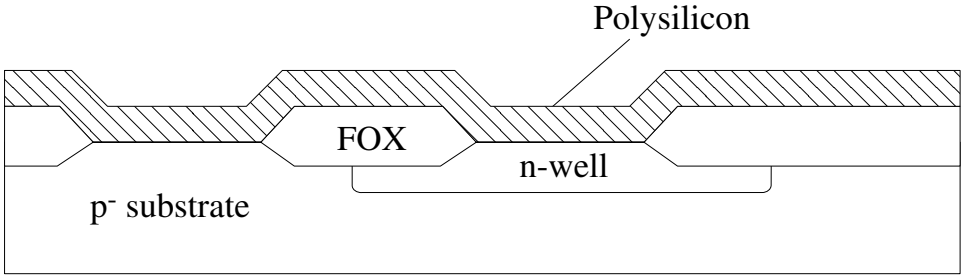
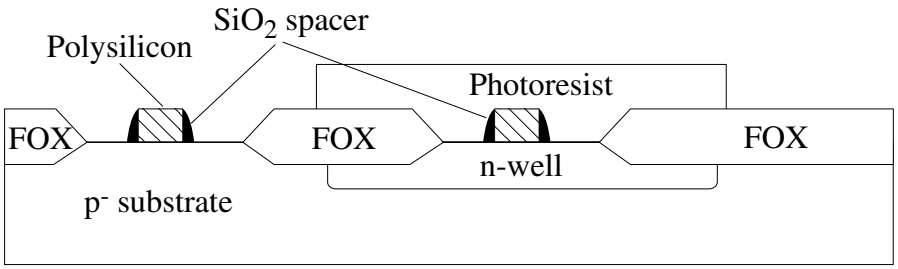


Fig. 180-03

Major CMOS Process Steps - Continued

Step 7.) Removal of polysilicon and formation of the sidewall spacers



Step 8.) Implantation of NMOS source and drain and contact to n-well (not shown)

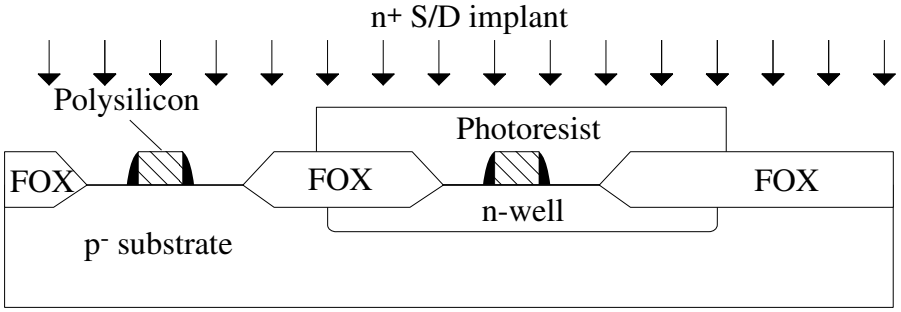
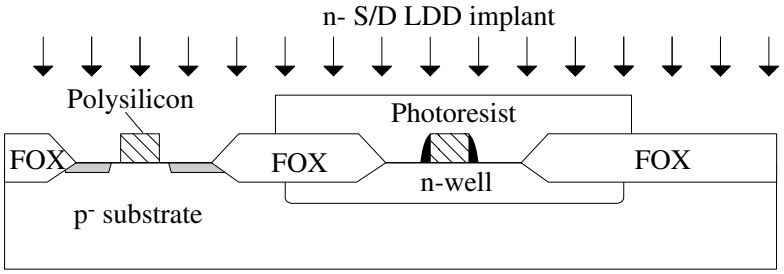


Fig. 180-04

Major CMOS Process Steps - Continued

Step 9.) Remove sidewall spacers and implant the NMOS lightly doped source/drains



Step 10.) Implant the PMOS source/drains and contacts to the p- substrate (not shown), remove the sidewall spacers and implant the PMOS lightly doped source/drains

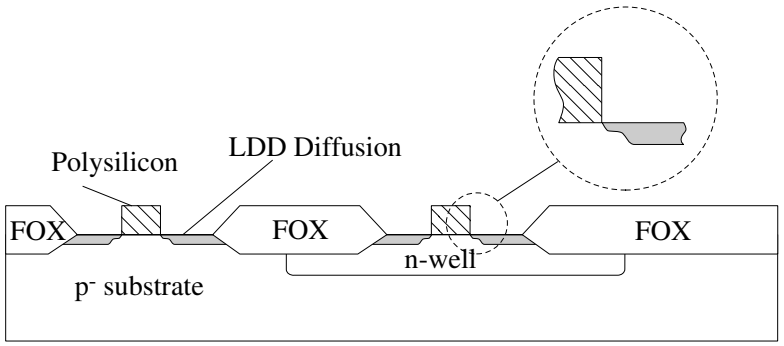
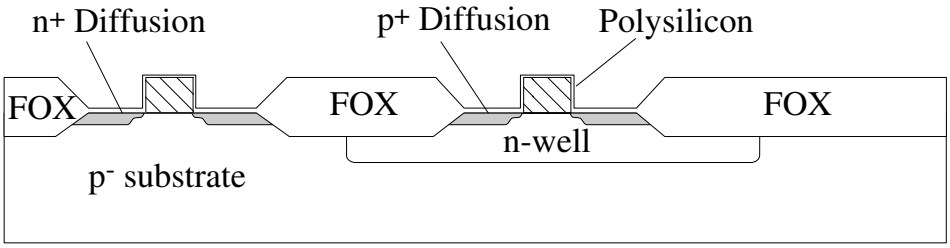


Fig. 180-05

Major CMOS Process Steps – Continued

Step 11.) Anneal to activate the implanted ions



Step 12.) Deposit a thick oxide layer (BPSG - borophosphosilicate glass)

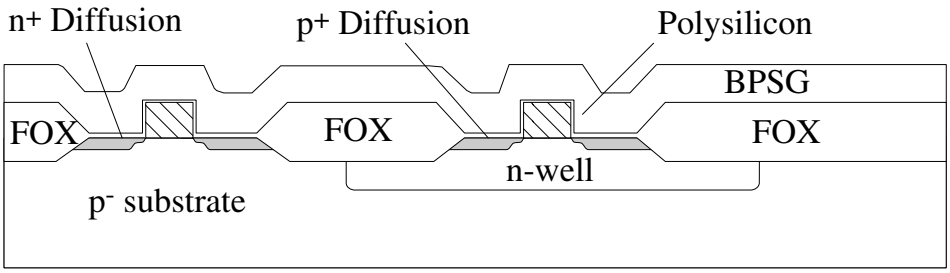
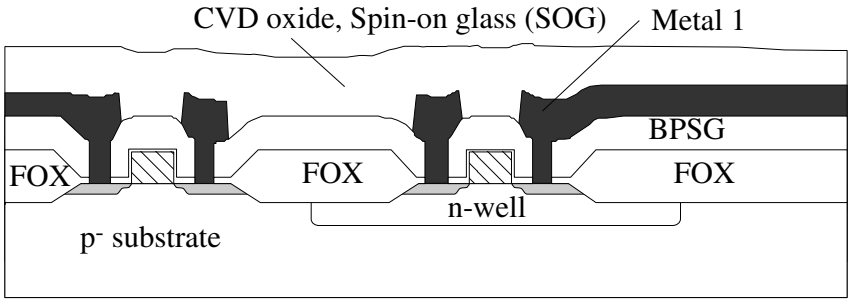


Fig. 180-06

Major CMOS Process Steps - Continued

Step 13.) Open contacts, deposit first level metal and etch unwanted metal



Step 14.) Deposit another interlayer dielectric (CVD SiO_2), open contacts, deposit second level metall

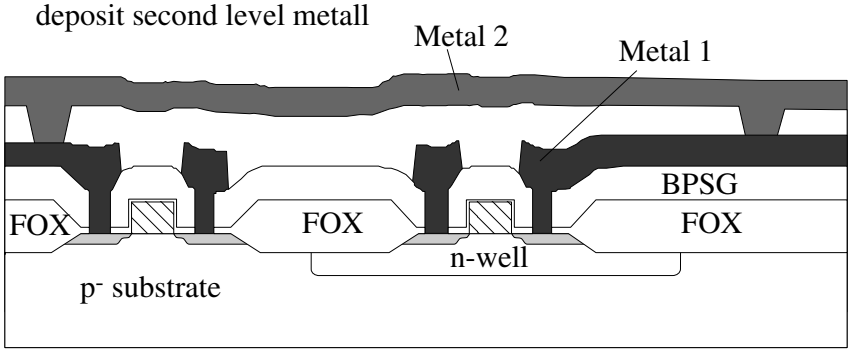


Fig. 180-07

Major CMOS Process Steps – Continued

Step 15.) Etch unwanted metal and deposit a passivation layer and open over bonding pads

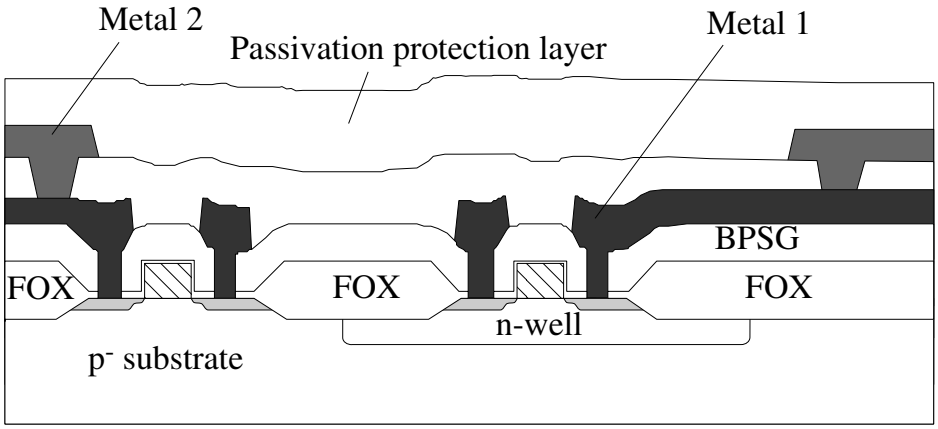


Fig. 180-08

p-well process is similar but starts with a p-well implant rather than an n-well implant.

Approximate Side View of CMOS Fabrication

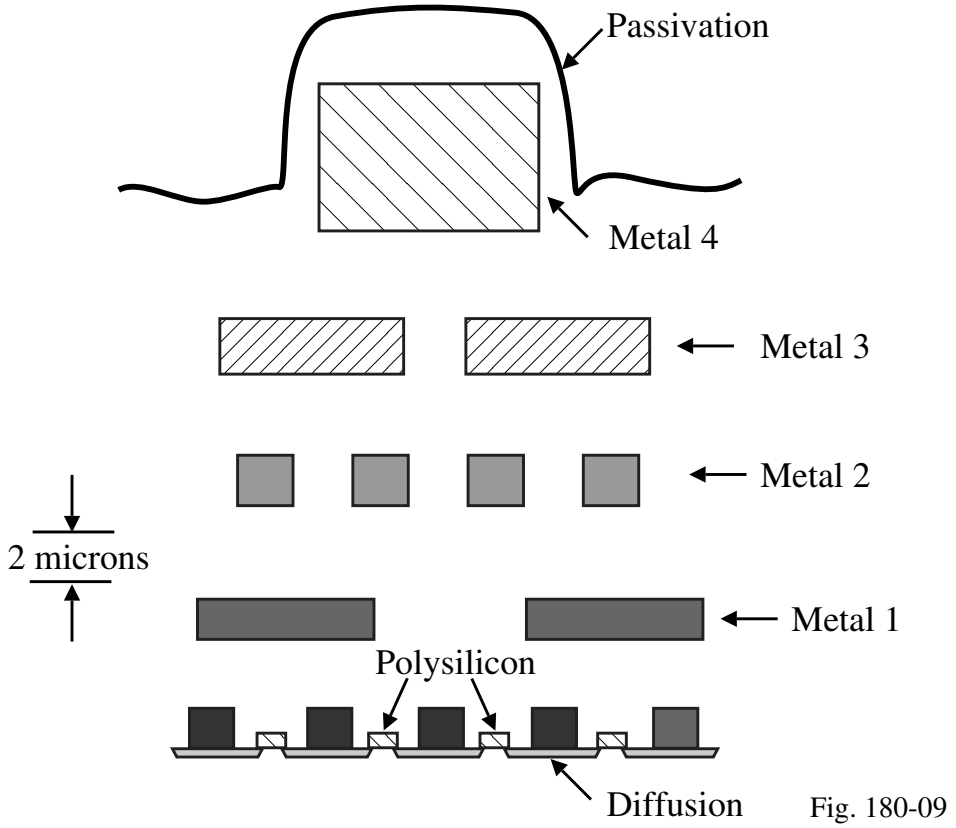
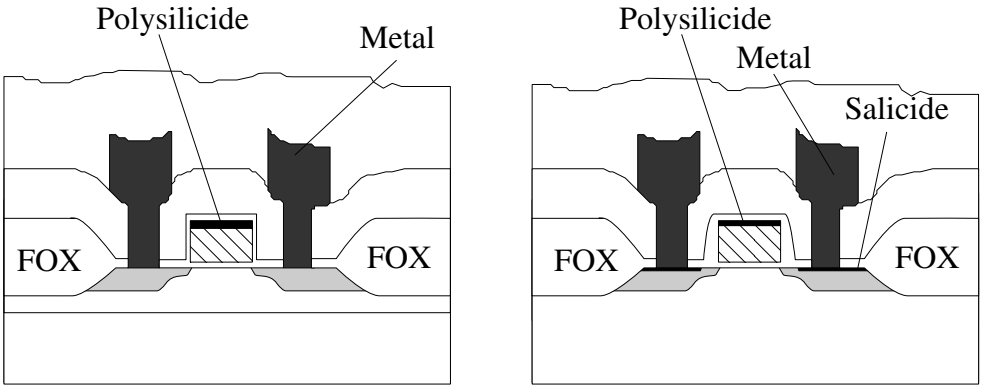


Fig. 180-09

Silicide/Salicide Technology

Used to reduce interconnect resistivity by placing a low-resistance silicide such as $TiSi_2$, WSi_2, $TaSi_2$, etc. on top of polysilicon

Salicide technology (self-aligned silicide) provides low resistance source/drain connections as well as low-resistance polysilicon.



Polycide structure Salicide structure

Fig 180-10

Scanning Electron Microscope of a MOSFET Cross-section

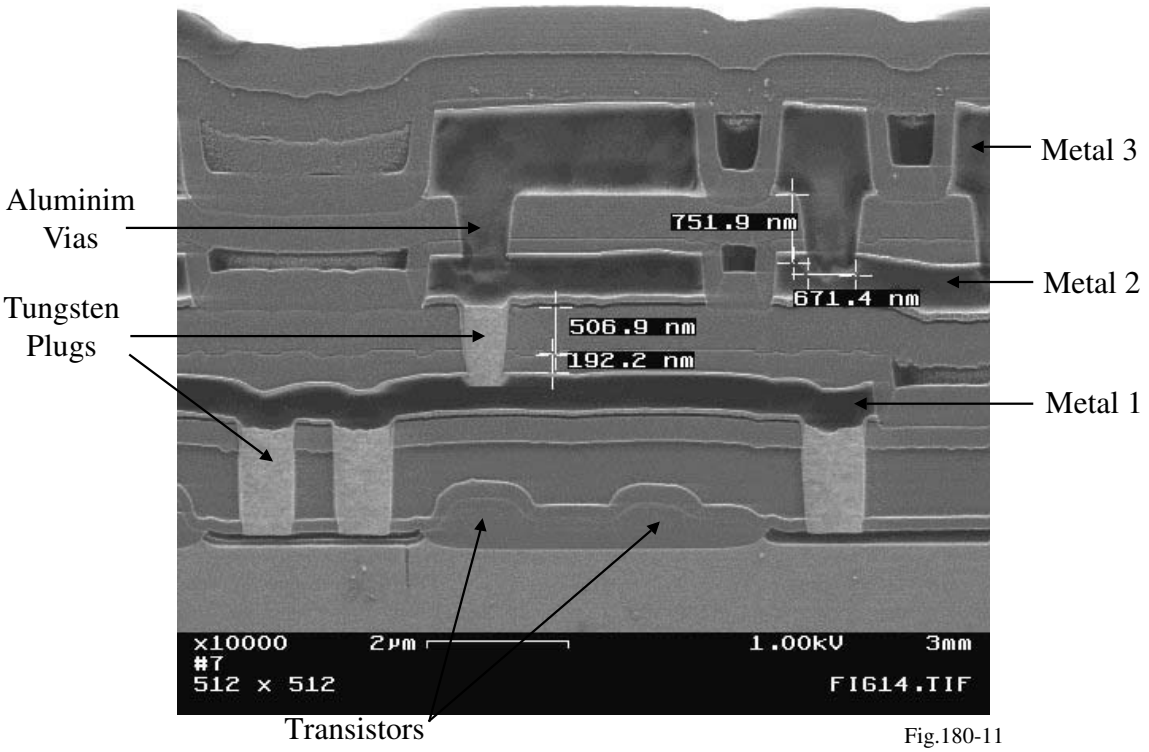


Fig.180-11

SUMMARY

Major CMOS Processing Steps

1.) Well definition
2.) Definition of active areas and substrate/well contacts (SiNi3)
3.) Thick field oxide (FOX)
4.) Thin field oxide and polysilicon
5.) Diffusion of the source and drains (includes the LDD)
6.) Dielectric layer/Contacts
7.) Metallization
8.) Dielectric layer/Vias
9.) Metallization
10.) Passivation
11.) Bond pad openings

