LECTURE 190 – CMOS TECHNOLOGY-COMPATIBLE DEVICES

(READING: Text-Sec. 2.9)

INTRODUCTION

Objective

The objective of this presentation is examine devices that are compatible with CMOS technology

Outline

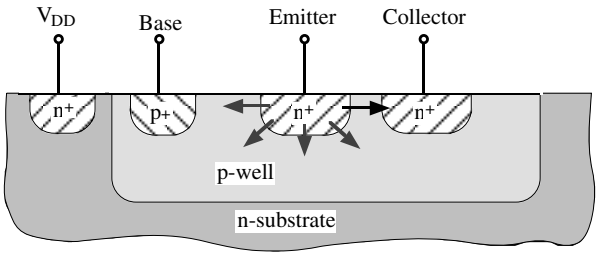
- Compatible active devices – the BJT lateral transistor
- Latchup and ESD
- Temperature and noise characteristics
- Summary

COMPATIBLE ACTIVE DEVICES

Lateral Bipolar Junction Transistor

P-Well Process

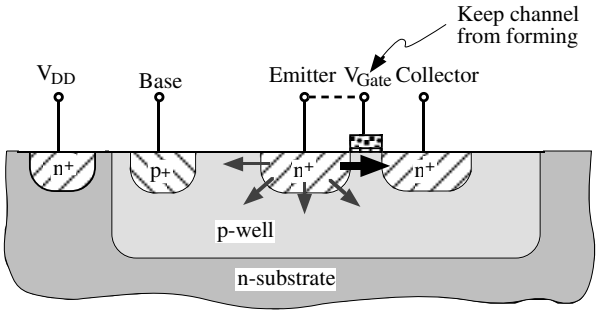
NPN Lateral-



Lateral Bipolar Junction Transistor - Continued

Field-aided Lateral-

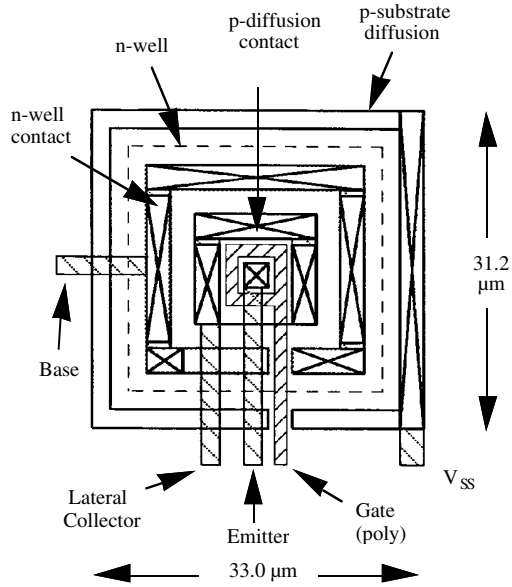
$ß_F \approx 50$ to 100 depending on the process



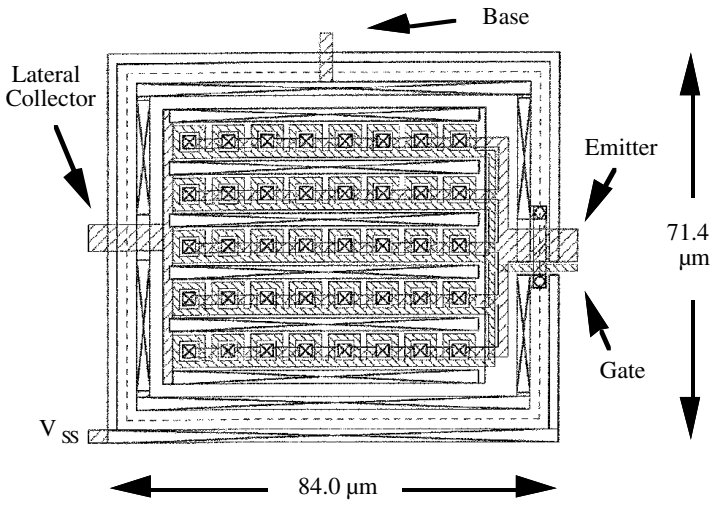
- Good geometry matching
- Low 1/f noise (if channel doesn't form)
- Acts like a photodetector with good efficiency

Geometry of the Lateral PNP BJT

Minimum Size layout of a single emitter dot lateral PNP BJT:

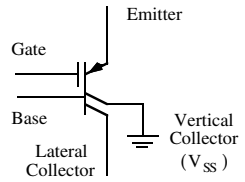


40 emitter dot LPNP transistor (total device area is $0.006mm^2$ in a 1.2µm CMOS process):

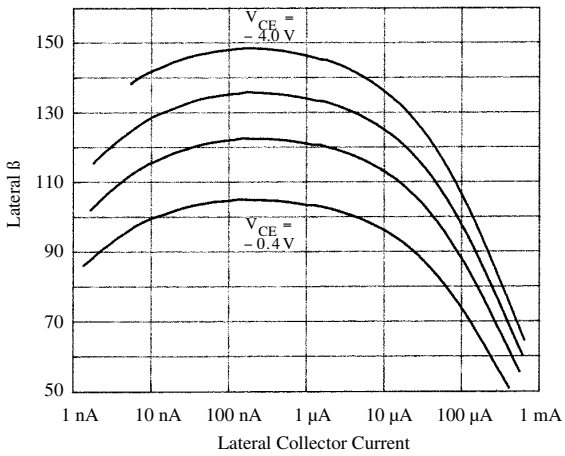


Performance of the Lateral PNP BJT

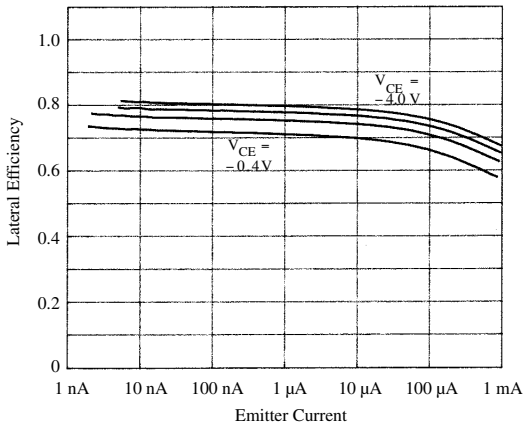
Schematic:



$ß_L$ vs I_{CL} for the 40 emitter dot LPNP BJT:



Lateral efficiency versus I_E for the 40 emitter dot LPNP BJT:



Performance of the Lateral PNP BJT - Continued

Typical Performance for the 40 emitter dot LPNP BJT:

Transistor area	0.006 mm^2
Lateral ß	90
Lateral efficiency	0.70
Base resistance	150 Ω
E_n @ 5 Hz	2.46 nV / $\sqrt{Hz}$
E_n (midband)	1.92 nV / $\sqrt{Hz}$
f_c (E_n)	3.2 Hz
I_n @ 5 Hz	3.53 pA / $\sqrt{Hz}$
I_n (midband)	0.61 pA / $\sqrt{Hz}$
f_c (In)	162 Hz
f_T	85 MHz
Early voltage	16 V

High Voltage MOS Transistor

The well can be substituted for the drain giving a lower conductivity drain and therefore higher breakdown voltage.

NMOS in n-well example:

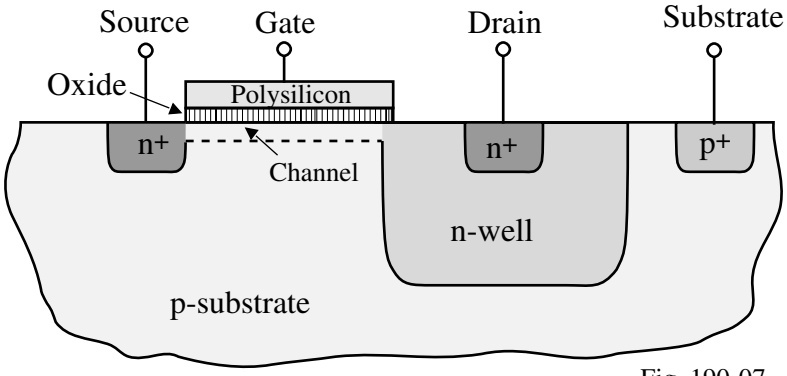


Fig. 190-07

Drain-substrate/channel can be as large as 20V or more.

Need to make the channel longer to avoid breakdowns via the channel.

Latch-up in CMOS Technology

Latch-up Mechanisms

1. SCR regenerative switching action.
2. Secondary breakdown.
3. Sustaining voltage breakdown.

Parasitic lateral PNP and vertical NPN BJTs in a p-well CMOS technology:

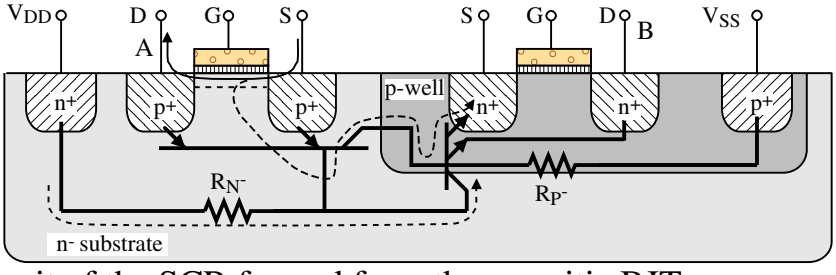


Fig. 190-08

Equivalent circuit of the SCR formed from the parasitic BJTs:

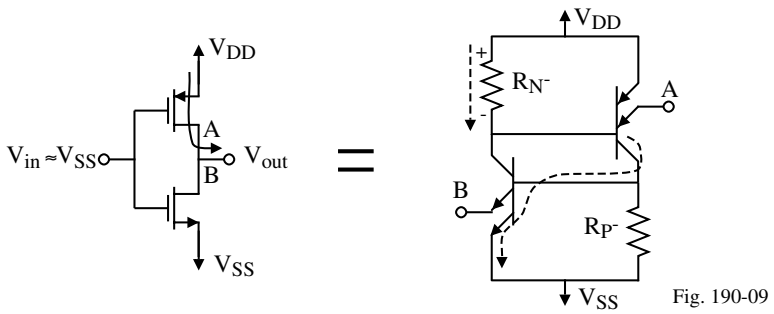


Fig. 190-09

Preventing Latch-Up in a P-Well Technology

1.) Keep the source/drain of the MOS device not in the well as far away from the well as possible. This will lower the value of the BJT betas.

2.) Reduce the values of R_{N^-} and R_{P^-}. This requires more current before latch-up can occur.

3.) Make a p^- diffusion around the p-well. This shorts the collector of Q1 to ground.

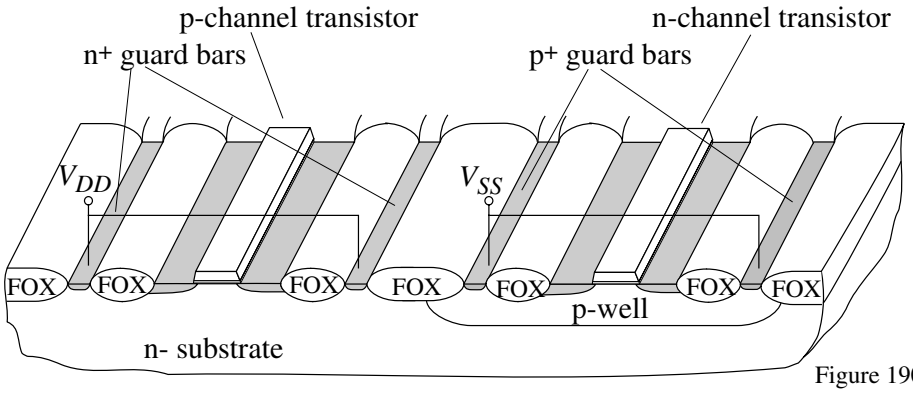


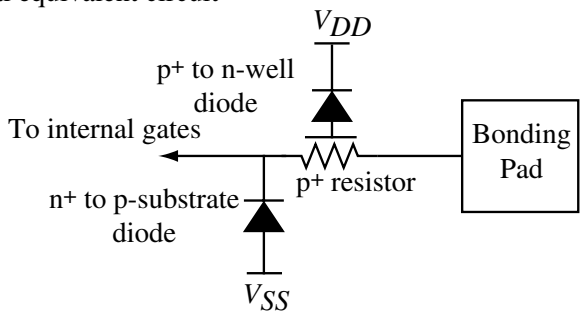
Figure 190-10

For more information see R. Troutman, "CMOS Latchup", Kluwer Academic Publishers.

Electrostatic Discharge Protection (ESD)

Objective: To prevent large external voltages from destroying the gate oxide.

Electrical equivalent circuit



Implementation in CMOS technology

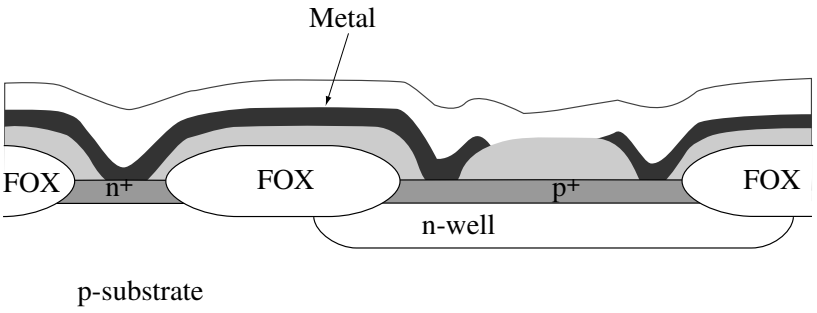


Fig. 190-11

Temperature Characteristics of Transistors

Fractional Temperature Coefficient

$$TCF = \frac{1}{x}\cdot\frac{\partial x}{\partial T}$$ Typically in ppm/°C

MOS Transistor

$V_T = V(T_0) + \alpha(T-T_0) + \cdots$, where $\alpha \approx -2.3$mV/°C (200°K to 400°K)

$\mu = K_\mu T^{-1.5}$

BJT Transistor

Reverse Current, I_S:

$$\frac{1}{I_S}\cdot\frac{\partial I_S}{\partial T} = \frac{3}{T} + \frac{1}{T}\frac{V_{G0}}{kT/q}$$

Empirically, I_S doubles approximately every 5°C increase

Forward Voltage, v_D:

$$\frac{\partial v_D}{\partial T} = -\frac{V_{G0} - v_D}{T} - \frac{3kT/q}{T} \approx -2\text{mV/°C at } v_D = 0.6\text{V}$$

Noise in Transistors

Shot Noise

$$\overline{i^2} = 2qI_D\Delta f \text{ (amperes}^2\text{)}$$

where

q = charge of an electron
I_D = dc value of i_D
Δf = bandwidth in Hz

Noise current spectral density = $\frac{\overline{i^2}}{\Delta f}$ (amperes^2/Hz)

Thermal Noise

Resistor:

$$\overline{v^2} = 4kTR\Delta f \text{ (volts}^2\text{)}$$

MOSFET:

$$\overline{i_D^2} = \frac{8kTg_m\Delta f}{3}$$ (ignoring bottom gate)

where

k = Boltzmann's constant
R = resistor or equivalent resistor in which the thermal noise is occurring.
g_m = transconductance of the MOSFET

Noise in Transistors - Continued

Flicker (1/f) Noise

$$\overline{i_D^2} = K_f\left(\frac{I^a}{f^b}\right)\Delta f$$

where

K_f = constant (10^{-28} Farad·amperes)

a = constant (0.5 to 2)

b = constant (≈1)

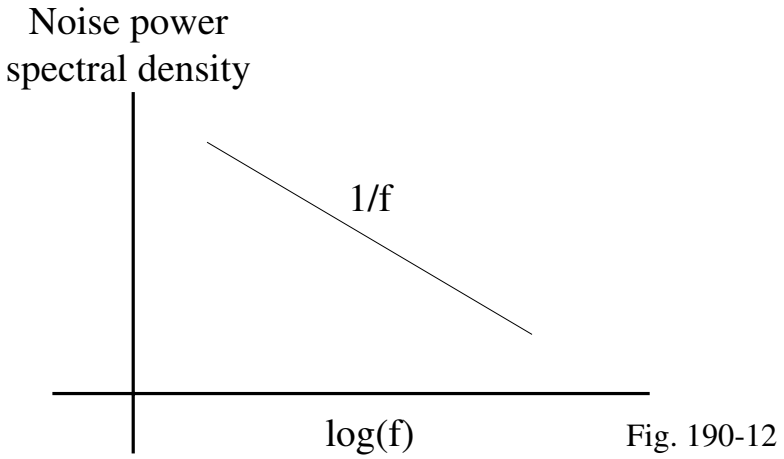


Fig. 190-12

SUMMARY

- Active devices compatible with standard CMOS technology are:
  - Lateral BJTs
  - Vertical BJTs (not shown)
- Other considerations
  - Latchup
  - Electrostatic Breakdown
  - Temperature and noise characteristics of transistors

