LECTURE 190 – CMOS TECHNOLOGY-COMPATIBLE DEVICES

(READING: Text-Sec. 2.9)

INTRODUCTION

Objective
The objective of this presentation is examine devices that are compatible with CMOS technology

Outline
• Compatible active devices – the BJT lateral transistor
• Latchup and ESD
• Temperature and noise characteristics
• Summary

COMPATIBLE ACTIVE DEVICES

Lateral Bipolar Junction Transistor
P-Well Process
NPN Lateral-
Lateral Bipolar Junction Transistor - Continued

Field-aided Lateral-

$\beta_F \approx 50$ to 100 depending on the process

- Good geometry matching
- Low $1/f$ noise (if channel doesn’t form)
- Acts like a photodetector with good efficiency

Geometry of the Lateral PNP BJT

Minimum Size layout of a single emitter dot lateral PNP BJT:

40 emitter dot LPNP transistor (total device area is $0.006 \text{mm}^2$ in a 1.2$\mu$m CMOS process):
Performance of the Lateral PNP BJT

Schematic:

\[
\begin{array}{c}
\text{Emitter} \\
\text{Gate} \\
\text{Base} \\
\text{Lateral Collector} \\
\text{Vertical Collector (Vss)}
\end{array}
\]

\[\beta_L \text{ vs } I_{CL} \text{ for the 40 emitter dot LPNP BJT:}\]

\[\text{Lateral efficiency versus } I_E \text{ for the 40 emitter dot LPNP BJT:}\]

\[
\begin{array}{c}
\text{Lateral Collector Current} \\
1 \text{nA} \quad 10 \text{nA} \quad 100 \text{nA} \quad 1 \mu A \quad 10 \mu A \quad 100 \mu A \quad 1 \text{mA}
\end{array}
\]

\[
\begin{array}{c}
\text{Lateral } \beta \\
50 \quad 70 \quad 90 \quad 110 \quad 130 \quad 150
\end{array}
\]

\[
\begin{array}{c}
\text{Emitter Current} \\
1 \text{nA} \quad 1 \mu A \quad 10 \mu A \quad 100 \mu A \quad 1 \text{mA}
\end{array}
\]

Performance of the Lateral PNP BJT - Continued

Typical Performance for the 40 emitter dot LPNP BJT:

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Transistor area</td>
<td>0.006 mm²</td>
</tr>
<tr>
<td>Lateral ( \beta )</td>
<td>90</td>
</tr>
<tr>
<td>Lateral efficiency</td>
<td>0.70</td>
</tr>
<tr>
<td>Base resistance</td>
<td>150 Ω</td>
</tr>
<tr>
<td>( E_n ) at 5 Hz</td>
<td>2.46 nV / \sqrt{Hz}</td>
</tr>
<tr>
<td>( E_n ) (midband)</td>
<td>1.92 nV / \sqrt{Hz}</td>
</tr>
<tr>
<td>( f_c ) (( E_n ))</td>
<td>3.2 Hz</td>
</tr>
<tr>
<td>( I_n ) at 5 Hz</td>
<td>3.53 pA / \sqrt{Hz}</td>
</tr>
<tr>
<td>( I_n ) (midband)</td>
<td>0.61 pA / \sqrt{Hz}</td>
</tr>
<tr>
<td>( f_c ) (( I_n ))</td>
<td>162 Hz</td>
</tr>
<tr>
<td>( f_T )</td>
<td>85 MHz</td>
</tr>
<tr>
<td>Early voltage</td>
<td>16 V</td>
</tr>
</tbody>
</table>
**High Voltage MOS Transistor**
The well can be substituted for the drain giving a lower conductivity drain and therefore higher breakdown voltage.

NMOS in n-well example:

Drain-substrate/channel can be as large as 20V or more. Need to make the channel longer to avoid breakdowns via the channel.

**Latch-up in CMOS Technology**

**Latch-up Mechanisms**
1. SCR regenerative switching action.
2. Secondary breakdown.
3. Sustaining voltage breakdown.

Parasitic lateral PNP and vertical NPN BJTs in a p-well CMOS technology:

Equivalent circuit of the SCR formed from the parasitic BJTs:
Preventing Latch-Up in a P-Well Technology

1.) Keep the source/drain of the MOS device not in the well as far away from the well as possible. This will lower the value of the BJT betas.

2.) Reduce the values of $R_N$ and $R_P$. This requires more current before latch-up can occur.

3.) Make a $p^-$ diffusion around the p-well. This shorts the collector of Q1 to ground.


Electrostatic Discharge Protection (ESD)

Objective: To prevent large external voltages from destroying the gate oxide.

Electrical equivalent circuit

Implementation in CMOS technology
Temperature Characteristics of Transistors

Fractional Temperature Coefficient

$$TCF = \frac{1}{X} \cdot \frac{\partial x}{\partial T}$$ Typically in ppm/°C

MOS Transistor

$$V_T = V(T_0) + \alpha(T-T_0) + \cdots$$, where $$\alpha \approx -2.3\text{mV/°C} \ (200\text{°K to 400°K})$$

$$\mu = K\mu T^{-1.5}$$

BJT Transistor

Reverse Current, $$I_S$$:

$$\frac{1}{I_S} \cdot \frac{\partial I_S}{\partial T} = T + \frac{1}{T} \frac{V_{G0}}{kT/q}$$

Empirically, $$I_S$$ doubles approximately every 5°C increase

Forward Voltage, $$v_D$$:

$$\frac{\partial v_D}{\partial T} = -\frac{V_{G0} - v_D}{T} - \frac{3kT/q}{T} \approx -2\text{mV/°C} \text{ at } v_D = 0.6V$$

Noise in Transistors

Shot Noise

$$\bar{i^2} = 2qID\Delta f \text{ (amperes}^2\text{)}$$

where

$$q = \text{charge of an electron}$$

$$ID = \text{dc value of } i_D$$

$$\Delta f = \text{bandwidth in Hz}$$

Noise current spectral density = $$\frac{i^2}{\Delta f} \text{ (amperes}^2/\text{Hz)}$$

Thermal Noise

Resistor:

$$\bar{v^2} = 4kTR\Delta f \text{ (volts}^2\text{)}$$

MOSFET:

$$\bar{i_D^2} = \frac{8kTg_m\Delta f}{3} \text{ (ignoring bottom gate)}$$

where

$$k = \text{Boltzmann’s constant}$$

$$R = \text{resistor or equivalent resistor in which the thermal noise is occurring.}$$

$$g_m = \text{transconductance of the MOSFET}$$
Noise in Transistors - Continued

Flicker (1/f) Noise

\[ i_D^2 = K_f \left( \frac{I_a}{f^a} \right) \Delta f \]

where

\[ K_f = \text{constant (10}^{-28} \text{ Farad}\cdot\text{amperes)} \]

\[ a = \text{constant (0.5 to 2)} \]

\[ b = \text{constant } (\approx 1) \]

SUMMARY

- Active devices compatible with standard CMOS technology are:
  - Lateral BJTs
  - Vertical BJTs (not shown)
- Other considerations
  - Latchup
  - Electrostatic Breakdown
  - Temperature and noise characteristics of transistors