LECTURE 192 – CMOS PASSIVE COMPONENTS - I
(READING: Text-Sec. 2.10)

Objective

The objective of this presentation is:

1.) Examine the passive components that are compatible with CMOS technology

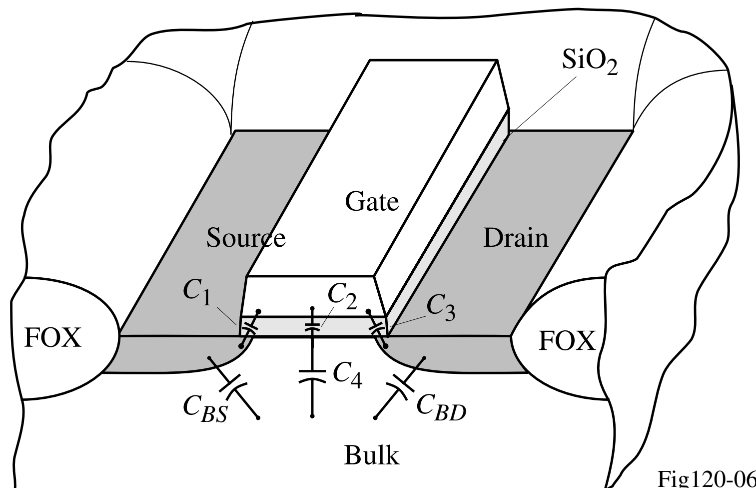
2.) Physical influence on passive components

Outline

- Capacitors
- Resistors
- Summary

Types of Capacitors in a MOSFET

Physical Picture:



MOSFET capacitors consist of:

- Depletion capacitances
- Charge storage or parallel plate capacitances

MOSFET Depletion Capacitors

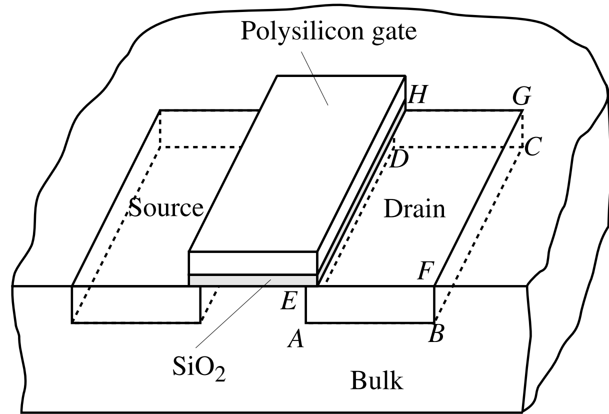


Fig. 120-07

Drain bottom = $ABCD$

Drain sidewall = $ABFE + BCGF + DCGH + ADHE$

Model:

1.) $v_{BS} \leq FC \cdot PB$

$$C_{BS} = \frac{CJ \cdot AS}{\left(1 - \frac{v_{BS}}{PB}\right)^{MJ}} + \frac{CJSW \cdot PS}{\left(1 - \frac{v_{BS}}{PB}\right)^{MJSW}},$$

and

2.) $v_{BS} > FC \cdot PB$

$$C_{BS} = \frac{CJ \cdot AS}{(1 - FC)^{1+MJ}}\left(1 - (1+MJ)FC + MJ\frac{V_{BS}}{PB}\right)$$

$$+ \frac{CJSW \cdot PS}{(1 - FC)^{1+MJSW}}\left(1 - (1+MJSW)FC + MJSW\frac{V_{BS}}{PB}\right)$$

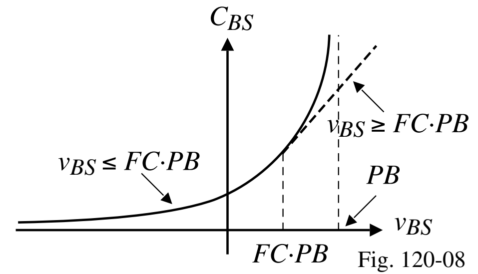


Fig. 120-08

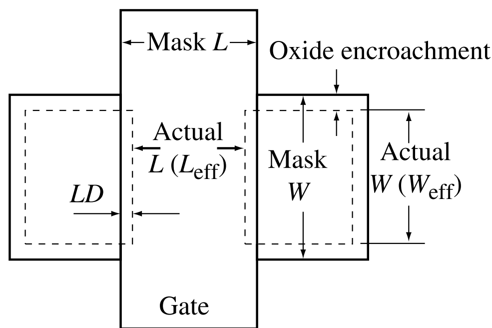
where

- AS = area of the source
- PS = perimeter of the source
- $CJSW$ = zero bias, bulk source sidewall capacitance
- $MJSW$ = bulk-source sidewall grading coefficient

For the bulk-drain depletion capacitance replace "S" by "D" in the above.

© P.E. Allen - 2002

Charge Storage (Parallel Plate) MOSFET Capacitances - C_1, C_2, C_3 and C_4



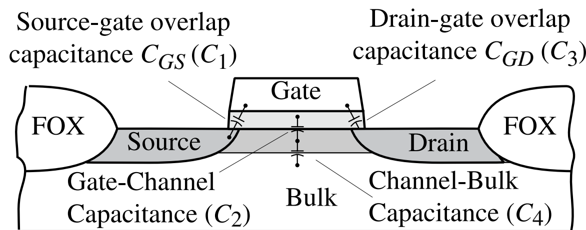


Fig. 120-09

Overlap capacitances:

$C_1 = C_3 = \text{LD} \cdot W_{eff} \cdot C_{ox}$ = CGSO or CGDO

(LD ≈ 0.015 μm for LDD structures)

Channel capacitances:

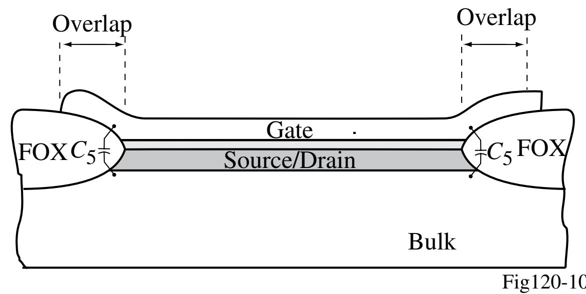
C_2 = gate-to-channel = $C_{ox}W_{eff} \cdot (L\text{-}2\text{LD}) = C_{ox}W_{eff} \cdot L_{eff}$

C_4 = voltage dependent channel-bulk/substrate capacitance

© P.E. Allen - 2002

Charge Storage (Parallel Plate) MOSFET Capacitances - C_5

View looking down the channel from source to drain



C_5 = CGBO

Capacitance values based on an oxide thickness of 140 Å or C_{ox}=24.7 × 10^{-4} F/m^2:

Type	P-Channel	N-Channel	Units
CGSO	220×10^{-12}	220×10^{-12}	F/m
CGDO	220×10^{-12}	220×10^{-12}	F/m
CGBO	700×10^{-12}	700×10^{-12}	F/m
CJ	560×10^{-6}	770×10^{-6}	F/m^2
CJSW	350×10^{-12}	380×10^{-12}	F/m
MJ	0.5	0.5	
MJSW	0.35	0.38	

© P.E. Allen - 2002

Expressions for C_{GD}, C_{GS} and C_{GB}

Cutoff Region:

$$C_{GB} = C_2 + 2C_5 = C_{ox}(W_{eff})(L_{eff}) + 2\text{CGBO}(L_{eff})$$

$$C_{GS} = C_1 \approx C_{ox}(\text{LD})W_{eff} = \text{CGSO}(W_{eff})$$

$$C_{GD} = C_3 \approx C_{ox}(\text{LD})W_{eff} = \text{CGDO}(W_{eff})$$

Saturation Region:

$$C_{GB} = 2C_5 = \text{CGBO}(L_{eff})$$

$$C_{GS} = C_1 + (2/3)C_2 = C_{ox}(\text{LD}+0.67L_{eff})(W_{eff}) = \text{CGSO}(W_{eff}) + 0.67C_{ox}(W_{eff})(L_{eff})$$

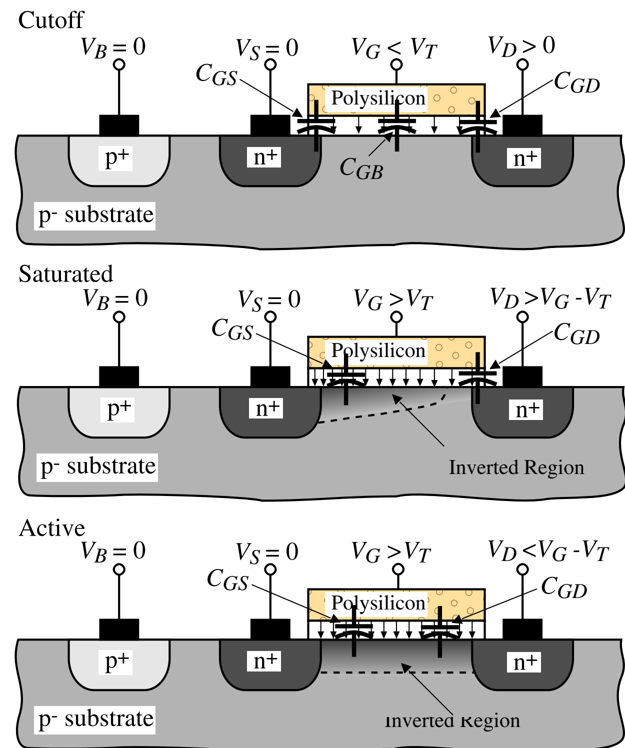
$$C_{GD} = C_3 \approx C_{ox}(\text{LD})W_{eff}) = \text{CGDO}(W_{eff})$$

Nonsaturated Region:

$$C_{GB} = 2\ C_5 = 2\text{CGBO}(L_{eff})$$

$$C_{GS} = C_1 + 0.5C_2 = C_{ox}(\text{LD}+0.5L_{eff})(W_{eff}) = (\text{CGSO} + 0.5C_{ox}L_{eff})W_{eff}$$

$$C_{GD} = C_3 + 0.5C_2 = C_{ox}(\text{LD}+0.5L_{eff})(W_{eff}) = (\text{CGDO} + 0.5C_{ox}L_{eff})W_{eff}$$



© P.E. Allen - 2002

Illustration of C_{GD}, C_{GS} and C_{GB}

Comments on the variation of C_{BG} in the cutoff region:

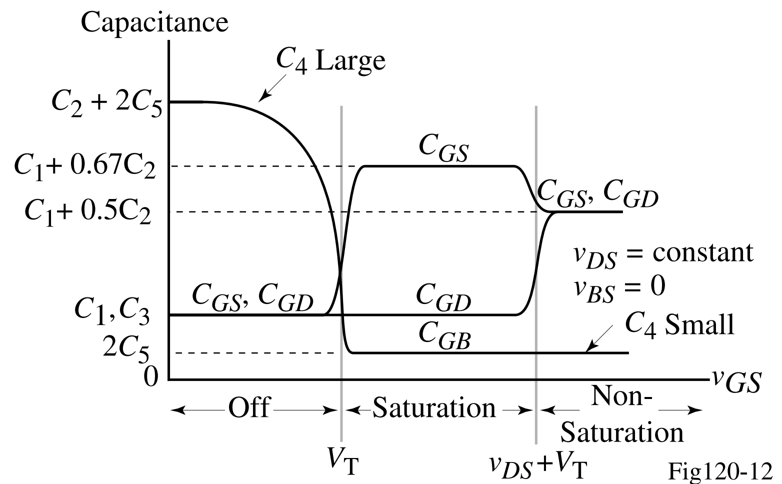
$$C_{BG} = \frac{1}{\frac{1}{C_2} + \frac{1}{C_4}} + 2C_5$$

1.) For $v_{GS} \approx 0$, $C_{GB} \approx C_2 + 2C_5$

(C_4 is large because of the thin inversion layer in weak inversion where V_{GS} is slightly less than V_T))

2.) For $0 < v_{GS} \leq V_T$, $C_{GB} \approx 2C_5$

(C_4 is small because of the thicker inversion layer in strong inversion)



 © P.E. Allen - 2002

Characterization of Capacitors

- C is the desired capacitance
- Dissipation of a capacitor

  $Q = \omega C R_p$

  where R_p is the equivalent parallel resistance associated with the capacitor, C
- A varactor is a variable capacitor
- C_{max}/C_{min} ratio is the ratio of the largest value of capacitance to the smallest when the capacitor is used as a varactor.
- Parasitic capacitors are the capacitors to ac ground from both terminals of the desired capacitance.

 © P.E. Allen - 2002

Standard MOS Capacitors

Polysilicon-Oxide-Channel for Enhancement MOSFETs

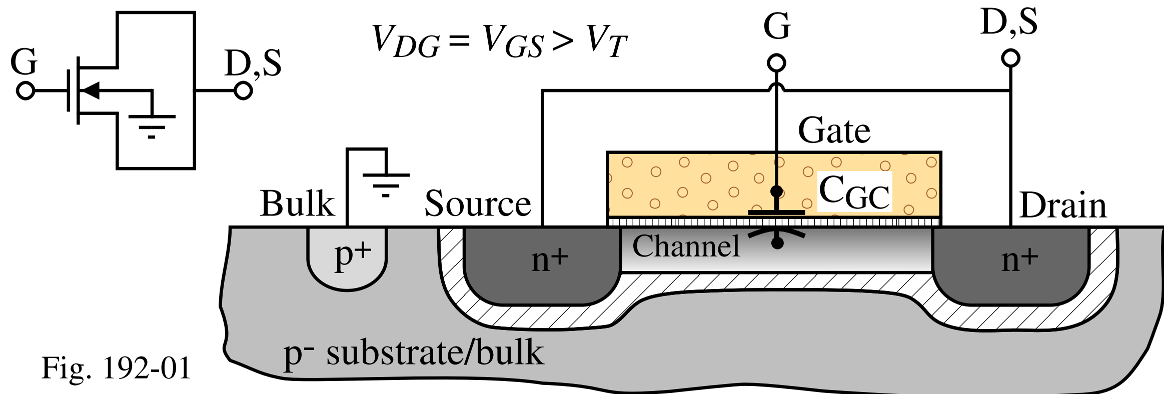


Fig. 192-01

Comments:

- The capacitance variation is achieved by changing the mode of operation from depletion (minimum capacitance) to inversion (maximum capacitance).
- Capacitance = $C_{GS} \approx C_{ox}W \cdot L$
- Channel must be formed, therefore $V_{GS} > V_T$
- With $V_{GS} > V_T$ and $V_{DS} = 0$, the transistor is in the active region.
- LDD transistors will give lower Q because of the increase of series resistance.

 © P.E. Allen - 2002

Standard MOS Capacitors - Continued

Bulk tuning of the polysilicon-oxide-channel capacitor (0.35µm CMOS)

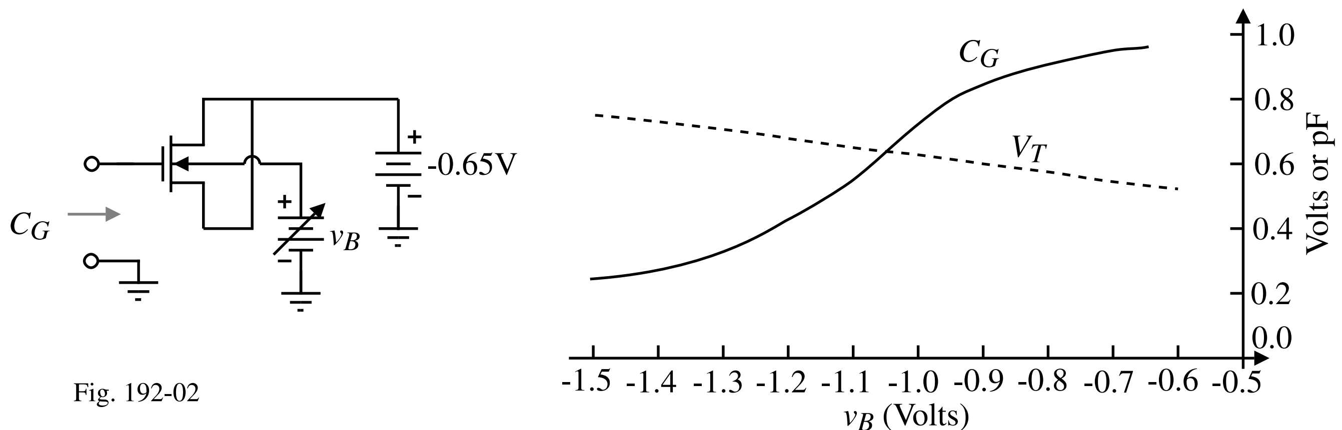


Fig. 192-02

$C_{max}/C_{min} \approx 4$

 © P.E. Allen - 2002

Standard MOS Capacitors - Continued

Bulk connected to Source-Drain

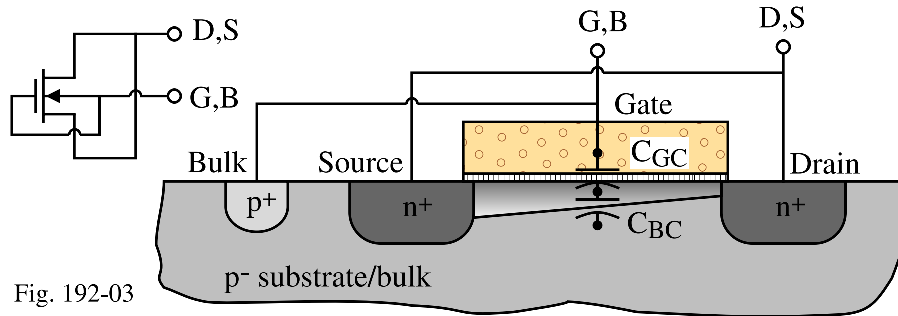


Fig. 192-03

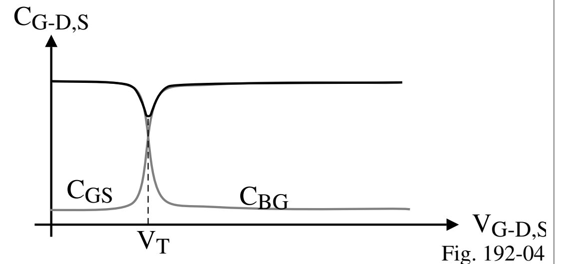


Fig. 192-04

$C_{G\text{-}D,S} = C_{GS} + C_{GB}$

Comments:

- Capacitance is more constant as a function of $V_{G\text{-}D,S}$
- Still not a good capacitor for large voltage swings
- Increased parasitics from the gate/bulk terminal

Standard Mode NMOS Varactor – Continued

More Detail - Includes the LDD transistor

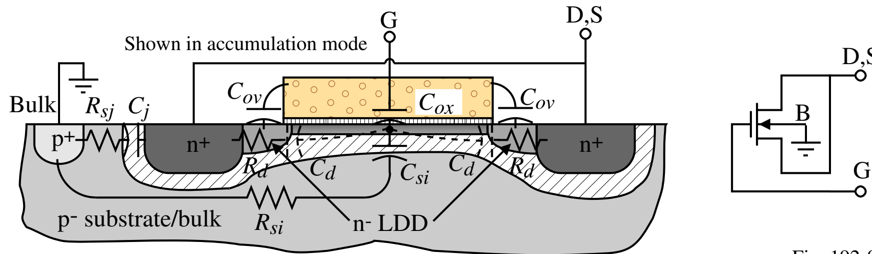


Fig. 192-05

Best results are obtained when the drain-source are on ac ground.

Experimental Results (Q at 2GHz, 0.5µm CMOS):

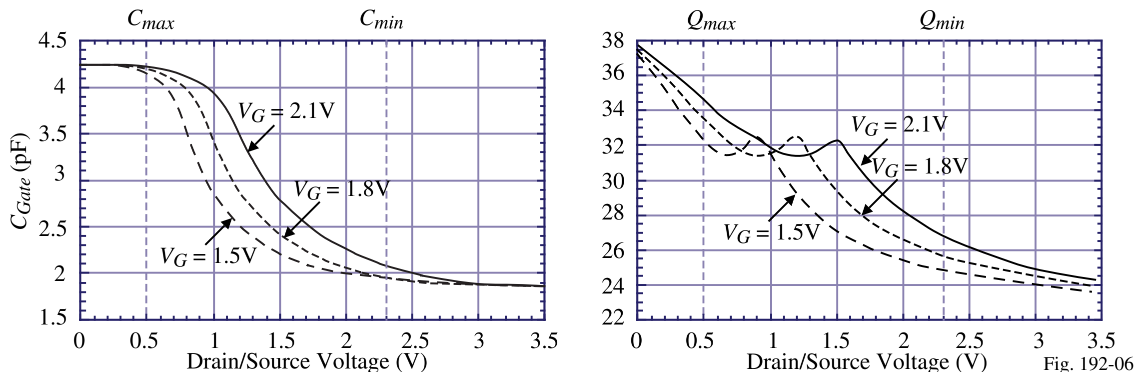


Fig. 192-06

V_G =1.8V: C_{max}/C_{min} ratio = 2.15 (1.91), Q_{max} = 34.3 (5.4), and Q_{min} = 25.8(4.9)

MOS Capacitors - Continued

Accumulation-Mode Capacitor[†],[††]

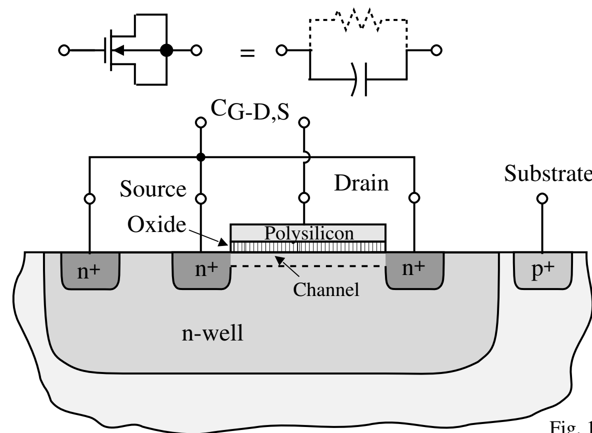


Fig. 192-07

Comments:

- Again, the capacitor variation is achieved by moving from the depletion (min. C) to accumulation (max. C)
- ±30% tuning range
- $Q \approx 25$ for 3.1pF at 1.8 GHz (optimization leads to Qs of 200 or greater)

---

† T. Soorapanth, et. al., "Analysis and Optimization of Accumulation-Mode Varactor for RF ICs," Proc. 1998 Sym. on VLSI Circuits, *Digest of Papers*, pp. 32-33, 1998.

†† R. Castello, et. al., "A ±30% Tuning Range Varactor Compatible with future Scaled Technologies," Proc. 1998 Sym. on VLSI Circuits, *Digest of Papers*, pp. 34-35, 1998.

 © P.E. Allen - 2002

Accumulation Capacitor – More Detail

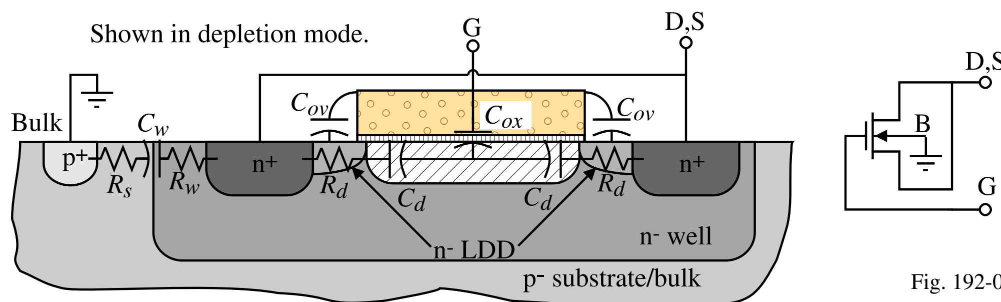


Fig. 192-08

Best results are obtained when the drain-source are on ac ground.

Experimental Results (Q at 2GHz, 0.5μm CMOS):

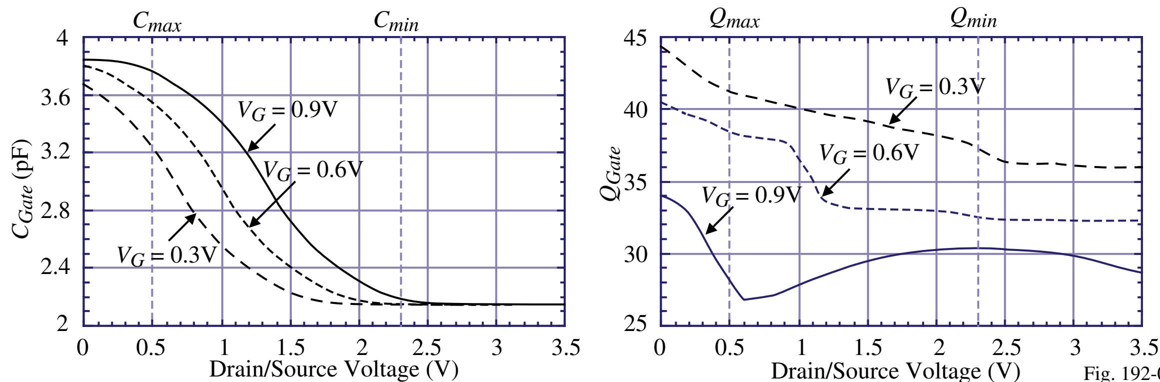


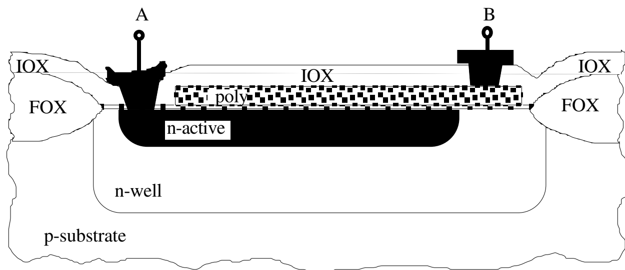
Fig. 192-09

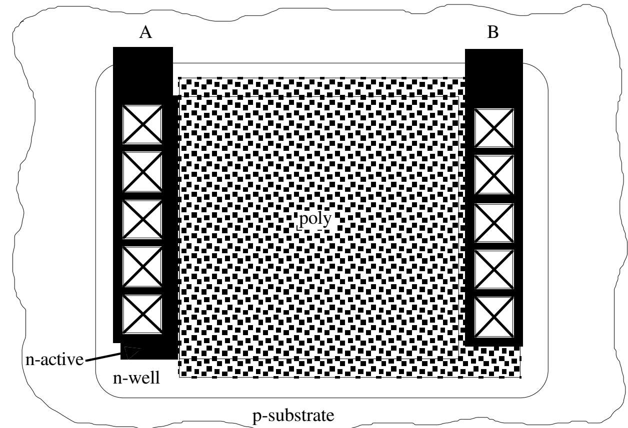
$V_G = 0.6$V: C_{max}/C_{min} ratio = 1.69 (1.61), Q_{max} = 38.3 (15.0), and Q_{min} = 33.2(13.6)

 © P.E. Allen - 2002

MOS Capacitors - Continued

Polysilicon-Oxide Diffusion/Active for Enhanced MOSFETs





Unit capacitance ≈ 1.2 fF/μm^2

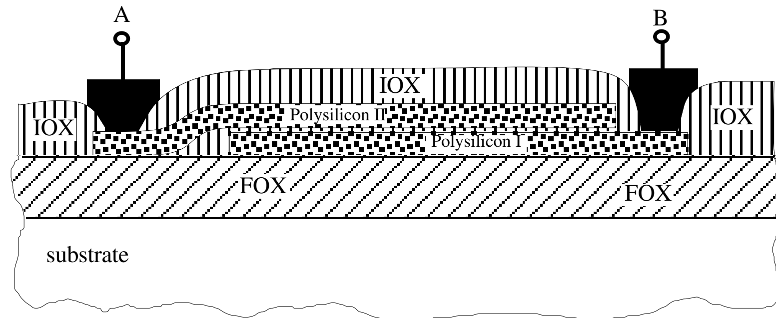
Voltage dependence:

$C(V) \approx C(0) + a_1 V + a_2 V^2$, where $a_1 \approx 0$ and $a_2 \approx 210$ ppm/V^2

(Not as good linearity as poly-poly capacitors)

MOS Capacitors - Continued

Polysilicon-Oxide-Polysilicon (Poly-Poly)



Best possible capacitor for analog circuits

Less parasitics

Voltage independent

Possible approach for increasing the voltage linearity:

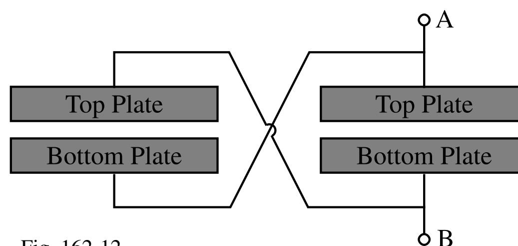


Fig. 162-12

Implementation of Capacitors using Available Interconnect Layers

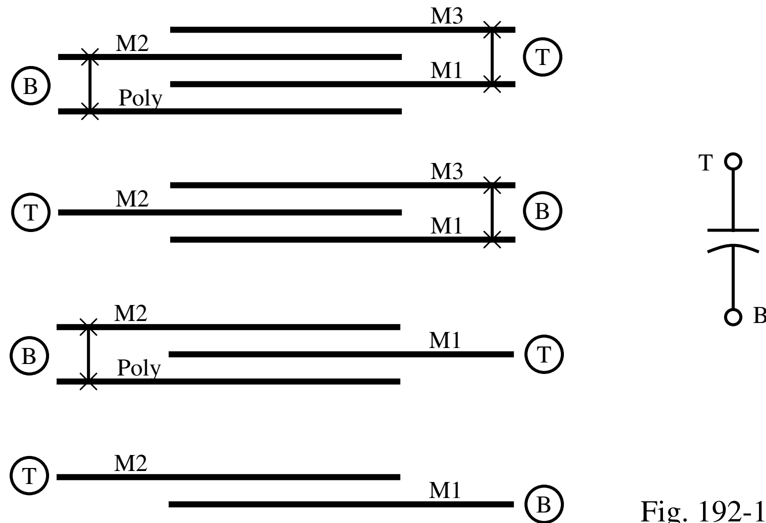
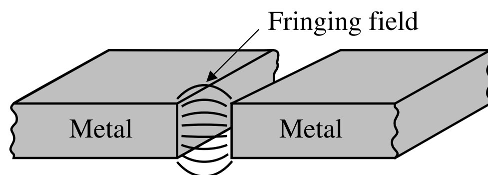


Fig. 192-13

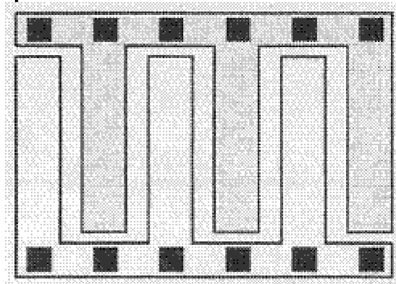
Horizontal Metal Capacitors

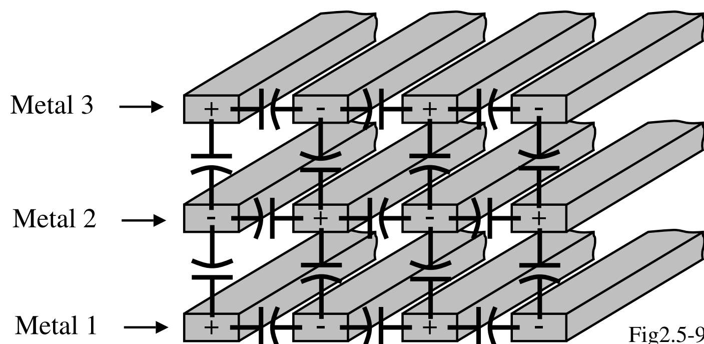
Capacitance between conductors on the same level and use lateral flux.

Fringing field

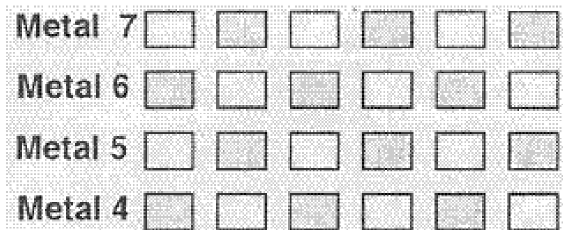


Top view:





Side view:



These capacitors are sometimes called fractal capacitors because the fractal patterns are structures that enclose a finite area with a near-infinite perimeter.

The capacitor/area can be increased by a factor of 10 over vertical flux capacitors (i.e., 1.5fF/μm^2).

To Be Continued

The next lecture will continue the examination of passive components compatible with CMOS technology.

© P.E. Allen - 2002