LECTURE 194 – CMOS PASSIVE COMPONENTS - II

(READING: Text-Sec. 2.10)

Objective

The objective of this presentation is:

1.) Examine the passive components that are compatible with CMOS technology

2.) Physical influence on passive components

Outline

- Capacitors
- Resistors
- Summary

Capacitor Errors

1.) Oxide gradients

2.) Edge effects

3.) Parasitics

4.) Voltage dependence

5.) Temperature dependence

Capacitor Errors - Oxide Gradients

Error due to a variation in oxide thickness across the wafer.

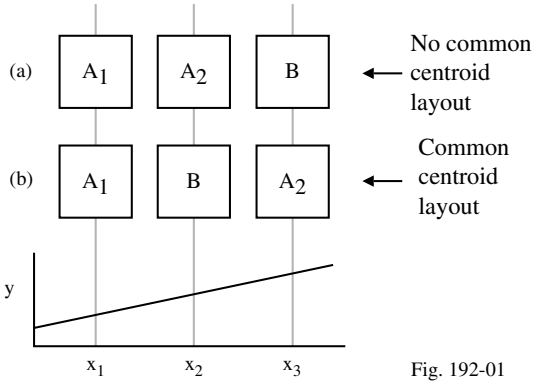


Fig. 192-01

Only good for one-dimensional errors.

An alternate approach is to layout numerous repetitions and connect them randomly to achieve a statistical error balanced over the entire area of interest.

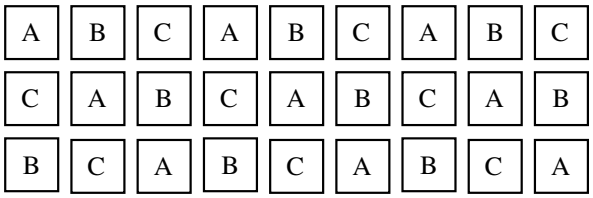


Fig. 194-02

0.2% matching of poly resistors was achieved using an array of 50 unit resistors.

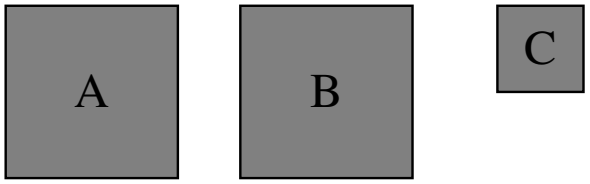
Capacitor Errors - Edge Effects

There will always be a randomness on the definition of the edge.

However, etching can be influenced by the presence of adjacent structures.

For example,

Matching of A and B are disturbed by the presence of C.



Improved matching achieved by balancing the adjacent material.

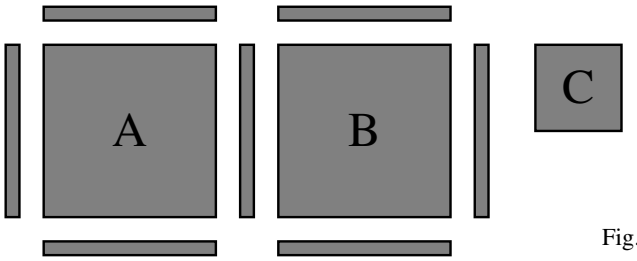


Fig. 194-03

Capacitor Errors - Area/Periphery Ratio

The best match between two structures occurs when their area-to-periphery ratios are identical.

Let $C'_1 = C_1 \pm \Delta C_1$ and $C'_2 = C_2 \pm \Delta C_2$

where

C' = the actual capacitance

C = the desired capacitance (which is proportional to *area*)

ΔC = edge uncertainty (which is proportional to the *periphery*)

Solve for the ratio of C'_2/C'_1,

$$\frac{C'_2}{C'_1} = \frac{C_2 \pm \Delta C_2}{C_1 \pm \Delta C_1} = \frac{C_2}{C_1}\left(\frac{1 \pm \frac{\Delta C_2}{C_2}}{1 \pm \frac{\Delta C_1}{C_1}}\right) \approx \frac{C_2}{C_1}\left(1 \pm \frac{\Delta C_2}{C_2}\right)\left(1 \mp \frac{\Delta C_1}{C_1}\right) \approx \frac{C_2}{C_1}\left(1 \pm \frac{\Delta C_2}{C_2} \mp \frac{\Delta C_1}{C_1}\right)$$

If $\frac{\Delta C_2}{C_2} = \frac{\Delta C_1}{C_1}$, then $\boxed{\frac{C'_2}{C'_1} = \frac{C_2}{C_1}}$

Therefore, the best matching results are obtained when the area/periphery ratio of C_2 is equal to the area/periphery ratio of C_1.

Capacitor Errors - Relative Accuracy

Capacitor relative accuracy is proportional to the area of the capacitors and inversely proportional to the difference in values between the two capacitors.

For example,

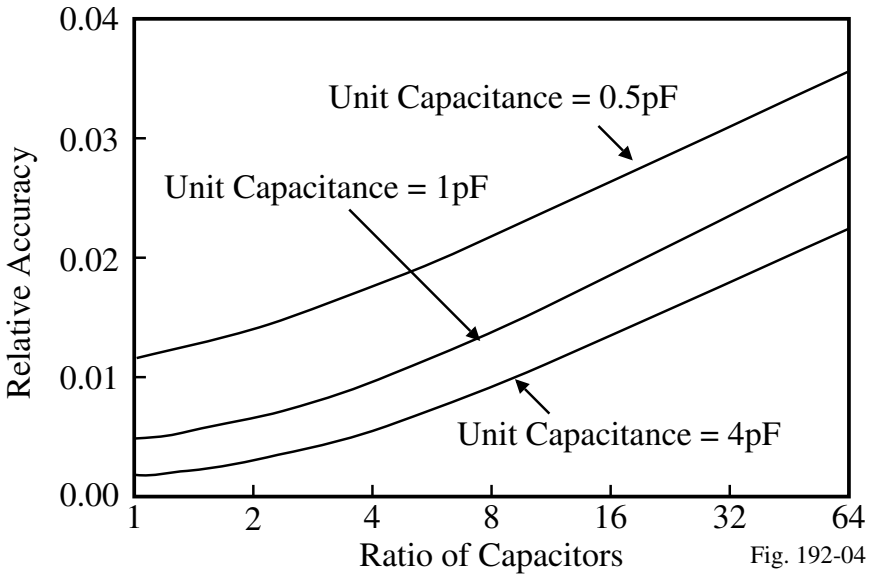


Fig. 192-04

This result will change if the unit capacitor consists of two or more unit capacitors.

Capacitor Errors - Parasitics

Parasitics are normally from the top and bottom plate to ac ground which is typically the substrate.

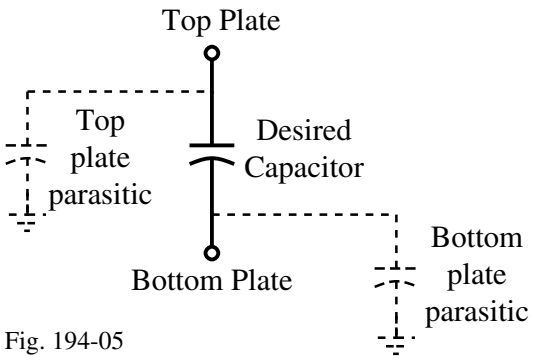


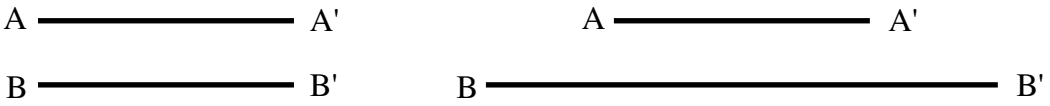
Fig. 194-05

Top plate parasitic is 0.01 to 0.001 of $C_{desired}$

Bottom plate parasitic is 0.05 to 0.2 $C_{desired}$

Other Considerations on Capacitor Accuracy

Decreasing Sensitivity to Edge Variation:



Sensitive to edge variation in both upper andlower plates

Sensitive to edge varation in upper plate only.

Fig. 194-06

A structure that minimizes the ratio of perimeter to area (circle is best).

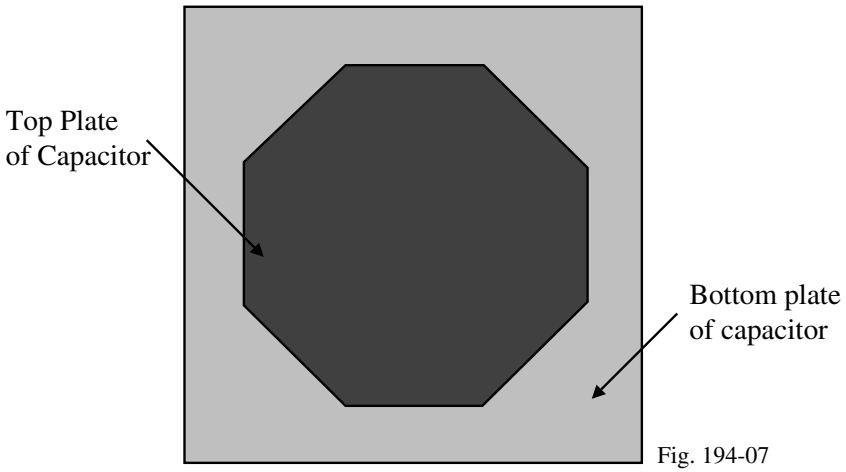


Fig. 194-07

Capacitor Errors - Temperature and Voltage Dependence

Polysilicon-Oxide-Semiconductor Capacitors

- Absolute accuracy ≈ ±10%
- Relative accuracy ≈ ±0.2%
- Temperature coefficient ≈ +25 ppm/C°
- Voltage coefficient ≈ -50ppm/V

Polysilicon-Oxide-Polysilicon Capacitors

- Absolute accuracy ≈ ±10%
- Relative accuracy ≈ ±0.2%
- Temperature coefficient ≈ +25 ppm/C°
- Voltage coefficient ≈ -20ppm/V

Accuracies depend upon the size of the capacitors.

- Accuracy $\propto 1/(\text{Area}^2)$

RESISTORS

MOS Resistors - Source/Drain Resistor

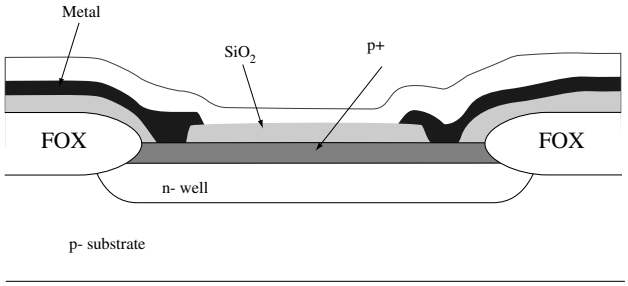


Fig. 194-08

Diffusion:

- 10-100 ohms/square
- Absolute accuracy = ±35%
- Relative accuracy = 2% (5μm), 0.2% (50 μm)
- Temperature coefficient = +1500 ppm/°C
- Voltage coefficient ≈ 200 ppm/V

Ion Implanted:

- 500-2000 ohms/square
- Absolute accuracy = ±15%
- Relative accuracy = 2% (5μm), 0.15% (50 μm)
- Temperature coefficient = +400 ppm/°C
- Voltage coefficient ≈ 800 ppm/V

Comments:

- Parasitic capacitance to substrate is voltage dependent.
- Piezoresistance effects occur due to chip strain from mounting.

Polysilicon Resistor

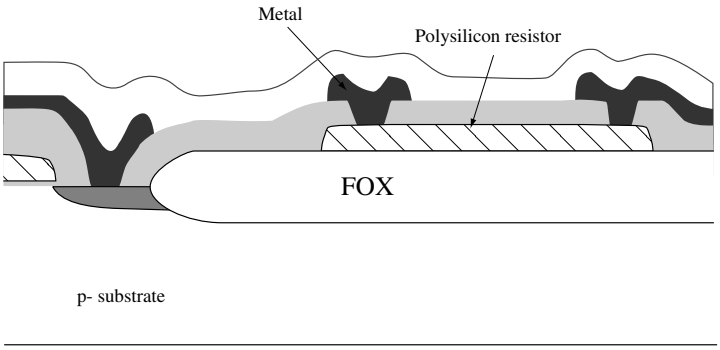


Fig. 194-09

30-100 ohms/square (unshielded)
100-500 ohms/square (shielded)
Absolute accuracy = ±30%
Relative accuracy = 2% (5 μm)
Temperature coefficient = 500-1000 ppm/°C
Voltage coefficient ≈ 100 ppm/V
Comments:

- Used for fuzes and laser trimming
- Good general resistor with low parasitics

N-well Resistor

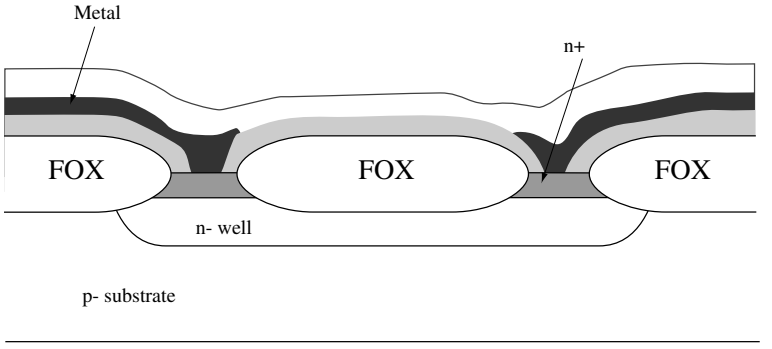


Fig. 194-10

1000-5000 ohms/square
Absolute accuracy = ±40%
Relative accuracy ≈ 5%
Temperature coefficient = 4000 ppm/°C
Voltage coefficient is large ≈ 8000 ppm/V
Comments:

- Good when large values of resistance are needed.
- Parasitics are large and resistance is voltage dependent

MOS Passive Component Performance Summary

Component Type	Range of Values	Absolute Accuracy	Relative Accuracy	Temperature Coefficient	Voltage Coefficient
Poly-oxide-semiconductor Capacitor	0.35-0.5 fF/μm²	10%	0.1%	20ppm/°C	±20ppm/V
Poly-Poly Capacitor	0.3-0.4 fF/μm²	20%	0.1%	25ppm/°C	±50ppm/V
Diffused Resistor	10-100 Ω/sq.	35%	2%	1500ppm/°C	200ppm/V
Ion Implanted Resistor	0.5-2 kΩ/sq.	15%	2%	400ppm/°C	800ppm/V
Poly Resistor	30-200 Ω/sq.	30%	2%	1500ppm/°C	100ppm/V
n-well Resistor	1-10 kΩ/sq.	40%	5%	8000ppm/°C	10kppm/V

The electrical performance of all passive components greatly depends on the geometry and physical aspects of the layout.

INDUCTORS

Inductors

What is the range of values for on-chip inductors?

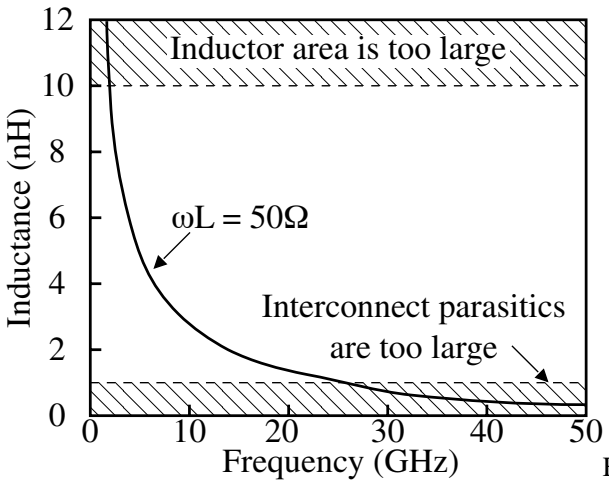


Fig. 6-5

Consider an inductor used to resonate with 5pF at 1000MHz.

$$L = \frac{1}{4\pi^2 f_o^2 C} = \frac{1}{(2\pi \cdot 10^9)^2 \cdot 5\text{x}10^{-12}} = 5\text{nH}$$

Note: Off-chip connections will result in inductance as well.

Candidates for inductors in CMOS technology are:

1.) Bond wires
2.) Spiral inductors
3.) Multi-level spiral
4.) Solenoid

Bond wire Inductors:

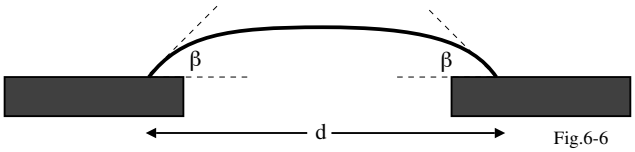


Fig.6-6

- Function of the pad distance d and the bond angle β
- Typical value is 1nH/mm which gives 2nH to 5nH in typical packages
- Series loss is 0.2 Ω/mm for 1 mil diameter aluminum wire
- $Q \approx 60$ at 2 GHz

Planar Spiral Inductors

Spiral Inductors on a Lossy Substrate:

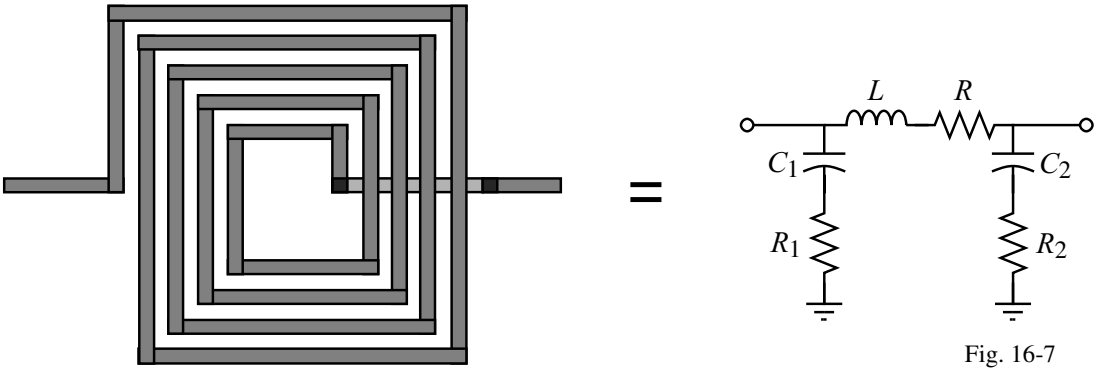


Fig. 16-7

- Design Parameters:

  Inductance, $L = \Sigma(L_{self} + L_{mutual})$

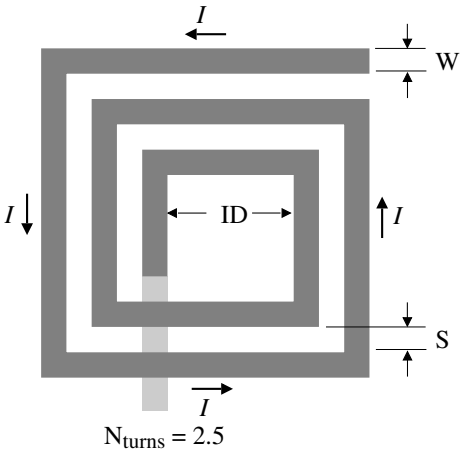
  Quality factor, $Q = \dfrac{\omega L}{R}$

  Self-resonant frequency: $f_{self} = \dfrac{1}{\sqrt{LC}}$

- Trade-off exists between the Q and self-resonant frequency
- Typical values are L = 1-8nH and Q = 3-6 at 2GHz

Planar Spiral Inductors - Continued

Inductor Design



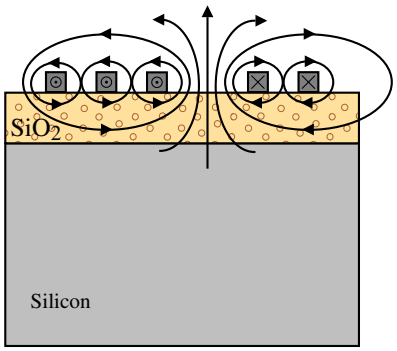


Fig. 6-9

Typically: $3 < N_{turns} < 5$ and $S = S_{min}$ for the given current

Select the OD, N_{turns}, and W so that ID allows sufficient magnetic flux to flow through the center.

Loss Mechanisms:

- Skin effect
- Capacitive substrate losses
- Eddy currents in the silicon

Planar Spiral Inductors - Continued

Influence of a Lossy Substrate

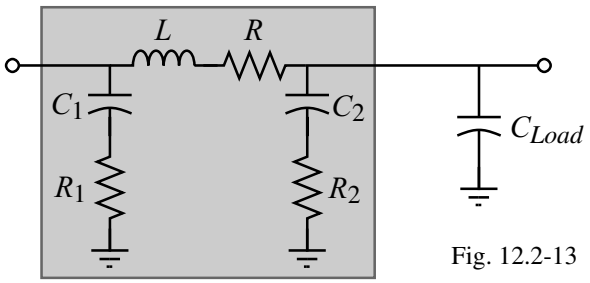


Fig. 12.2-13

where:

L is the desired inductance

R is the series resistance

C_1 and C_2 are the capacitance from the inductor to the ground plane

R_1 and R_2 are the eddy current losses in the silicon

Guidelines for using spiral inductors on chip:

- Lossy substrate degrades Q at frequencies close to f_{self}
- To achieve an inductor, one must select frequencies less than f_{self}
- The Q of the capacitors associated with the inductor should be very high

Planar Spiral Inductors - Continued

Comments concerning implementation:

1.) Put a metal ground shield between the inductor and the silicon to reduce the capacitance.

- Should be patterned so flux goes through but electric field is grounded
- Metal strips should be orthogonal to the spiral to avoid induced loop current
- The resistance of the shield should be low to terminate the electric field

2.) Avoid contact resistance wherever possible to keep the series resistance low.

3.) Use the metal with the lowest resistance and furtherest away from the substrate.

4.) Parallel metal strips if other metal levels are available to reduce the resistance.

Example:

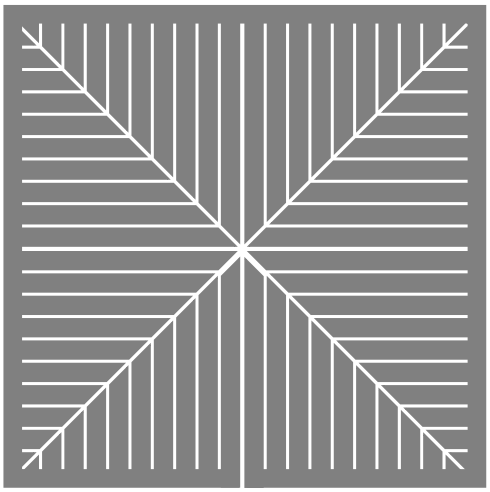
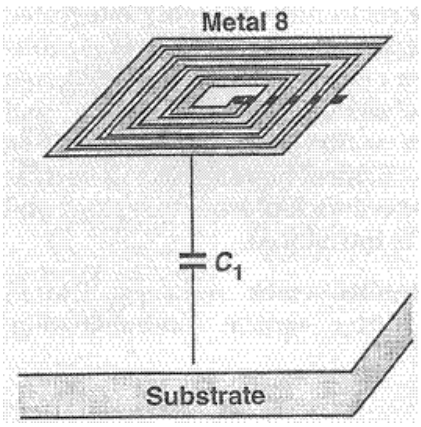


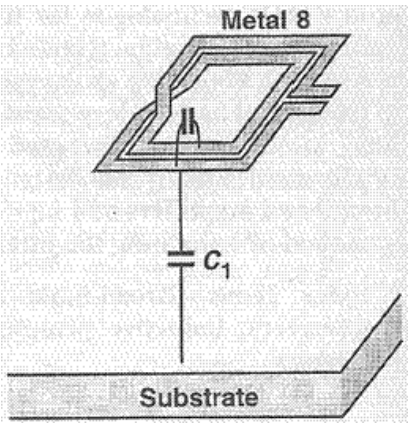
Fig. 2.5-12

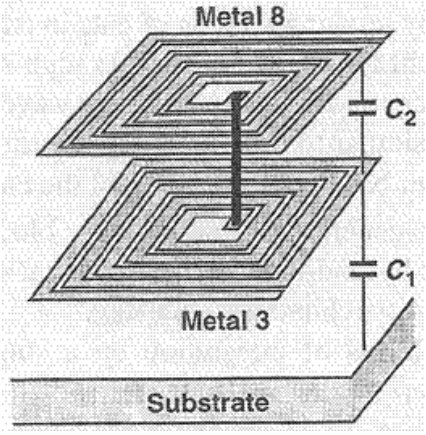
Multi-Level Spiral Inductors

Use of more than one level of metal to make the inductor.

- Can get more inductance per area
- Can increase the interwire capacitance so the different levels are often offset to get minimum overlap.
- Multi-level spiral inductors suffer from contact resistance (must have many parallel contacts to reduce the contact resistance).
- Metal especially designed for inductors is top level approximately 4μm thick.





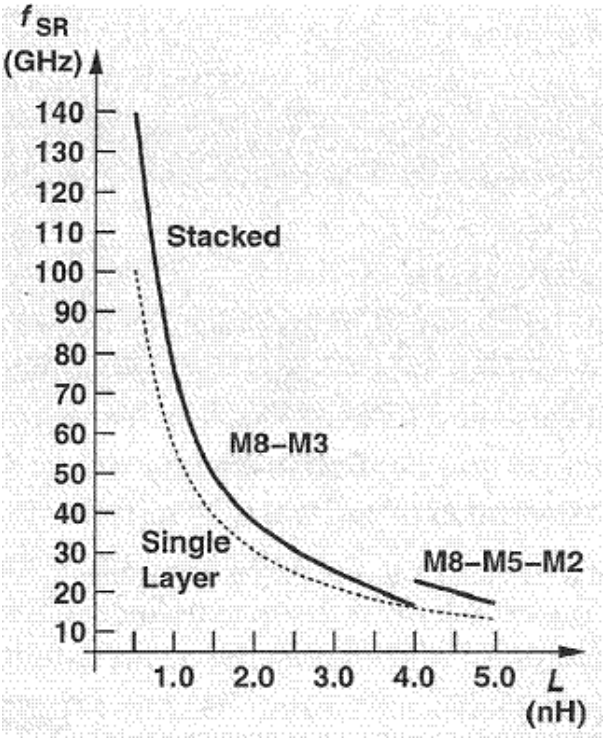


Q = 5-6, f_{SR} = 30-40GHz. Q = 10-11, f_{SR} = 15-30GHz[1]. Good for high L in small area.

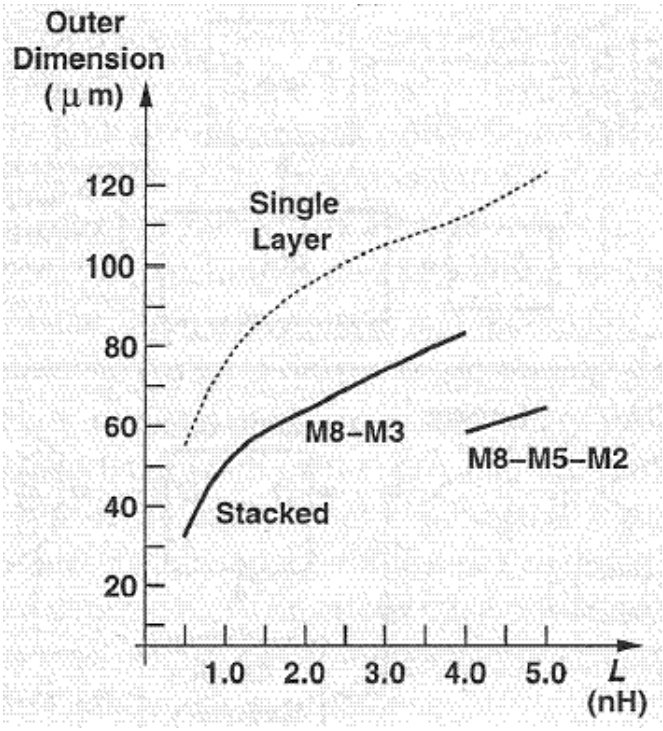
[1] The skin effect and substrate loss appear to be the limiting factor at higher frequencies of self-resonance.

Inductors - Continued

Self-resonance as a function of inductance.

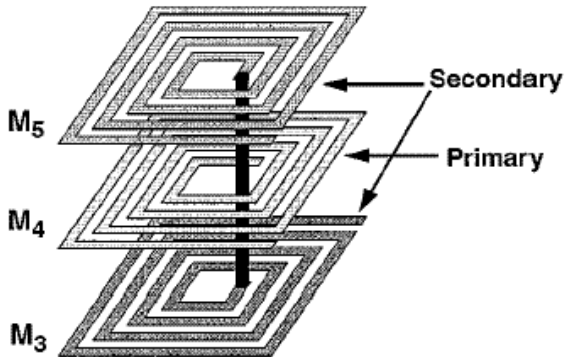


Outer dimension of inductors.

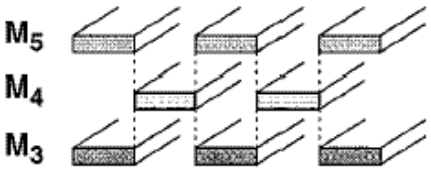


Transformers

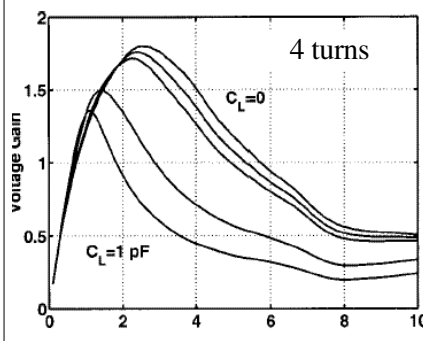
Transformer structures are easily obtained using stacked inductors as shown below for a 1:2 transformer.

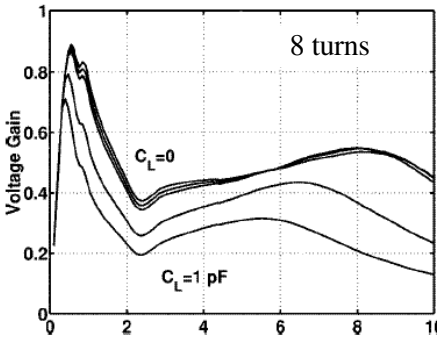


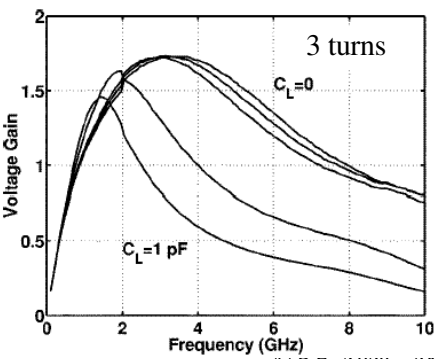
Method of reducing the inter-winding capacitances.



Measured 1:2 transformer voltage gains:



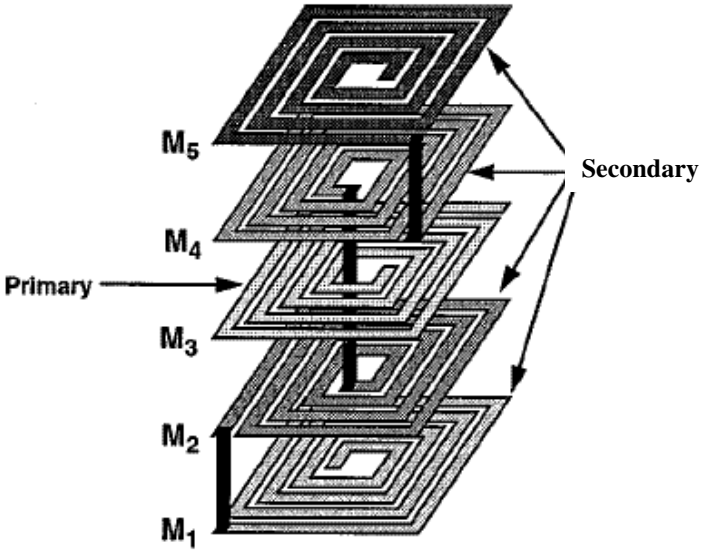




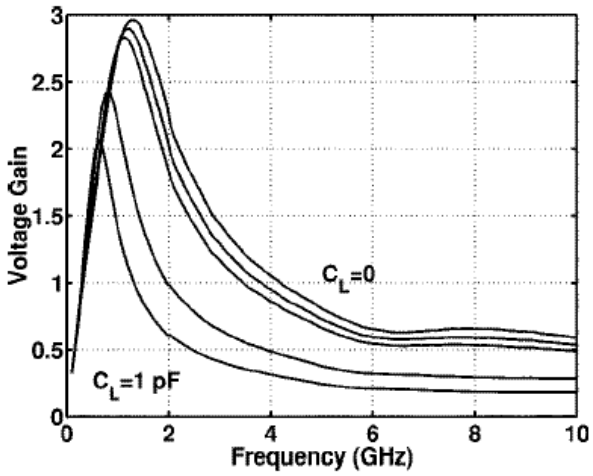
Transformers – Continued

A 1:4 transformer:

Structure-



Measured voltage gain-



SUMMARY

- IC passive components consist of:
  - Capacitors – depletion and parallel-plate
  - Resistors – diffusion/implantation, polysilicon, well/epitaxial and diodes
  - Inductors – metal spiral good at only high frequencies
  - Transformers – coupling coefficients of about 0.5-0.7
- For analog IC design, good quality passive components are extremely important
- Passive components determine gains, time constants, current-to-voltage conversion, etc.
- Most technologies are driven by digital demands and passive components are highly variable and have poor accuracies
- Accuracy generally increases with area
- Because IC technology has good relative accuracies for passive components, the designer should always try to express the desired performance as ratios of similar passive components.