LECTURE 210 – PHYSICAL ASPECTS OF ICs

(READING: Text-Sec. 2.5, 2.6, 2.8)

INTRODUCTION

Objective

- Illustrate the physical aspects of integrated circuits

Outline

- Examples
  - Identifying circuits from layouts
  - Identifying cross-sections corresponding to a layout
  - Extracting parasitics from layouts
- Summary

Example 1

Draw the schematic of the circuit corresponding to the CMOS layout.

Solution

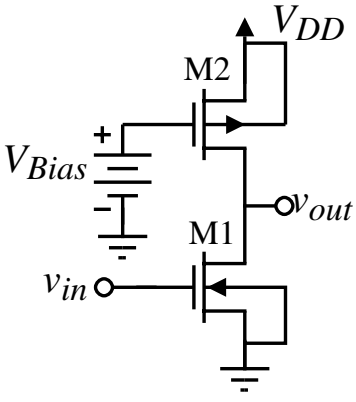


Fig. 210-02

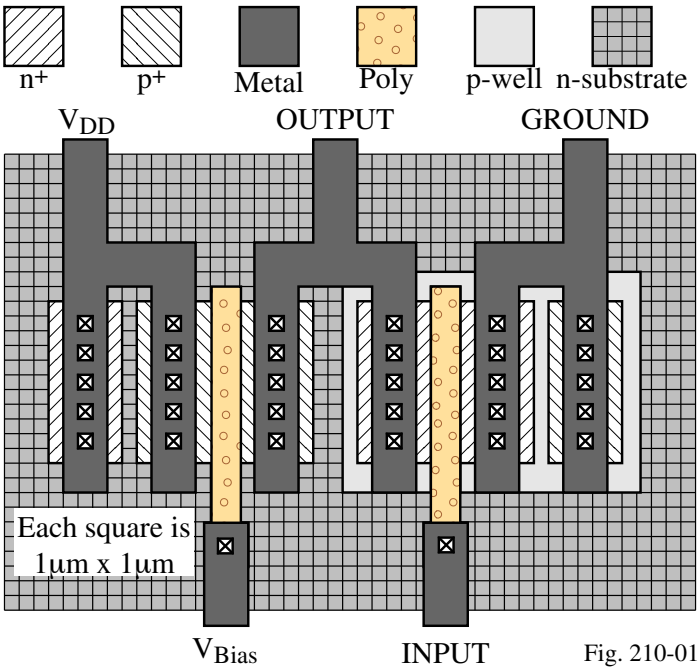


Fig. 210-01

Example 2

Draw the A-A' cross-section to scale of the integrated layout shown. The approximate physical thicknesses are:

- n^+ diffusion = 0.5μm
- p^+ diffusion = 0.6μm
- p-well depth = 3μm
- Field oxide (FOX) = 4μm
- Polysilicon = 1μm
- Metal = 1μm
- Thin oxide = 0.05μm
- Intermediate oxide (IOX) = 1μm

(You may use square corners in the oxides and diffusions for purposes of simplicity.)

Solution

See drawing. The scale for this drawing vertically is 0.25μm per square.

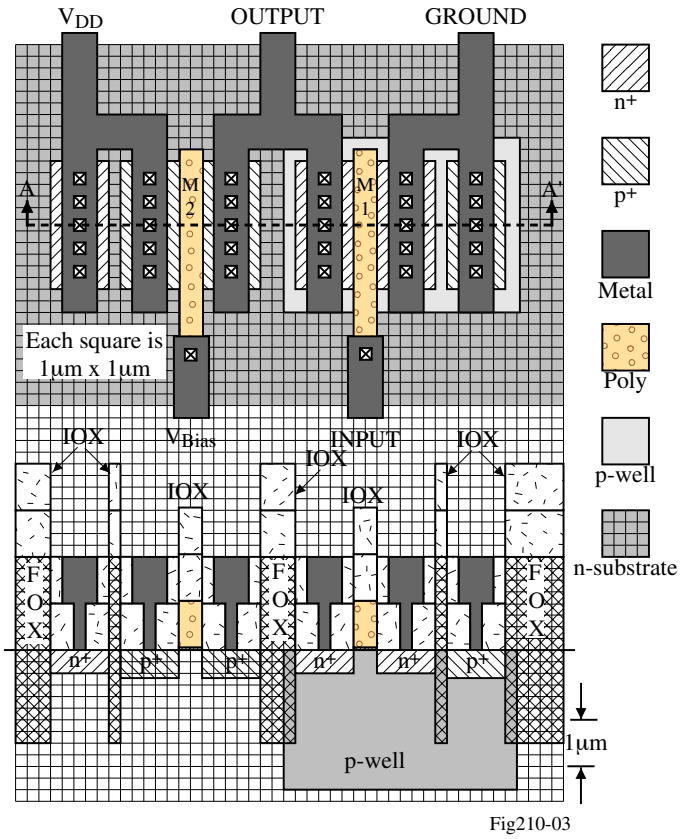


Fig210-03

Example 3

For the MOS transistors of Example 1, find the bulk resistances between the source and drain of each transistor to the metal. Assume that the sheet resistance of the n^+ is 35 Ω/sq. and of the p^+ is 80 Ω/sq. Number each MOSFET and use this number to identify your answers.

Solution

"To the metal" means to the closest edge of the contacts. Therefore, the area of all sources and drains are the same, a rectangle which is 2μm by 11μm. Thus,

$$R_{S1} = R_{D1} = (35\Omega/\text{sq.})(2/11) = 6.364\ \Omega$$

and

$$R_{S2} = R_{D2} = (80\Omega/\text{sq.})(2/11) = 14.546\ \Omega$$

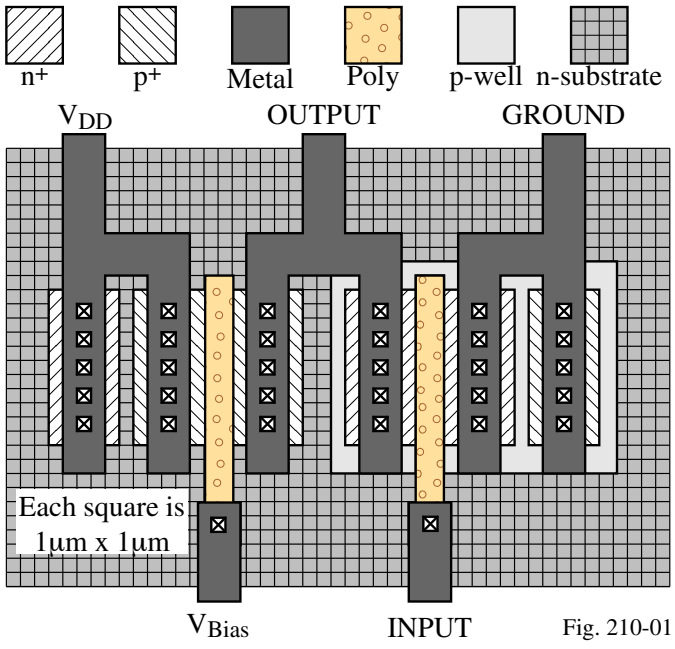


Fig. 210-01

Example 4

For the FETs of Example 1, find C_{GS}, C_{GD}, C_{BD}, and C_{BS} for each transistor. Assume that the voltage across the voltage dependent capacitors is zero and no channel is formed (cutoff). The various capacitances for this example are:

$C_{ox} = 0.7\text{fF}/\mu\text{m}^2$

LD(NMOS) = 0.45μm LD(PMOS) = 0.6μm

n+ diffusion to p-well (junction, bottom) = $0.33\text{fF}/\mu\text{m}^2$

n+ diffusion sidewall (junction, sidewall) = 0.9fF/μm

p+ diffusion to substrate (junction, bottom) = $0.38\text{fF}/\mu\text{m}^2$

p+ diffusion sidewall (junction, sidewall) = 1.0fF/μm

n-channel to bulk (junction, bottom) = $0.1\text{fF}/\mu\text{m}^2$

n-channel to bulk (junction, sidewall) = 0.3fF/μm

p-channel to bulk (junction, bottom) = $0.1\text{fF}/\mu\text{m}^2$

p-channel to bulk (junction, sidewall) = 0.3fF/μm

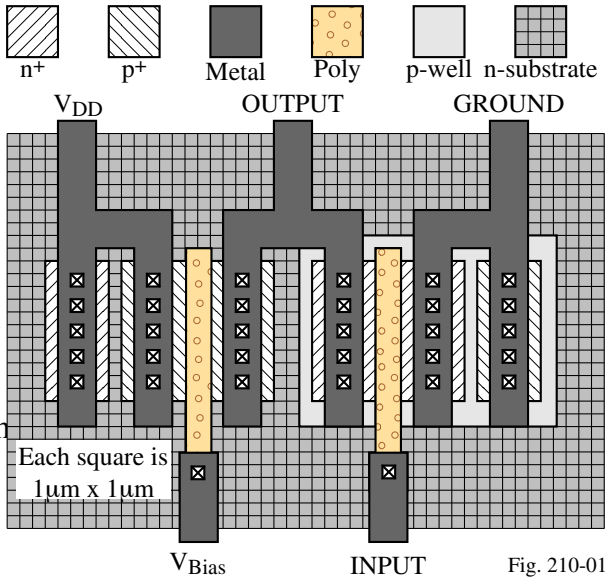


Fig. 210-01

Example 4 - Continued

Solution

The area for all sources and drains is a rectangle 5μm by 11μm.

Thus for M1,

$C_{GD1} = C_{GS1} = \text{LD(NMOS)xWx}C_{ox}$

$= 0.45\mu\text{m}\cdot 11\mu\text{m}\cdot 0.7\text{fF}/\mu\text{m}^2 = 3.465\text{ fF}$

$\boxed{C_{GD1} = C_{GS1} = 3.465\text{ fF}}$

$C_{BS1} = C_{BD1} = \text{W}\cdot\text{L}\cdot 0.33\text{fF}/\mu\text{m}^2 + 2(\text{W}+\text{L})0.9\text{fF}/\mu\text{m}^2$

$= 5\cdot 11\cdot 0.33 + 32\cdot 0.9 = 18.15+28.8 = 46.95\text{ fF}$

$\boxed{C_{BS1} = C_{BD1} = 46.95\text{ fF}}$

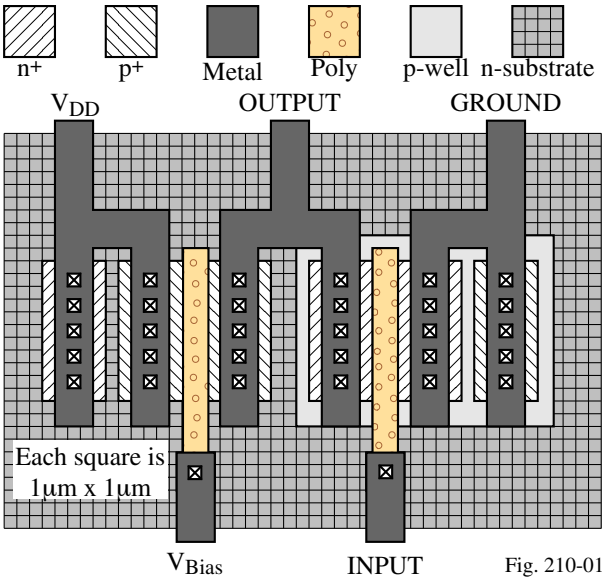


Fig. 210-01

For M2, we get

$\boxed{C_{GD2} = C_{GS2} = \text{LD(PMOS)xWx}C_{ox} = 0.6\mu\text{m}\cdot 11\mu\text{m}\cdot 0.7\text{fF}/\mu\text{m}^2 = 4.62\text{ fF}}$

$C_{BS2} = C_{BD2} = \text{W}\cdot\text{L}\cdot 0.38\text{fF}/\mu\text{m}^2 + (2\text{W}+2\text{L})\cdot 1.0\text{fF}/\mu\text{m}^2$

$= 5\cdot 11\cdot 0.38 + 32\cdot 1.0 = 20.9 + 32 = 52.9\text{ fF}$

$\boxed{C_{BS2} = C_{BD2} = 52.9\text{ fF}}$

Example 5

Draw the schematic of the circuit indicated below in the BJT layout and identify the collector, base and emitter terminals.

Solution

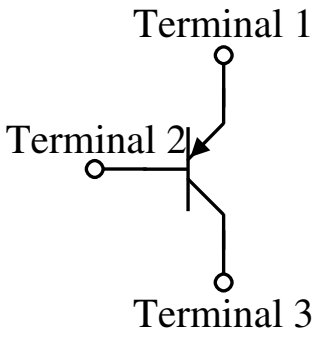


Fig. 210-05

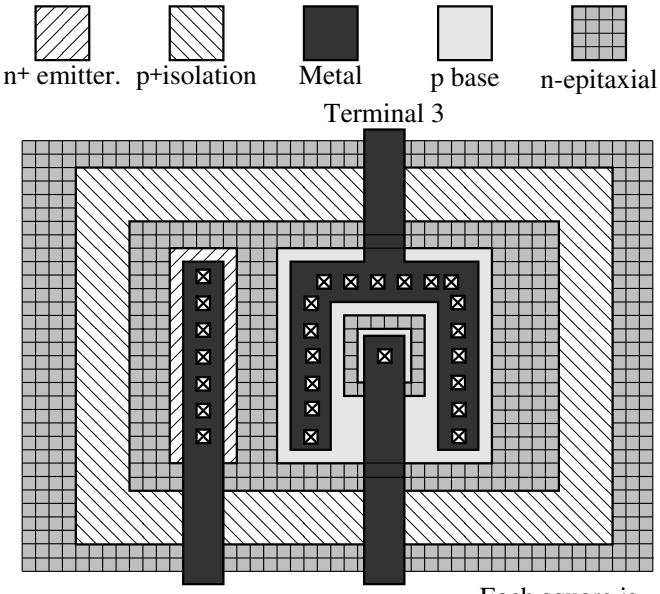


Fig. 210-04

Example 6

Draw the A-A' cross-section to scale. The approximate physical thicknesses are:

- n^+ emitter diffusion 1.3μm
- p-base diffusion 2.6μm
- n-epitaxial layer 10μm
- n^+ buried collector diffusion (not seen from the top view) - into the epitaxial layer 4μm and into the substrate 8μm
- All oxide and metal thickness are approximately 1μm.

(You may approximate the oxides and diffusions with straight edges for simplicity.)

Solution

See layout.

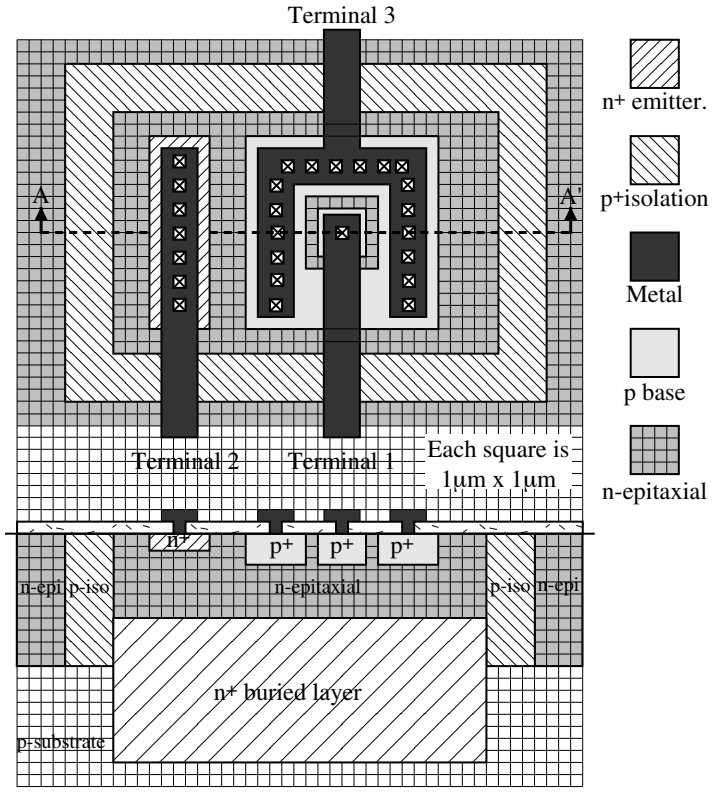
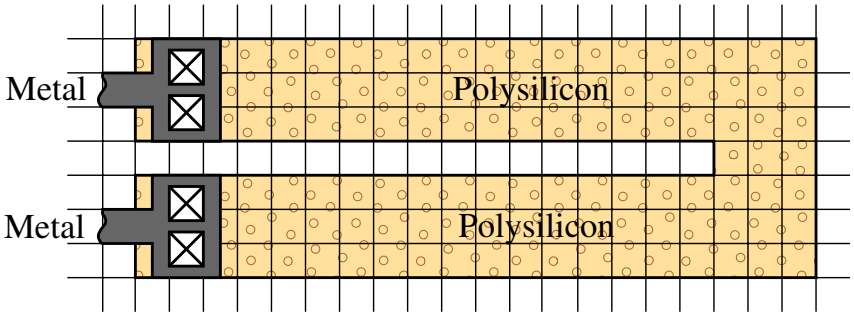


Fig. 210-06

Example 7

What is the resistance of the poly resistor shown if the sheet resistance is 30Ω/sq.?



Corner squares should have 1/2 of the normal sheet resistance

Fig. 210-07

Solution

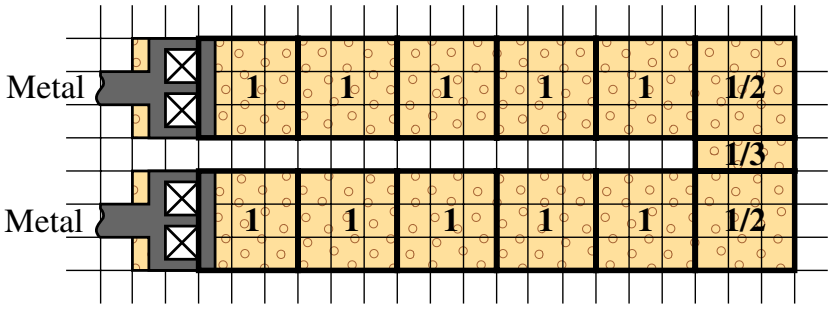


Fig. 210-08

Resistance = (10squares + 0.5sq. + 0.5sq. + 0.33sq.)x30Ω/sq. = 339Ω

Example 8

A layout of two PMOS transistors both having a W/L of 20μm/2μm is shown. One of the layouts is concentric (M1) and the other is rectangular (M2). Find the value of C_{BD}, C_{BS}, C_{GD} and C_{GS} for both transistors. Assume zero-bias for any voltage dependent capacitors and that both transistors are saturated.

C_{ox} = 0.7fF/μm^2

LD(NMOS) = 0.45μm LD(PMOS) = 0.6μm

n+ diffusion to p-well (junction, bottom) = 0.33fF/μm^2

n+ diffusion sidewall (junction, sidewall) = 0.9fF/μm

p+ diffusion to substrate (junction, bottom) = 0.38fF/μm^2

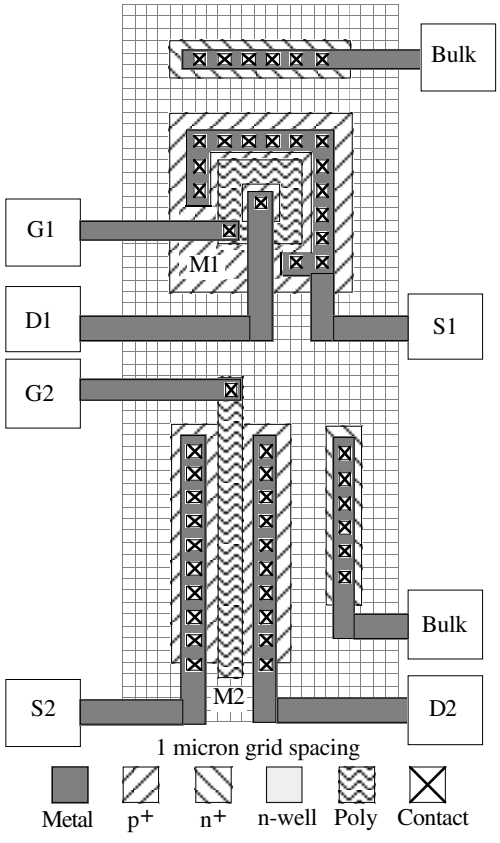
p+ diffusion sidewall (junction, sidewall) = 1.0fF/μm

n-channel to bulk (junction, bottom) = 0.1fF/μm^2

n-channel to bulk (junction, sidewall) = 0.3fF/μm

p-channel to bulk (junction, bottom) = 0.1fF/μm^2

p-channel to bulk (junction, sidewall) = 0.3fF/μm



Example 8 – Continued

Solution

M1:

$A_{S1} = (15x15 - 7x7) = 176\mu^2$ $A_{D1} = 3x3 = 9\mu^2$

$P_{S1} = 4x15 + 4x7 = 88\mu$ $P_{D1} = 4x3 = 12\mu$

$C_{BD1} = 9\mu^2 x 0.38fF/\mu^2 + 12\mu x 1.0fF/\mu$ $\boxed{C_{BD1} = 15.42\ fF}$

$C_{BS1} = 176\mu^2 x 0.38fF/\mu^2 + 88\mu x 1.0fF/\mu = 155fF$ $\boxed{C_{BS1} = 155\ fF}$

$C_{GS1} = C_{ox} \cdot W \cdot LD + 0.667 C_{ox} \cdot W \cdot L$

$= 0.7fF/\mu^2 \cdot 28\mu \cdot 0.6\mu + 0.667 \cdot 0.7fF/\mu^2 \cdot 20\mu \cdot 2\mu = 30.4\ fF$

$\therefore$ $\boxed{C_{GS1} = C_{GS2} = 30.4\ fF}$

$\boxed{C_{DG1} = 0.7fF/\mu^2 \cdot 12\mu \cdot 0.6\mu = 5.04\ fF}$

M2:

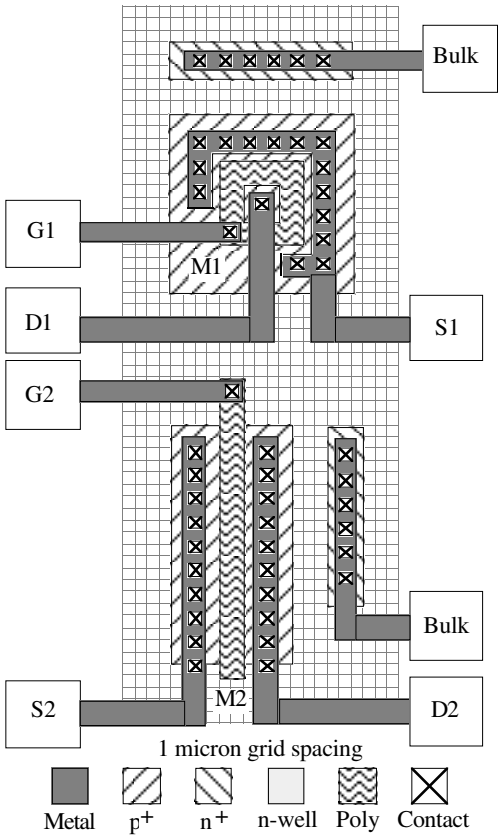
$A_{S2} = A_{D2} = 4x20 = 80\mu^2$, $P_{S2} = P_{D2} = 4+4+20+2 = 48\mu$

$C_{BD2} = C_{BS2} = 80\mu^2 x 0.38fF/\mu^2 + 48\mu x 1.0fF/\mu = 78.4fF$

$\therefore$ $\boxed{C_{BD2} = C_{BS2} = 78.4\ fF}$

$\boxed{C_{DG2} = 0.7fF/\mu^2 \cdot 20\mu \cdot 0.6\mu = 8.4\ fF}$

$\boxed{C_{GS2} = 0.7fF/\mu^2 \cdot 20 \cdot 0.6\mu\ 0.667 \cdot 0.7fF/\mu^2 \cdot 20\mu \cdot 2\mu = 27.07\ fF}$



SUMMARY

- Understanding the physical layout of transistors and passive components is very important for analog integrated circuit design
- The physical perspective gives the designer a feeling for the parasitics associated with the active and passive components
- Extraction of these parasitics requires knowledge of the physical layout

