LECTURE 215 – CHAPTER 2 – REVIEW PROBLEMS
(READING: Text-Chapter 2)

Chapter 2 Topics

- Integrated Circuit Technology
- Bipolar Technology
- Passive Components in Bipolar Technology
- CMOS Technology
- CMOS Technology-Compatible Devices
- BiCMOS Technology

Problem 1

(a.) Sketch the approximate side view of a NMOS transistor in a p-substrate. Identify each region and identify the connections at the top surface of the integrated circuit for the source, drain, gate and bulk/substrate.

Solution

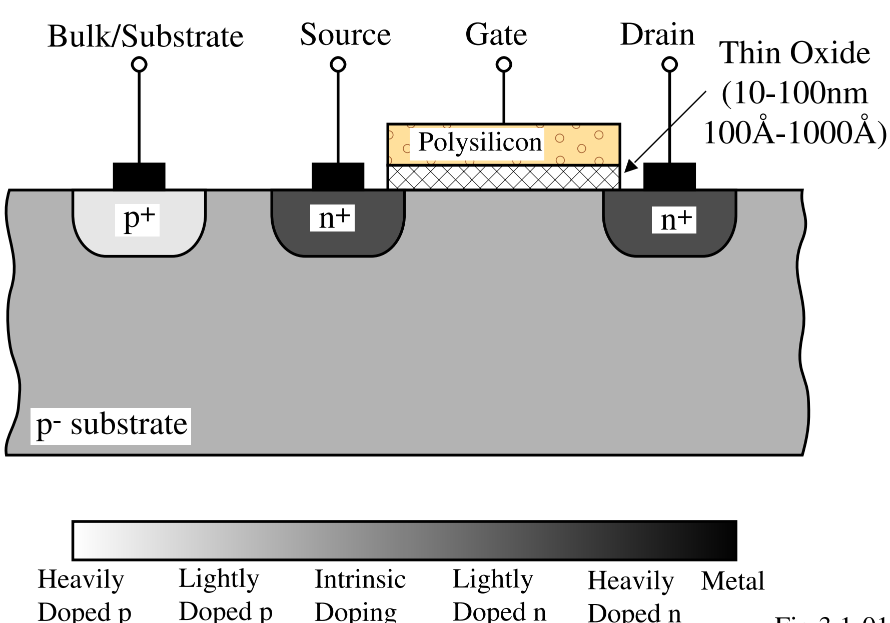
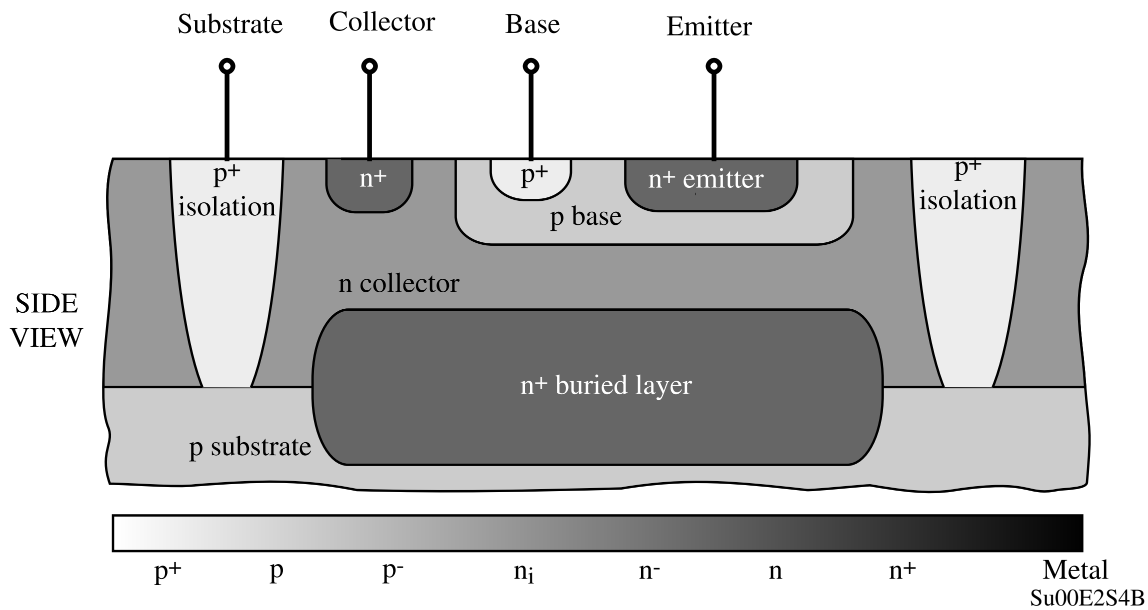


Fig.3.1-01

Problem 1 - Continued

(b.) Sketch the approximate side view of a NPN vertical transistor in an n-epitaxial region which is on top of a p-substrate. Identify each region (including the n+ buried layer) and identify the connection at the top surface of the integrated circuit for the base, emitter, collector and substrate.

Solution



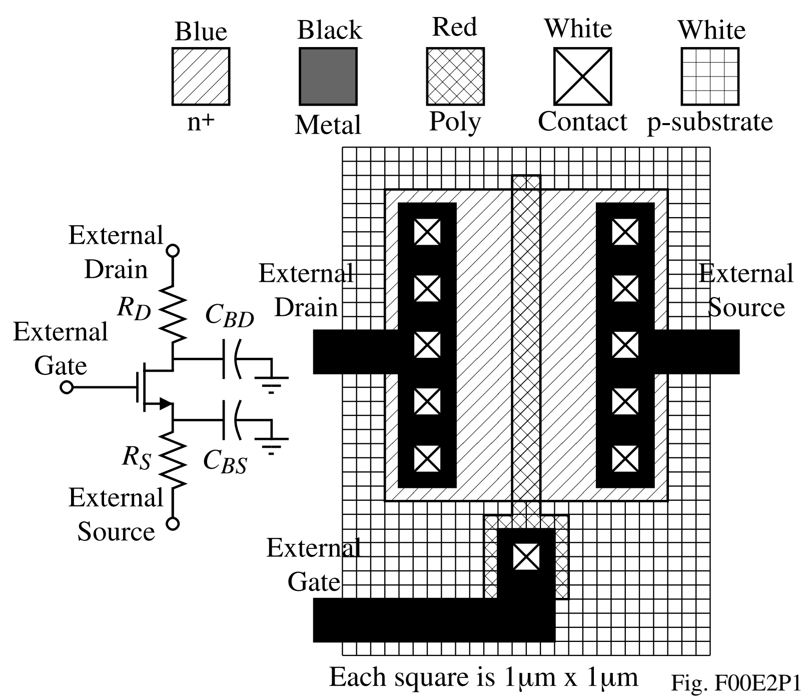
Problem 2

A layout of a NMOS transistor is shown.

(a.) Find the values of *RD*, and *RS* in the schematic shown if the sheet resistance of the n+ is 35 Ω/sq. and the resistance of a single contact is 1Ω.

(b.) Find the values of C_{BD} and C_{BS} assuming the transistor is cutoff and the drain and source are at ground potential if *CJ* and *CJSW* for an NMOS transistor are $770\text{x}10^{-6}$ F/m^2 and $380\text{x}10^{-12}$F/m. Assume the capacitors are lumped and appear on the source/drain side of the bulk resistors in part (a.).

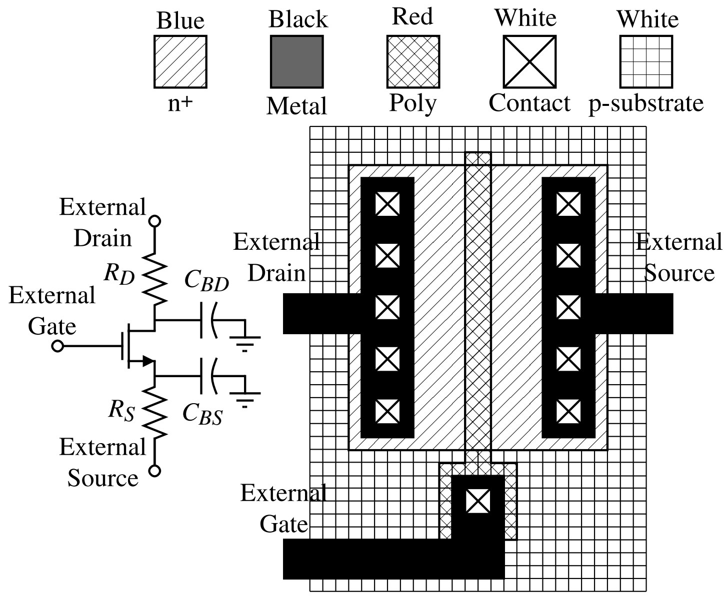
(c.) What is the W and L of this transistor?



(d.) If the overlap capacitor/unit length is $220\text{x}10^{-12}$F/m, what is C_{GD}?

Problem 2 – Continued

Solution



Each square is 1µm x 1µm Fig. F00E2P1

(a.) The area between the edge of the contacts to the polysilicon is 5µm by 22µm. This represents a bulk resistance of (5/22)x35 Ω/sq. = 7.95Ω. Adding 5 contacts in parallel gives

$\underline{RD = RS = 7.95\Omega + 0.2\Omega = 8.15\Omega}$.

(b.) The area or the source and drain are equal and are 9µm by 22µm or 198µm². The perimeter of the source and drain are 2(9µm+22µm) or 62µm. Therefore,

$$C_{BD} = C_{BS} = 770\text{x}10^{-6}\text{F/m}^2 \text{ x} 198\text{x}10^{-12}\text{m}^2 + 380\text{x}10^{-12}\text{F/m x } 62\text{x}10^{-6}\text{m}$$

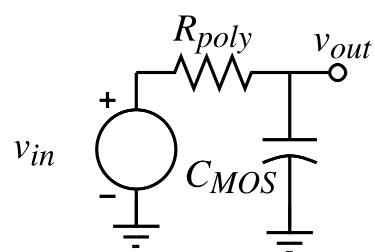
$$\underline{C_{BD} = C_{BS} = 152\text{fF} + 24\text{fF} = 176\text{fF}}$$

(c.) The $\underline{W = 22\mu m}$ and the $\underline{L = 2\mu m}$.

(d.) The overlap capacitor is

$$\underline{C_{GD} = 220\text{x}10^{-12}\text{F/m x } 22\text{x}10^{-6}\text{m} = 4.8\text{fF}}$$

Problem 3



F00E2P2

A simple first-order filter shown is to be built with a polysilicon resistor and a MOS capacitor. The polysilicon resistor has a sheet resistance of 50Ω/sq. ± 30% and is 5µm wide. The MOS capacitor is 2fF/µm² ± 10%. The -3dB frequency of the lowpass filter is 1MHz. (a.) Choose the size of the resistor (the number of squares, N) to minimize the total area of the filter including both the resistor and the capacitor. Find the area of the resistor and the capacitor in µm² and their values. (b.) Using the worst-case tolerance of the resistor and capacitor, find the maximum and minimum -3dB frequencies.

Solution

(a.) Value of $R = 50\Omega/\text{sq.x}N \text{ sq.} = 50N\ \Omega$

Value of $C = 2\text{fF}/\mu\text{m}^2\text{x}A_C\mu\text{m}^2 = 2A_C$ fF

Area of $C = A_C$

Area of $R = A_R = 25\mu\text{m}^2\text{x}N = 25N\ \mu\text{m}^2$

Total Area $= A_T = (25N + A_C)\ \ \mu\text{m}^2$

We know that the RC product is given as

$$RC = \frac{1}{2\pi\text{x}10^6} = (50N)(2A_C\text{x}10^{-15}) = NA_C\text{x}10^{-13} \qquad \therefore\ A_C = \frac{1}{2\pi\text{x}10^{-7}N}$$

Problem 3 - Continued

Thus, $A_T = 25N + \dfrac{1}{2\pi \text{x} 10^{-7} N} \rightarrow \dfrac{dA_T}{dN} = 25 - \dfrac{1}{2\pi \text{x} 10^{-7} N^2} = 0$

$\therefore\ N = \dfrac{1}{\sqrt{50\pi \text{x} 10^{-7}}} = 252 \ \Rightarrow\ \underline{A_R = 252\text{x}25\mu\text{m}^2 = 6308\mu\text{m}^2}$ and $\underline{A_C = 6308\mu\text{m}^2}$

Also, $\underline{R_{poly} = R = 252\text{x}50\Omega = 12.6\text{k}\Omega}$ and $\underline{C_{MOS} = 6308\mu\text{m}^2\text{x}2\text{fF}/\mu\text{m}^2 = 12.6\text{pF}}$

(b.)

$$\text{Maximum -3dB frequency} = \frac{1}{2\pi(0.7)(12.6\text{k}\Omega)(0.9)(12.6\text{pF})} = \underline{1.6\text{MHz}}$$

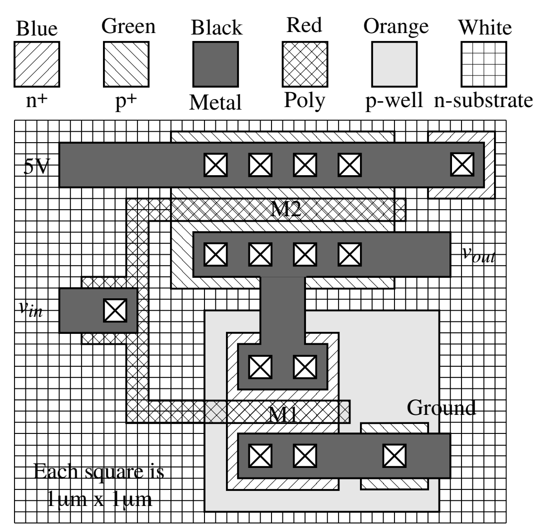
$$\text{Minimum -3dB frequency} = \frac{1}{2\pi(1.3)(12.6\text{k}\Omega)(1.1)(12.6\text{pF})} = \underline{0.7\text{MHz}}$$

Problem 4

A CMOS amplifier is shown along with the top view of the circuit layout assuming a p-well CMOS technology. Find the values of the capacitors shown in the circuit if

Type	P-Channel	N-Channel	Units
CGDO (CGSO)	220×10^{-12}	220×10^{-12}	F/m
CGBO	700×10^{-12}	700×10^{-12}	F/m
CJ	560×10^{-6}	770×10^{-6}	F/m^2
CJSW	350×10^{-12}	380×10^{-12}	F/m
MJ	0.5	0.5	
MJSW	0.35	0.38	
$2\lvert\phi_F\rvert$	0.7	0.8	V

Based on an oxide thickness of 140 or Cox=24.7×10^{-4} F/m^2.



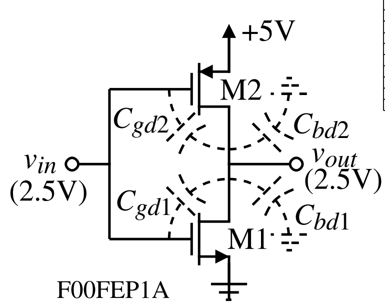
Solution

$C_{gd1} = 220 \times 10^{-12} \cdot 10\text{x}10^{-6}$

$\underline{C_{gd1} = 2.2\text{fF}}$

$C_{gd2} = 220 \times 10^{-12} \cdot 20\text{x}10^{-6}$

$\underline{C_{gd1} = 4.4\text{fF}}$



Problem 4 - Continued

Next, we must find the area and perimeter of each drain.

AD1 = 60µm^2 & PD1 = 32µm

AD2 = 120µm^2 & PD2 = 52µm

$$C_{bd1} = \frac{CJ\cdot AD1}{\left(1+\frac{2.5V}{2|\phi_F|}\right)^{MJ}} + \frac{CJSW\cdot PD1}{\left(1+\frac{2.5V}{2|\phi_F|}\right)^{MJSW}} = \frac{770\text{x}10^{-6}\cdot 60\text{x}10^{-12}}{\left(1+\frac{2.5V}{0.8}\right)^{0.5}} + \frac{380\text{x}10^{-12}\cdot 32\text{x}10^{-6}}{\left(1+\frac{2.5V}{0.8}\right)^{0.38}}$$

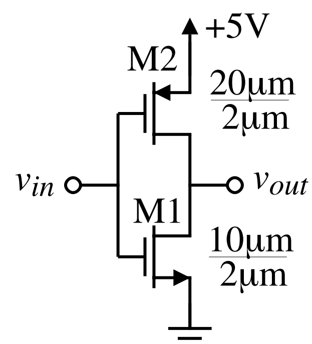
$$\underline{\underline{C_{bd1} = 22.75\text{fF} + 7.10\text{fF} = 29.84\text{fF}}}$$

$$C_{bd2} = \frac{CJ\cdot AD2}{\left(1+\frac{2.5V}{2|\phi_F|}\right)^{MJ}} + \frac{CJSW\cdot PD2}{\left(1+\frac{2.5V}{2|\phi_F|}\right)^{MJSW}} = \frac{560\text{x}10^{-6}\cdot 120\text{x}10^{-12}}{\left(1+\frac{2.5V}{0.7}\right)^{0.5}} + \frac{350\text{x}10^{-12}\cdot 52\text{x}10^{-6}}{\left(1+\frac{2.5V}{0.7}\right)^{0.35}}$$

$$\underline{\underline{C_{bd2} = 31.43\text{fF} + 10.69\text{fF} = 42.12\text{fF}}}$$

Problem 5

A CMOS circuit is shown. Assume a p-well CMOS technology and draw the complete layout for the NMOS and PMOS transistors that has *minimum* rectangular area for the source and drain diffusions. Some pertinent design rules are listed below.



F99E1P1A

- DR1 = distance from the square contact to diffusion from polysilicon = 2µm
- DR2 = all contacts are to be square with a dimension of 2µm by 2µm
- DR3 = the overlap of the contact by the diffusion or poly = 2µm
- DR4 = min. separation between n$^+$ diffusion and p-well = 2µm
- DR5 = minimum overlap of contact by metal = 1µm
- DR6 = poly must overlap the channel by 1µm

All metal widths are to be 4µm. Put as many contacts between the metal and diffusions as possible. Show the metal connections between transistors and indicate where metal goes for connections from transistors to external connections (v_{in} and v_{out} must be in metal). Use the indicated scheme below for identifying the various regions. If you wish to use colored pencil, use the scheme below or indicate which colors pertain to which region.

Problem 5 – Continued

Solution

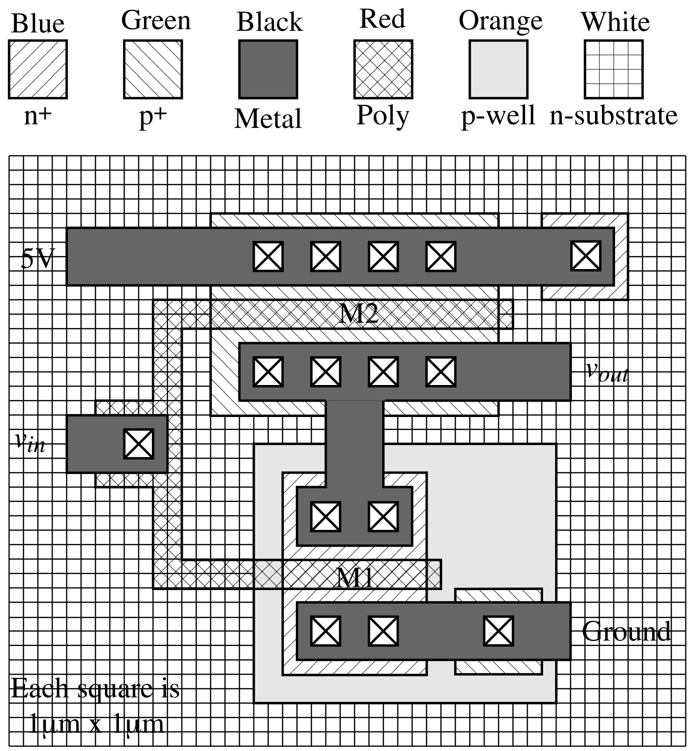
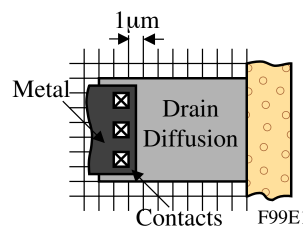


Fig. F99E1S1B

Problem 6

This problem consists of a number of short questions



F99E1P3A

1. What is the resistance of the drain if the sheet resistance of n^+ diffusion is 10Ω/sq.? What is the drain-bulk capacitance assuming V_{BD} =0V if bottom capacitance is 0.33pF/μm^2 and the sidewall capacitance is 0.9fF/μm?

   $R_{n+} \approx 10\Omega/\text{sq.x}\,\frac{8}{7} = 11.43\Omega$ $\boxed{R_{n+} = 11.43\Omega}$

   $C_{BD} = 0.33\text{pF}/\mu\text{m}^2\text{x}70\mu\text{m}^2 + 0.9\text{fF}/\mu\text{mx}34\mu\text{m} = 23.1\text{fF}+30.6\text{fF} = 53.7\text{fF}$

   $\boxed{C_{BD} = 53.7\text{fF}}$

2. Why are contacts normally square and minimum size?
   They are square because that is minimum area and they are minimum size because different size contacts do not etch evenly so small contacts are chosen for minimum contact area. Larger contacts are done by repeated use of minimum size contacts.

3. What is the function of the field oxide (FOX) in a CMOS technology? The function of field oxide is to isolate the substrate from conductors on the surface.

Problem 6 – Continued

4. How are two BJT transistors fabricated in the same substrate electrically isolated from each other?

   Each BJT is fabricated in its own n-epitaxial region surrounded on all sides by p material. This pn junction is reversed biased to electrically isolate the two transistors.

5. Assume that a 1kΩ resistance of an IC process has a voltage coefficient of -1000ppm/V. What is the resistance value if the average voltage across the resistor is increased from 0 to 5V?

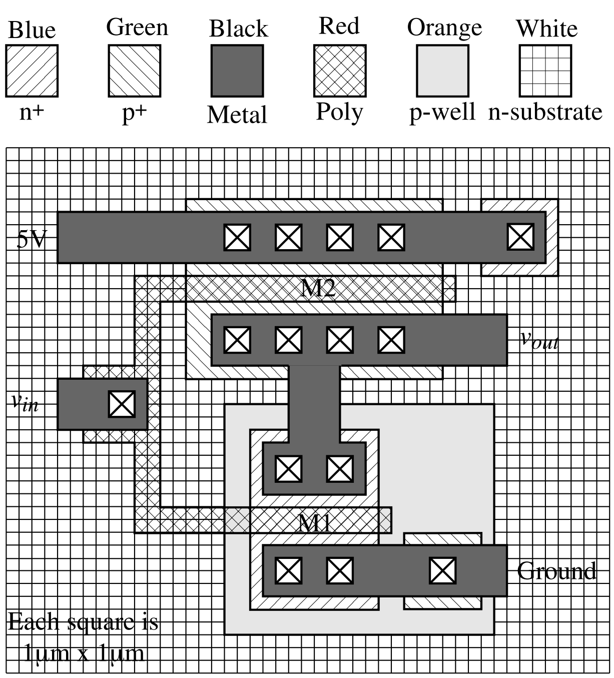
$$R(5\text{V}) = R(0\text{V}) - \frac{1000}{1{,}000{,}000}\, 5\text{V} \times 1000\Omega = 1000\Omega - 5\Omega = 995\Omega \quad \boxed{R(5\text{V}) = 995\Omega}$$

6. List the 5 capacitances associated with the MOSFET operating in the saturation region and tell whether this capacitance is depletion or parallel plate or both.

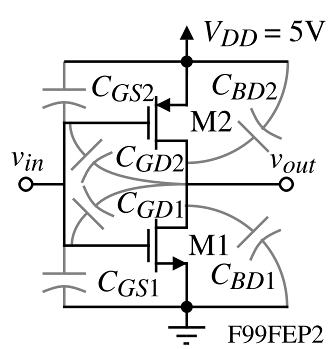
   1.) Gate -drain which is parallel plate
   2.) Gate-source which is both parallel plate and depletion
   3.) Bulk-drain which is depletion
   4.) Bulk-source which is depletion
   5.) Gate-bulk which is parallel plate

Problem 7

A top view of a CMOS push-pull amplifier is shown. Find the numerical value of all capacitances shown on the schematic. Assume that the dc value of the output is 2.5V and the MJ and MJSW is 0.5 for both transistors.



F99FEP2B



F99FEP2

Problem 7 - Continued

Solution

M1:

$W_1 = 10\mu m$, $L_1 = 2\mu m$, $AS_1 = AD_1 = 6x10 = 60\mu m^2$, $PS_1 = PD_1 = 32\mu m$

$C_{GD1} = 10\mu m\cdot 0.45\mu m\cdot 0.7fF/\mu m^2 = \underline{\underline{3.15fF}}$

$$C_{BD1} = \frac{[60\mu m^2\cdot 0.33fF/m^2 + 32\mu m\cdot 0.9fF/\mu m]}{\sqrt{1+\frac{2.5}{0.6}}} = \underline{\underline{21.38fF}}$$

$C_{GS1} = 10\mu m\cdot 0.45\mu m\cdot 0.7fF/\mu m^2 + 0.67[20\mu m^2\cdot 0.7fF/m^2] = \underline{\underline{12.48fF}}$

M2:

$W_2 = 20\mu m$, $L_2 = 2\mu m$, $AS_2 = AD_2 = 6x20 = 120\mu m^2$, $PS_2 = PD_2 = 52\mu m$

$C_{GD2} = 20\mu m\cdot 0.6\mu m\cdot 0.7fF/\mu m^2 = \underline{\underline{8.4fF}}$

$$C_{BD2} = \frac{[120\mu m^2\cdot 0.38fF/m^2 + 52\mu m\cdot 1fF/\mu m]}{\sqrt{1+\frac{2.5}{0.6}}} = \underline{\underline{42.94fF}}$$

$C_{GS2} = 20\mu m\cdot 0.6\mu m\cdot 0.7fF/\mu m^2 + 0.67[40\mu m^2\cdot 0.7fF/m^2] = \underline{\underline{27fF}}$

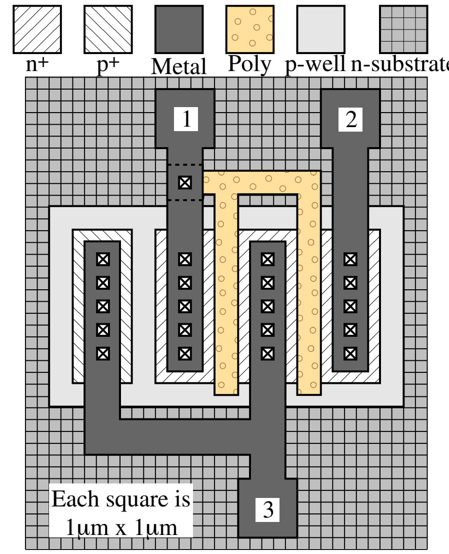
Problem 8

This problem consists of a number of short questions

1. List three functions of polysilicon.
   (1)__Gate of a MOS transistor____________________
   (2)__Ohmic connection between two points________________
   (3)__Resistor______________________________
   (4)__Capacitor plate___________________________
2. In a CMOS technology, list three functions for the n^+ or p^+ diffusions.
   (1)___They can form the source or drain of a MOSFET____________
   (2)___They are used to make an ohmic contact with metal____________
   (3)___They can be used as a resistor______________________
   (4)___Capacitor plate___________________________
3. Nitride is only used to define the active areas of transistors. True___ or False_X_
4. How are two NMOS transistors fabricated in the same substrate electrically isolated from each other?
   They are fabricated in an oppositely doped substrate so that they can be reverse biased and thus isolated from the substrate and from each other.__________
5. What is the purpose of masks in an integrated circuit fabrication process?
   To allow selective processing of an area of a wafer.____________

Problem 9

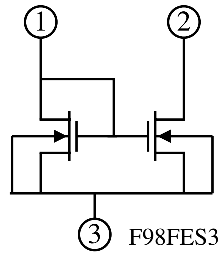
A CMOS layout is shown. (a.) Draw the schematic corresponding to this layout. What is this circuit? (b.) Find the value of C_{BD}, C_{BS}, C_{GD} and C_{GS} of all transistors. Assume zero-bias for any voltage dependent capacitors and that all transistors are saturated.



F98FEP3

Solution

(a.) The schematic for this circuit is shown. The circuit is a simple NMOS current mirror.



(b.) There are two transistors that are identical. The drain areas and peripheries are:

$$AD = 5x13 = 65\mu m^2,\ \ PD = 10+26 = 36\mu m$$

The sources are shared. We will simply divide the bulk-source capacitances by two using the above area and periphery for the source.

$$C_{BD} = 0.33fF/\mu m^2 x 65\mu m^2 + 0.9fF/\mu m x 36\mu m = 21.4fF + 32.4fF = 53.85fF$$

$$C_{BS} = 0.5xC_{BD} = 26.9fF \qquad C_{GD} = C_{OL} = 13\mu m x 0.45\mu m x 0.7fF/\mu m^2 = 4.1fF$$

$$C_{GS} = C_{OL}+0.67 \cdot W \cdot L \cdot C_{ox} = C_{OL}+0.67x13\mu m x 2\mu m x 0.7fF/\mu m^2 = 4.1fF+12.1fF = 16.2fF$$

$$\therefore \boxed{C_{BD} = 53.85fF,\ C_{BS} = 26.9fF,\ C_{GD} = 4.1fF,\ \text{and}\ C_{GS} = 16.2fF}$$