Problem 1 - (20 points - This problem is required)

If the folded-cascode op amp shown having a small-signal voltage gain of 7464V/V is used as a comparator, find the dominant pole if $C_L = 5\text{pF}$. If the input step is 10mV, determine whether the response is linear or slewing and find the propagation delay time. Assume the parameters of the NMOS transistors are $K_N' = 110\text{V/µA}^2$, $V_{TN} = 0.7\text{V}$, $\lambda_N = 0.04\text{V}^{-1}$ and for the PMOS transistors are $K_P' = 110\text{V/µA}^2$, $V_{TP} = -0.7\text{V}$, $\lambda_P = 0.05\text{V}^{-1}$.

Solution

$V_{OH}$ and $V_{OL}$ can be found from many approaches. The easiest is simply to assume that $V_{OH}$ and $V_{OL}$ are 2.5V and –2.5V, respectively. However, no matter what the input, the values of $V_{OH}$ and $V_{OL}$ will be in the following range,

$$(V_{DD} - 2V_{ON}) < V_{OH} < V_{DD} \quad \text{and} \quad V_{DD} < V_{OH} < (V_{SS} + 2V_{ON})$$

The reasoning is as follows, suppose $V_{in} > 0$. This gives $I_1 > I_2$ which gives $I_5 < I_7$ which gives $I_9 < I_7$. $V_{out}$ will increase until $I_7$ equals $I_9$. The only way this can happen is for $M_5$ and $M_7$ to leave saturation. The same reasoning holds for $V_{in} < 0$.

Therefore assuming that $V_{OH}$ and $V_{OL}$ are 2.5V and –2.5V, respectively, we get

$$V_{in}(\text{min}) = \frac{5\text{V}}{7464} = 0.67\text{mV} \quad \rightarrow \quad k = \frac{10\text{mV}}{0.67\text{mV}} = 14.93$$
The folded-cascode op amp as a comparator can be modeled by a single dominant pole. This pole is found as,

\[ p_1 = \frac{1}{R_{out}C_L} \text{ where } R_{out} = g_{m9}r_{ds9}r_{ds11} || [g_{m9}r_{ds7}(r_{ds2} || r_{ds5})] \]

\[ g_{m9} = \sqrt{2.75 \cdot 110 \cdot 36} = 771 \mu S, \quad g_{ds9} = g_{ds11} = 75 \times 10^{-6} \cdot 0.04 = 3 \mu S, \quad g_{ds2} = 50 \times 10^{-6} (0.04) = 2 \mu S \]

\[ g_{m7} = \sqrt{2.75 \cdot 50 \cdot 80} = 775 \mu S, \quad g_{ds5} = 125 \times 10^{-6} \cdot 0.05 = 6.25 \mu S, \quad g_{ds7} = 50 \times 10^{-6} (0.05) = 3.75 \mu S \]

\[ g_{m9}r_{ds9}r_{ds11} = (771 \mu S) \left( \frac{1}{3 \mu S} \right) \left( \frac{1}{3 \mu S} \right) = 85.67 \text{ M\Omega} \]

\[ g_{m7}(r_{ds2} || r_{ds5}) = (775 \mu S) \left( \frac{1}{2 \mu S} \right) \left( \frac{1}{6.25 \mu S} \right) = 25.05 \text{ M\Omega} , \]

\[ R_{out} = 85.67 \text{ M\Omega} || 25.05 \text{ M\Omega} = 19.4 \text{ M\Omega} \]

The dominant pole is found as, \[ p_1 = \frac{1}{R_{out}C_L} = \frac{1}{19.4 \times 10^6 \text{ pF}} = 10,318 \text{ rps} \]

The time constant is \( \tau_1 = 96.9 \mu s \).

For a dominant pole system, the step response is, \( v_{out}(t) = A_{vd}(1-e^{-t/\tau_1})V_{in} \)

The slope is the largest at \( t = 0 \). Evaluating this slope gives,

\[ \frac{dv_{out}}{dt} = \frac{A_{vd}}{\tau_1} e^{-t/\tau_1}V_{in} \quad \text{For } t = 0, \text{ the slope is } \frac{A_{vd}}{\tau_1} V_{in} = \frac{7464}{96.9 \mu s} \text{ (10mV)} = 0.77 \text{V/\mu s} \]

The slew rate of this op amp/comparator is \( SR = \frac{I_3}{C_L} = \frac{100 \mu A}{5 \text{ pF}} = 20 \text{V/\mu s} \)

Therefore, the comparator does not slew and its propagation delay time is found from the linear response as,

\[ t_p = \tau_1 \ln\left( \frac{2k}{2k-1} \right) = 96.9 \mu s \ln\left( \frac{2 \cdot 14.93}{2 \cdot 14.93 - 1} \right) = (96.9 \mu s)(0.0341) = 3.3 \mu s \]
Problem 2 - (20 points - This problem is required)

A comparator consists of an amplifier cascaded with a latch as shown below. The amplifier has voltage gain of 10V/V and $f_{-3dB} = 100MHz$ and the latch has a time constant of 10ns. The maximum and minimum voltage swings of the amplifier and latch are $V_{OH}$ and $V_{OL}$. When should the latch be enabled after the application of a step input to the amplifier of $0.05(V_{OH}-V_{OL})$ to get minimum overall propagation time delay? What is the value of the minimum propagation time delay? It may useful to recall that the propagation time delay of the latch is given as $t_p = \tau_L \ln \left( \frac{V_{OH}-V_{OL}}{2v_{il}} \right)$ where $v_{il}$ is the latch input ($\Delta V_i$ of the text).

\[ v_{in} = 0.05(V_{OH}-V_{OL}) \]

\[
\begin{align*}
&\text{Amplifier} \quad A_v(0)=10V/V \quad f_{-3dB}=100MHz \\
&\text{Latch} \quad \tau_L=10ns \\
&\text{Comparator}
\end{align*}
\]

\[ v_{oa} \]

\[ v_{il} \]

\[ v_{out} \]

\[ v_{in} = 0.05(V_{OH}-V_{OL}) \]

\[ t=0 \]

\[ \frac{v_{oa}}{v_{il}} \]

\[ t_1 = \frac{1}{\omega_{3dB}} \ln \left( \frac{1}{1-2x} \right) \]

From the propagation time delay of the latch we get,

\[ t_2 = \tau_L \ln \left( \frac{V_{OH}-V_{OL}}{2v_{il}} \right) = \tau_L \ln \left( \frac{1}{2} \right) \]

\[ \therefore t_p = t_1 + t_2 = \frac{1}{\omega_{3dB}} \ln \left( \frac{1}{1-2x} \right) + \tau_L \ln \left( \frac{1}{2} \right) \quad \text{gives} \quad x = \frac{\pi}{1+2\pi} = 0.4313 \]

\[ t_1 = \frac{10ns}{2\pi} \ln (1+2\pi) = 1.592ns \cdot 1.9856 = 3.16ns \quad \text{and} \quad t_2 = 10ns \ln \left( \frac{1+2\pi}{2\pi} \right) = 1.477ns \]

\[ \therefore t_p = t_1 + t_2 = 3.16ns + 1.477ns = 4.637ns \]
Problem 3 - (20 points - This problem is optional)

If \( R_1 = R_2 \) of the circuit shown, find an expression for the small-signal output resistance \( R_{out} \) ignoring \( R_L \). Repeat including the influence of \( R_L \) on the output resistance. Let \( R_1 = R_2 \) and \( R_L = 1k\Omega \), dc currents through M1 and M2 be 500\( \mu \)A, \( W_1/L_1 = 100\mu m/1\mu m \) and \( W_2/L_2 = 200\mu m/1\mu m \). Find the value of \( R_{out} \).

**Solution**

The loop-gain for this network can be written from inspection as,

\[
LG = \left( \frac{R_1}{R_1+R_1} \right) \left( \frac{g_{m1}+g_{m2}}{g_{ds1}+g_{ds2}+G_L} \right)
\]

Therefore, since the output is shunt feedback we can solve for output resistance as,

\[
R_{out} = \frac{r_{ds1}||r_{ds2}}{1+\left( \frac{R_1}{R_1+R_1} \right) \left( \frac{g_{m1}+g_{m2}}{g_{ds1}+g_{ds2}+G_L} \right)}
\]

Setting \( G_L = 0 \) \((R_L = \infty)\) gives the output resistance not including the load resistor, \( R_L \), as

\[
R_{out}(R_L = \infty) = \frac{50k\Omega||40k\Omega}{1 + 0.5 \left( \frac{3316+3162}{25+20} \right) } = \frac{22.22k\Omega}{72.98} = 304\Omega
\]

\[
R_{out}(R_L = 1k\Omega) = \frac{50k\Omega||40k\Omega||1k\Omega}{1 + 0.5 \left( \frac{3316+3162}{25+20+1000} \right) } = \frac{957\Omega}{4.0995} = 233\Omega
\]

As usual, straight-forward small-signal models are faster, summing the currents at the output,

\[
I_{out} = V_{out} \left[ \frac{1}{r_{ds1}} + \frac{1}{r_{ds2}} + \frac{1}{R_1+R_2} + \frac{g_{m1}+g_{m2}}{2} + \frac{1}{R_L} \right] = V_{out} \left[ \frac{1}{r_{ds1}} + \frac{1}{r_{ds2}} + \frac{g_{m1}+g_{m2}}{2} + \frac{1}{R_L} \right]
\]

\[
\therefore R_{out} = \left[ \frac{1}{r_{ds1}} + \frac{1}{r_{ds2}} + \frac{g_{m1}+g_{m2}}{2} + \frac{1}{R_L} \right]^{-1} = 304\Omega \ (R_L = \infty)
\]

\[
R_{out} = 233\Omega \ (R_L = 1k\Omega)
\]

(Principle: Feedback is a great concept tool but a terrible analysis tool.)
Problem 4 - (20 points - This problem is optional)

A current mirror load, CMOS differential amplifier is shown. The current in M5 is 100µA. Assume the parameters of the NMOS transistors are \( K_N' = 110 \text{V/µA}^2 \), \( V_{TN} = 0.7 \text{V} \), \( \lambda_N = 0.04 \text{V}^{-1} \) and for the PMOS transistors are \( K_P' = 110 \text{V/µA}^2 \), \( V_{TP} = 0.7 \text{V} \), \( \lambda_P = 0.04 \text{V}^{-1} \). (a.) Find the small-signal output resistance and voltage gain if the \( W/L \) ratio of M1 and M2 is 100µm/1µm. (b.) If the \( W/L \) ratio of M3 and M4 is 50µm/1µm and \( C_{ox} = 24.7 \times 10^{-4} \text{F/m}^2 \), and the effective output capacitance is 1pF, find all roots of this amplifier (ignore the influence of \( C_{gd4} \)). (c.) What is the –3dB frequency in Hertz?

**Solution**

The small-signal model suitable for this problem is shown below.

The roots of this circuit are,

\[ p_1 = - \frac{g_{m3} \ C_1}{C_1 g_{m3} + 1} = -6.072 \times 10^9 \text{rps} \]

\[ p_2 = - \frac{g_{ds2} + g_{ds4} C_2}{C_2} = -4.504 \times 10^6 \text{rps} \]

\[ f_{3dB} = \frac{4.504 \times 10^6}{2\pi} = 717 \text{kHz} \]
Problem 5 - (20 points - This problem is optional)

The simplified schematic of a feedback amplifier is shown. Use the method of feedback analysis to find \( \frac{v_2}{v_1} \), \( R_{in} = \frac{v_1}{i_1} \), and \( R_{out} = \frac{v_2}{i_2} \). Assume that all transistors are matched and that \( \beta = 100 \), \( r_{\pi} = 5k\Omega \) and \( r_o = \infty \).

Solution

Open-loop, quasi-ac model:

Small-signal, open-loop model:

\[
R_i = \frac{v_s}{i_{b1}} = r_{\pi} + (1+\beta)(R_2\|R_4) = 5k\Omega + (101)(1k\Omega\|20k\Omega) = 101.19k\Omega
\]

\[
a = \frac{v_o}{v_s} = \left( \frac{v_o}{i_{b1}} \right) \left( \frac{i_{b2}}{i_{b1}} \right) \left( \frac{i_{b3}}{i_{b2}} \right) \left( \frac{i_{b1}'}{i_{b3}'} \right) \frac{v_s'}{v_s} = \frac{-\beta R_5}{R_5 + r_{\pi} + (1+\beta)[R_6\|R_2+R_4]} \left( \frac{-\beta R_3}{R_3 + r_{\pi}} \right) \frac{1}{R_i}
\]
\[
= \frac{[(101)(954.55)](-8.976)(-66.67)(1/101.19k\Omega)}{570.16 V/V}
\]

\[
f = \frac{R_2}{R_2+R_4} = \frac{1}{2.17} = 0.0476 \quad \text{and} \quad R_0 = \frac{v_o'}{i_{b1}'} = R_6\|R_2+R_4||\frac{R_{\pi}+R_5}{1+\beta} = 128.5\Omega
\]

Closed-loop quantities are:

\[
A_{vf} = \frac{v_o}{v_s} = \frac{a}{1+af} = \frac{570.16}{1+27.15} = 20.25, \quad R_{if} = (1+af)R_i = 2.848M\Omega
\]

\[
\therefore \quad R_{out} = R_{of} = \frac{R_0}{1+Av_{vf}} = \frac{128.5\Omega}{28.15} = 4.565\Omega
\]

\[
R_{in} = R_1+R_{if} = 2.858M\Omega \quad \text{and} \quad \frac{v_2}{v_1} = \frac{R_{if}}{R_1+R_{if}} = 20.18 V/V
\]
Problem 6 - (20 points - This problem is optional)

A voltage follower feedback circuit is shown. For the MOS transistor, \( I_D = 0.5\text{mA}, K' = 180\mu\text{A/V}^2, r_{ds} = \infty \), and \( W/L = 100 \). Although, the bulk effect, \( g_{mbst} \), should be considered, for simplicity ignore the bulk effects in this problem. For the op amp, assume that \( R_i = 1\text{M}\Omega, R_o = 10\text{k}\Omega \), and \( a_v = 1000 \). Calculate the input resistance and output resistance using Blackman’s formula given below.

\[
R_{out} = R_{out} \quad \text{(Controlled Source Gain=0)} \left[ \frac{1 + RR(\text{output port shorted})}{1 + RR(\text{output port open})} \right]
\]

**Solution**

Circuit for calculating the return ratios.

Input Port:

\[
R_{in}(a_v=0) = R_i + \left( \frac{1}{g_m} \right), \quad g_m = \sqrt{2 \cdot 500 \cdot 100 \cdot 180} = 4.243\text{mS}
\]

\[
R_{in}(a_v=0) = 1\text{M}\Omega + 236\Omega = 1\text{M}\Omega
\]

\( RR(\text{input port shorted}) \):

\[
V_r = -g_mR_i \ V_2 \quad \text{and} \quad V_2 = a_vV_t - g_mR_i \ V_2 \rightarrow V_r = -a_v \ g_mR_i \ \frac{V_2}{1+g_mR_i} \ V_t
\]

\( RR(\text{input port shorted}) = \frac{V_r}{V_t} = \frac{-a_v \ g_mR_i}{1+g_mR_i} = \frac{1000 \cdot 4.243\text{mS} \cdot 1\text{M}\Omega}{1+4.243\text{mS} \cdot 1\text{M}\Omega} = -999.8
\]

\( RR(\text{input port open}) \):

\( RR(\text{input port open}) = 0 \) because \( V_r = 0 \)

\[
R_{in} = R_{in} \quad (a_v=0) \left[ \frac{1 + RR(\text{output port shorted})}{1 + RR(\text{output port open})} \right] = 1\text{M}\Omega(1+999.8) = 1000.8\text{M}\Omega
\]

Output Port:

\[
R_{out}(a_v=0) = R_i \ ||\left( \frac{1}{g_m} \right) = 236\Omega
\]

\( RR(\text{output port shorted})\):

\( RR(\text{output port shorted}) = 0 \) because \( V_r = 0 \)

\( RR(\text{output port open}) \):

Same as the \( RR \) for the input port shorted.

\[
R_{out} = R_{out} \quad (a_v=0) \left[ \frac{1 + RR(\text{output port shorted})}{1 + RR(\text{output port open})} \right] = 236\Omega \left( \frac{1+0}{1+999.8} \right) = 0.236\Omega
\]
Problem 7 – (20 points – This problem is optional)

A CMOS op amp capable of operating from 1.5V power supply is shown. All device lengths are 1µm and are to operate in the saturation region. Design all of the W values of every transistor of this op amp to meet the following specifications.

<table>
<thead>
<tr>
<th>Specification</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Slew rate</td>
<td>±10V/µs</td>
</tr>
<tr>
<td>( V_{out(max)} )</td>
<td>1.25V</td>
</tr>
<tr>
<td>( V_{out(min)} )</td>
<td>0.75V</td>
</tr>
<tr>
<td>( V_{ic(min)} )</td>
<td>1V</td>
</tr>
<tr>
<td>( V_{ic(max)} )</td>
<td>2V</td>
</tr>
<tr>
<td>GB</td>
<td>10MHz</td>
</tr>
<tr>
<td>Phase margin</td>
<td>60°</td>
</tr>
<tr>
<td>Output pole</td>
<td>2GB</td>
</tr>
<tr>
<td>RHP zero</td>
<td>10GB</td>
</tr>
<tr>
<td>Mirror pole</td>
<td>≥ 10GB</td>
</tr>
</tbody>
</table>

Your design should meet or exceed these specifications. Ignore bulk effects in this problem and summarize your W values to the nearest micron, the value of \( C_c \) (pF), and \( I \) (µA) in the following table. Use the following model parameters: \( K_N' = 24\mu A/V^2 \), \( K_P' = 8\mu A/V^2 \), \( V_{TN} = -0.75V \), \( \lambda_N = 0.01V^{-1} \), and \( \lambda_P = 0.02V^{-1} \).

Solution

1.) \( p_2 = 2GB \Rightarrow g_{m6}/C_L = 2g_{m1}/C_c \) and \( z = 10GB \Rightarrow g_{m6} = 10g_{m1} \). \( C_c = C_L/5 = 2pF \)

2.) \( I = C_c \cdot SR = (2x10^{-12}) \cdot 10^7 = 20\mu A \) \( \therefore I = 20\mu A \)

3.) \( GB = g_{m1}/C_c \Rightarrow g_{m1} = 20\pi x 10^6 \cdot 2x10^{-12} = 40\pi x 10^{-6} = 125.67\mu S \)

\[
\frac{W_1}{L_1} = \frac{W_2}{L_2} = \frac{g_{m1}^2}{2K_N(I/2)} = \frac{(125.67x10^{-6})^2}{2\cdot 24x10^{-6} \cdot 10x10^{-6}} = 32.9 \Rightarrow W_1 = W_2 = 33\mu m
\]

4.) \( V_{ic(min)} = V_{DS5(sat)} + V_{GS1(10\mu A)} = 1V \rightarrow V_{DS5(sat)} = 1 - \sqrt{\frac{2 \cdot 10}{24 \cdot 33}} - 0.75 = 0.0908 \)

\( V_{DS5(sat)} = 0.0908 = \sqrt{\frac{2 \cdot 1}{K_N S_5}} \rightarrow W_5 = \frac{2 \cdot 20}{24 \cdot (0.0908)^2} = 201.9\mu m \quad W_5 = 202\mu m \)

5.) \( V_{ic(max)} = V_{DD} - V_{SD11(sat)} + V_{TN} = 1.5 - V_{SD11(sat)} + 0.75 = 2V \rightarrow V_{SD11(sat)} = 0.25V \)

\( V_{SD11(sat)} \leq \sqrt{\frac{2 \cdot 1.5I}{K_P S_{11}}} \rightarrow S_{11} = W_{11} \geq \frac{2 \cdot 30}{(0.25)^2} \cdot 8 = 120 \rightarrow W_{11} = W_{12} \geq 120\mu m \)
Problem 7 - Continued
6.) Choose $S_3(S_4)$ by satisfying $V_{ic}(\text{max})$ specification then check mirror pole.

$$V_{ic}(\text{max}) \geq V_{GS3}(20\mu A) + V_{TN} \rightarrow V_{GS3}(20\mu A) = 1.25V \geq \sqrt{\frac{2\cdot I}{K_N\cdot S_3}} + 0.75V$$

$$S_3 = S_4 = \frac{2\cdot 20}{(0.5)^2 \cdot 24} = 6.67 \Rightarrow W_3 = W_4 = 7\mu m$$

7.) Check mirror pole ($p_3 = \frac{g_{m3}}{C_{Mirror}}$).

$$p_3 = \frac{g_{m3}}{C_{Mirror}} = \frac{g_{m3}}{2\cdot 0.667\cdot W_3\cdot L_3\cdot \text{Cox}} = \frac{\sqrt{2\cdot 24\cdot 6.67\cdot 20\times 10^{-6}}}{2\cdot 0.667\cdot 6.67\cdot 0.5\times 10^{-15}} = 17.98\times 10^9$$

which is much greater than $10GB (0.0628\times 10^9)$. Therefore, $W_3$ and $W_4$ are OK.

8.) $g_{m6} = 10g_{m1} = 1256.7\mu S$

a.) $g_{m6} = \sqrt{2K_N S_6 I}\Rightarrow W_6 = 164.5\mu m$

b.) $V_{out}(\text{min}) = 0.5 \Rightarrow V_{DS6}(\text{sat}) = 0.5 = \sqrt{2\cdot I_{6} K_N S_6} \Rightarrow W_6 = 66.67\mu m$

Therefore, use $W_6 = 165\mu m$

Note: For proper mirroring, $S_4 = \frac{I_4}{I_6} S_6 = 8.25\mu m$ which is close enough to 7$\mu m$.

9.) Use the $V_{out}(\text{max})$ specification to design $W_7$.

$$V_{out}(\text{max}) = 0.25V \geq V_{DS7}(\text{sat}) = \sqrt{\frac{2\cdot 200\mu A}{8\times 10^{-6}\cdot S_7}}$$

$$\therefore S_7 \geq \frac{400\mu A}{8\times 10^{-6}(0.25)^2} \Rightarrow W_7 = 800\mu m$$

10.) Now to achieve the proper currents from the current source $I$ gives,

$$S_9 = S_{10} = \frac{S_7}{10} = 80 \Rightarrow W_9 = W_{10} = 80\mu m$$

and

$$S_{11} = S_{12} = \frac{1.5\cdot S_7}{10} = 120 \Rightarrow W_{11} = W_{12} = 120\mu m.$$ We saw in step 5 that $W_{11}$ and $W_{12}$ had to be greater than 120$\mu m$ to satisfy $V_{ic}(\text{max})$. \therefore $W_{11}=W_{12}=120\mu m$

11.) $P_{diss} = 15I\cdot 1.5V = 300\mu A\cdot 1.5V = 450\mu W$

<table>
<thead>
<tr>
<th>$C_c$</th>
<th>$I$</th>
<th>$W_1=W_2$</th>
<th>$W_3=W_4$</th>
<th>$W_5=W_8$</th>
<th>$W_6$</th>
<th>$W_7$</th>
<th>$W_9=W_{10}$</th>
<th>$W_{11}=W_{12}$</th>
<th>$P_{diss}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>2pF</td>
<td>20$\mu A$</td>
<td>33$\mu m$</td>
<td>7$\mu m$</td>
<td>202$\mu m$</td>
<td>165$\mu m$</td>
<td>800$\mu m$</td>
<td>80$\mu m$</td>
<td>120$\mu m$</td>
<td>450$\mu W$</td>
</tr>
</tbody>
</table>
Problem 8 – (20 points – This problem is optional)

A differential CMOS amplifier using depletion mode input devices is shown. Assume that the normal MOSFETs parameters are $K_N' = 110\text{V}/\mu\text{A}^2$, $V_{TN} = 0.7\text{V}$, $\lambda_N = 0.04\text{V}^{-1}$ and for the PMOS transistors are $K_P' = 110\text{V}/\mu\text{A}^2$, $V_{TP} = 0.7\text{V}$, $\lambda_P = 0.04\text{V}^{-1}$. For the depletion mode NMOS transistors, the parameters are the same as the normal NMOS except that $V_{TN} = -0.5\text{V}$. (a.) What is the maximum input common-mode voltage, $V_{icm}^+(\text{max})$? (b.) What is the minimum input common-mode voltage, $V_{icm}^-(\text{min})$? (c.) What value of $V_{DD}$ gives an $ICMR = 0.5V_{DD}$?

Solution

(a.) $V_{icm}^+(\text{max}) = V_{DD} - V_{SD3}(\text{sat}) - V_{DS1}(\text{sat}) + V_{GS1}(50\mu\text{A})$

$$i_D = \frac{\beta}{2} (V_{GS1} - V_{T1})^2 \rightarrow \quad V_{GS1} = \sqrt{\frac{2i_D}{\beta}} + V_{T1} = V_{DS1}(\text{sat}) + V_{T1}$$

$\therefore \quad V_{icm}^+(\text{max}) = V_{DD} - 0.4472 - 0.5 = V_{DD} - 0.9472$

(b.) $V_{icm}^-(\text{min}) = V_{DS5}(\text{sat}) + V_{GS1}(50\mu\text{A}) = V_{DS5}(\text{sat}) + V_{DS1}(\text{sat}) + V_{T1}$

$V_{icm}^-(\text{min}) = \sqrt{\frac{2I_{D3}}{\beta_3}} + \sqrt{\frac{2I_{D1}}{\beta_1}} + V_{T1} = 0.1348 + 0.0953 - 0.5 = -0.2698\text{V}$

(c.) $ICMR = V_{icm}^+(\text{max}) - V_{icm}^-(\text{min}) = V_{DD} - 0.9472 + 0.2698 = V_{DD} - 0.6774$

$\therefore \quad V_{DD} - 0.6774 = 0.5V_{DD} \rightarrow \quad V_{DD} = 2(0.6774) = 1.355\text{V}$