Homework Assignment No. 6 - Solutions

Problem 1 - (10 points)
For the CMOS op amp shown, find the following quantities.

1.) Slew rate (V/sec.)
2.) Positive and negative output voltage limits (all transistors remain in saturation)
3.) Positive and negative input common voltage limits (all transistors remain in saturation and use nominal parameter values)
4.) Small signal voltage gain
5.) Unity-gain bandwidth (MHz) and 6.) Power dissipation (mW).

Solution

1.) \( SR = \frac{I_S}{C_c} = \frac{50\mu A}{5pF} = 10^7 V/\text{second} \quad \Rightarrow \quad SR = 10^7 V/\text{sec} \)

2.) \( V_{SD7} = \sqrt{\frac{2I_7}{K_p(W/L)}} = \sqrt{\frac{500\mu A}{50-50}} = 0.447V \) and \( V_{DS6} = \sqrt{\frac{500\mu A}{110-50}} = 0.3015V \)
\[ \therefore \quad V_{out}(\text{max}) = 2.5-0.447 = 2.053V \]
\[ \quad \text{and} \]
\[ \quad V_{out}(\text{min}) = -2.5+0.3015V = -2.198V \]

3.) \( ICM(\text{min}) = -2.5V+V_{GSS} - |V_{TP}| = -2.5V+\sqrt{\frac{2.25}{110-10}}+0.7V-0.7V \)
\[ \therefore ICM(\text{min}) = -2.5+0.213 = -2.287V \quad \Rightarrow \quad ICM(\text{min}) = -2.287V \]

\( ICM(\text{max}) = ? \quad V_{SD5}(\text{sat}) = \sqrt{\frac{2.50}{50-10}} = 0.4472V \) and \( V_{SG1} = \sqrt{\frac{2.25}{50-10}}+0.7 = 1.016V \)
\[ \therefore ICM(\text{max}) = 2.5-V_{SD5}(\text{sat})-V_{SG1} = 2.5-0.4472-1.016 = 1.0366V \]
\[ \quad \text{ICM(\text{max}) = 1.0366V} \]

4.) \( A_v = \frac{g_{m1}g_{m6}}{(g_{sd2}+g_{ds4})(g_{ds6}+g_{sd7})} \quad g_{m1} = \sqrt{\frac{2K_pW_1I_1}{L_1}} = \sqrt{2.50-10-25} = 158\mu S \)
\[ g_{m6} = \sqrt{\frac{2K_pW_6I_6}{L_6}} = \sqrt{2.50-50-250} = 1118\mu S \]
\[ G_I = 0.09-250\mu A = 22.5\mu S \]
\[ \therefore A_v = \frac{158\cdot 1118}{2.25-22.5} = 3.489V/V \quad \Rightarrow \quad A_v = 3.489V/V \]

5.) \( GB = \frac{g_{m1}}{C_c} = \frac{158\mu S}{5pF} = 31.6\text{Mrads/sec} \quad \Rightarrow \quad GB = 5.03MHz \)

6.) \( P_{diss} = 5\times 350\mu A = 1.75mW \quad \Rightarrow \quad P_{diss} = 1.75mW \)
Problem 2 - (10 points)

Bias current calculation:

\[ V_{I8} + V_{ON8} + I_8 \cdot R_S = V_{dd} - V_{ss} \quad \text{or} \quad V_{T8} + \frac{2I_8}{3K_p} = 5 - I_8 \cdot R_S \]  

(1)

Solving for \( I_8 \) quadratically would give, \( I_8 \approx 36\mu A \), \( I_5 \approx 36\mu A \), and \( I_7 \approx 60\mu A \)

Using the formula, \( g_m = \sqrt{2K_p \frac{W}{L} I} \) and \( g_{ds} = \lambda I \) we get,

\[ g_{m2} = 60\mu S \quad g_{ds2} = 0.9\mu S \quad g_{ds4} = 0.72\mu S \]  

(2)

\[ g_{m6} = 363\mu S \quad g_{ds6} = 3\mu S \quad g_{ds7} = 2.4\mu S \]  

(3)

Small-signal open-loop gain:

The small-signal voltage gain can be expressed as,

\[ A_{V1} = \frac{-g_{m2}}{g_{ds2} + g_{ds4}} = -37 \quad \text{and} \quad A_{V2} = \frac{-g_{m6}}{g_{ds6} + g_{ds7}} = -67 \]

Thus, total open-loop gain is,

\[ A_v = A_{V1} \cdot A_{V2} = 2489\text{V/V} \]  

(3)

Output resistance:

\[ R_{out} = \frac{1}{g_{ds6} + g_{ds7}} = 185\text{K\Omega} \]  

(5)

Power dissipation:

\[ P_{diss} = 5(36 + 36 + 60)\mu W = 660\mu W \]  

(6)

ICMR:

\[ V_{on,max} = 2.5 - V_{T1} - V_{ON1} - V_{ON5} = 0.51V \]  

(7)

\[ V_{on,min} = 2.5 - V_{T1} + V_{T3} + V_{ON5} = -2.21V \]  

(8)

Output voltage swing:

\[ V_{L,\text{max}} = 2.5 - V_{ON7} = 1.81V \]  

(9)

Slew Rate:

Slew rate under no load condition can be given as,

\[ SR = \frac{I_5}{C_C} = 6V/\mu s \]

In presence of a load capacitor of 20 pF, slew rate would be,

\[ SR = \min \left[ \frac{I_5}{C_C}, \frac{I_7}{C_L} \right] \]
Problem 6.3-7 - Continued

CMRR:

Under perfectly balanced condition where \( I_1 = I_2 \), if a small signal common-mode variation occurs at the two input terminals, the small signal currents \( i_1 = i_2 = i_3 = i_4 \) and the differential output current at node (7) is zero. So, ideally, common-mode gain would be zero and the value for CMRR would be infinity.

GBW:

Let us design M9 and M10 first. Both these transistors would operate in triode region and will carry zero dc current. Thus, \( V_{ds9} = V_{ds10} \equiv 0 \). The equation of drain current in triode region is given as,

\[
I_D = K' \frac{W}{L}(V_{GS} - V_T) \phi_{ds}.
\]

The on resistance of the MOS transistor in triode region of operation would be,

\[
R_{ON} = K' \frac{W}{L}(V_{GS} - V_T).
\]

It is intended to make the effective resistance of M9 and M10 equal to \( \frac{1}{g_{m6}} \).

So,

\[
K' \frac{W_9}{L_9} (V_{GS9} - V_{T9}) + K' \frac{W_{10}}{L_{10}} (V_{GS10} - V_{T10}) = g_{m6}
\]

(11)

\[
V_{d4} = V_{d3} = -2.5 + V_{T3} + V_{ON3} = -1.5 V
\]

Thus,

\[
V_{GS9} \equiv 4 V \quad \text{and} \quad V_{GS10} \equiv -1 V.
\]

Putting the appropriate values in (11), we can solve for the aspect ratios of M9 and M10. One of the solutions could be,

\[
K' \frac{W_9}{L_9} = \frac{1}{1} \quad \text{and} \quad K' \frac{W_{10}}{L_{10}} = \text{very small}
\]

(12)

The dominant pole could be calculated as,

\[
P_1 = - \left( \frac{g_{d4} + g_{d2}}{2\pi A_f C_C} \right) = -1.16 KHz.
\]

And the load pole would be,

\[
P_2 = - \left( \frac{g_{m6}}{2\pi C_L} \right) = -2.8 MHz.
\]

for a 20 pF load.

It can be noted that in this problem, the product of the open-loop gain and the dominant pole is approximately equal to the load pole. Thus, the gain bandwidth is approximately equal to 2.8 MHz and the phase margin would be close to 45 degrees.
Problem 6.3-7 - Continued

PSRR:

If a small ripple \( v_s \) is applied at the \( V_{dd} \) terminal, then the gain of this ripple from this terminal to the output can be expressed as,

\[
\frac{v_o}{v_s} = \frac{R_S}{g_{ds6} + g_{ds7}} \left( 1 + \frac{1}{g_m8} \right) \approx 2.8 \text{V/V}
\]

Thus, PSRR due to variations in \( V_{dd} \) would be, \( A_{PSRR} = \frac{2489}{2.8} = 889 \).

SPICE file:

```
.model nmos nmos vto=0.7 lambda=0.04 kp=110u
.model pmos pmos vto=-0.8 lambda=0.05 kp=50u

vdd 1 0 dc 2.5 ac 0
vss 10 0 dc -2.5 ac 0
vinp 5 0 dc 0 ac 1
*vinn 4 0 dc 0 ac 0

m8 2 2 1 1 pmos w=3u l=1u
rs 2 10 100k
m5 3 2 1 1 pmos w=3u l=1u
m1 6 8 3 3 pmos w=2u l=1u
m2 7 5 3 3 pmos w=2u l=1u
m3 6 6 10 10 nmos w=4u l=1u
m4 7 6 10 10 nmos w=4u l=1u
m7 8 2 1 1 pmos w=5u l=1u
m6 8 7 10 10 nmos w=10u l=1u
cc 7 9 6p
ci 8 0 20p
m9 8 1 9 9 nmos w=1u l=1u
m10 8 10 9 9 pmos w=1u l=100u

.op
.ac dec 10 1 100meg
.option post
.end
```

Operating points:

**** mosfets

```
subckt element 0:m8 0:m5 0:m1 0:m2 0:m3 0:m4
model 0:pmos 0:pmos 0:pmos 0:pmos 0:pmos 0:nmos
region Cutoff Cutoff Cutoff Cutoff Saturati Saturati
id -35.3708u -34.8506u -17.4107u -17.4399u 17.4107u 17.4399u
ibs 0. 0. 0. 0. 0. 0.
```
Problem 6.3-7 - Continued

| vgs  | -1.4629 | -1.4629 | -1.3517 | -1.3527 | 975.9818m | 975.9818m |
| vds  | -1.4629 | -1.1473 | -2.8768 | -2.8331 | 975.9818m | 1.0196   |
| vbs  | 0.0     | 0.0     | 0.0     | 0.0     | 0.0       | 0.0       |
| vth  | -800.0000m | -800.0000m | -800.0000m | -800.0000m | 700.0000m |
| vdsat| -662.9217m | -662.9217m | -551.7476m | -552.7377m | 275.9818m |
| 700.0000m | 275.9818m |

| beta | 160.9719u | 158.6045u | 114.3838u | 114.1657u | 457.1773u | 457.9449u |
| gam eff | 527.6252m | 527.6252m | 527.6252m | 527.6252m | 527.6252m | 527.6252m |
| gm   | 106.7118u | 105.1423u | 63.1110u  | 63.1037u  | 126.1726u | 126.3844u |
| gds  | 1.6480u   | 1.6480u   | 761.0636n | 763.7975n | 670.2604n | 670.2604n |
| gmb  | 36.9704u  | 36.4266u  | 21.8648u  | 21.8623u  | 43.7126u  | 43.7860u  |
| cdtot| 2.021e-18 | 1.585e-18 | 2.649e-18 | 2.609e-18 | 1.797e-18 | 1.878e-18 |
| cgtot| 7.005e-16 | 7.000e-16 | 4.693e-16 | 4.692e-16 | 9.467e-16 | 9.467e-16 |
| cbtot| 7.806e-18 | 7.806e-18 | 6.216e-18 | 6.205e-18 | 2.402e-17 | 2.402e-17 |
| cgd  | 2.021e-18 | 1.585e-18 | 2.649e-18 | 2.609e-18 | 1.797e-18 | 1.878e-18 |

| subckt element | 0:m7 | 0:m6 | 0:m9 | 0:m10 |
| model          | 0:pmos | 0:nmos | 0:nmos | 0:pmos |
| region         | Cutoff | Saturati | Linear | Cutoff |
| id             | -61.7971u | 61.7971u | 0.0 | 0.0 |
| ibs            | 0.0 | 0.0 | 0.0 | 0.0 |
| ibd            | 24.9901f | -25.0099f | 0.0 | 0.0 |
| vgs            | -1.4629 | 1.0196 | 2.4990 | -2.5010 |
| vds            | -2.4990 | 2.5010 | 0.0 | 0.0 |
| vbs            | 0.0 | 0.0 | 0.0 | 0.0 |
| vth            | -800.0000m | 700.0000m | 700.0000m | -800.0000m |
| vdsat          | -662.9217m | 319.5939m | 0.0 | 0.0 |
| beta           | 281.2376u | 1.2100m | 110.0000u | 500.0000n |
| gam eff        | 527.6252m | 527.6252m | 527.6252m | 527.6252m |
| gm             | 186.4385u | 386.7225u | 0.0 | 0.0 |
| gds            | 2.7467u   | 2.2471u   | 197.8911u | 850.4951n |
| gmb            | 64.5917u  | 133.9802u | 0.0 | 0.0 |
| cdtot          | 5.753e-18 | 1.152e-17 | 1.727e-16 | 17.2658f |
| cgtot          | 1.1698f   | 2.3660f   | 3.463e-16 | 34.6349f |
| cstot          | 1.1511f   | 2.3021f   | 1.727e-16 | 17.2658f |
| cbtot          | 1.301e-17 | 5.233e-17 | 9.769e-19 | 1.033e-16 |
| cgs            | 1.1511f   | 2.3021f   | 1.727e-16 | 17.2658f |
| cgd            | 5.753e-18 | 1.152e-17 | 1.727e-16 | 17.2658f |

Results from SPICE simulation:

i. Unloaded output (load capacitor = 0)
   \[ GBW = 1.5 \text{ MHz}, \text{ Phase Margin} = 90 \text{ deg}, 1\% \text{ settling time} = 0.39 \text{ us}. \]

ii. Loaded output (load capacitor = 20 pF)
   \[ GBW = 1.5 \text{ MHz}, \text{ Phase Margin} = 65 \text{ deg}, 1\% \text{ settling time} = 0.48 \text{ us}. \]
Problem 6.3-7 - Continued

Load Capacitance = 20 pF

Gain vs. Frequency

Load Capacitance = 0 pF

Gain vs. Frequency
Problem 6.3-7 - Continued

CL = 0 pF

1% settling time = 0.39 µs.

CL = 20 pF

1% settling time = 0.48 µs.
Problem 3 - (10 points)
Small signal differential voltage gain:
By intuitive analysis methods,
\[
\frac{v_{o1}}{v_{in}} = \frac{-0.5g_{m1}}{g_{ds1} + g_{ds3}}
\]
and
\[
\frac{v_{out}}{v_{o1}} = \frac{-g_{m4}}{g_{ds4} + g_{ds5}}
\]
\[
\therefore \frac{v_{out}}{v_{in}} = \frac{0.5g_{m1}g_{m4}}{(g_{ds1}+g_{ds3})(g_{ds4}+g_{ds5})}
\]
\[
g_{m1} = \sqrt{\frac{2K_NW_1I_{D1}}{L_1}} = \sqrt{24.2 \cdot 2.4 \cdot 10^{-6}} = 43.82 \mu S
\]
\[
g_{ds1} = \lambda_NI_{D1} = 0.01 \cdot 10 \mu A = 0.1 \mu S, \quad g_{ds3} = \lambda_PI_{D3} = 0.02 \cdot 10 \mu A = 0.2 \mu S
\]
\[
g_{m4} = \sqrt{\frac{2K_PW_4I_{P4}}{L_4}} = \sqrt{2.8 \cdot 10^{-6}} = 126.5 \mu S
\]
\[
g_{ds4} = \lambda_PI_{D4} = 0.02 \cdot 10 \mu A = 2 \mu S, \quad g_{ds5} = \lambda_NI_{D5} = 0.01 \cdot 10 \mu A = 1 \mu S
\]
\[
\therefore \frac{v_{out}}{v_{in}} = \frac{0.5 \cdot 43.82 \cdot 126.5}{(0.1+0.2)(1+2)} = 3.079 \text{V/V}
\]
Output resistance:
\[
R_{out} = \frac{1}{g_{ds4}+g_{ds5}} = \frac{10^6}{1+2} = 333 \text{k}\Omega
\]
Dominant pole, \( p_1 \):
\[
|p_1| = \frac{1}{R_1C_1} \quad \text{where} \quad R_1 = \frac{1}{g_{ds1}+g_{ds3}} = \frac{10^6}{0.1+0.2} = 3.33 \text{M}\Omega
\]
and
\[
C_1 = C_c(1+|I_{A_{v2}}|) = 5 \text{pF}\left( 1 + \frac{g_{m4}}{g_{ds4}+g_{ds5}} \right) = 5\left( 1 + \frac{126.5}{3} \right) = 215.8 \text{pF}
\]
\[
\therefore |p_1| = \frac{10^6}{3.33 \cdot 2.158} = 1.391 \text{rads/sec} \rightarrow |p_1| = 1.391 \text{rads/sec} = 221 \text{Hz}
\]
\[
GB = \frac{0.5g_{m1}}{C_1} = \frac{0.5 \cdot 43.82 \cdot 10^{-6}}{5 \times 10^{-12}} = 4.382 \text{Mrads/sec}
\]
\[
GB = 4.382 \text{ Mrads/sec} = 0.697 \text{MHz}
\]
\[
SR = \frac{I_{D6}}{C_c} = \frac{10 \mu A}{5 \text{pF}} = 2 \text{ V/\mu s}
\]
\[
P_{\text{diss}} = 10 \text{V}(140 \mu A) = 1.4 \text{mW}
\]
Problem 4 - Design Problem 2 (50 points)

**NMOS Characteristics**

\[ V_{th} = 0.662 \text{ V} \]

\[ g_{ds} = \lambda_n I_D \Rightarrow 29.8824 \mu = \lambda_n \times 1.1465 \text{ m} \]

\[ \Rightarrow \lambda_n = 0.026 \]

\[ g_m^2 = 2k_n' \frac{W}{L} I_D \Rightarrow [5.82 \times 10^{-3}]^2 = 2k_n' \times 100 \times 1.1465 \times 10^{-3} \]

\[ \Rightarrow k_n' = 149.86 \text{ mA/V}^2 \]

Therefore,

\[ \begin{cases} 
V_{th} = 0.662 \text{ V} \\
k_n' = 149.86 \text{ mA/V}^2 \\
\lambda_n = 0.026 
\end{cases} \]

forms the foundation to do the final design by hand calculation.
**PMOS Characteristics**

\[ V_{th} = -0.864 \text{ V} \]

\[ G_{ds} = \lambda_p I_D \Rightarrow 9.1481 \mu A = \lambda_p \times 87.3301 \mu A \]

\[ \Rightarrow \lambda_p = 0.105 \]

\[ g_m^2 = 2k' \frac{W}{L} I_D \Rightarrow \left[ 1.009 \times 10^{-3} \right]^2 = 2k' \times 100 \times 87.3301 \times 10^{-6} \]

\[ \Rightarrow k' = 58.3 \text{ mA/V}^2 \]

Therefore, \[ \begin{cases} V_{th} = -0.864 \text{ V} \\ k' = 58.3 \text{ mA/V}^2 \\ \lambda_p = 0.105 \end{cases} \]

forms the basis to do the initial design by trial calculation.
**Explanation:**

1. M10, M9, setup the bias voltage at gate of M9. Then M9, M5, M7 are current mirrors to setup the bias currents for differential pair and M7 is a constant current sink load with respect to M6.

2. M1, M2 differential pair with current mirror load consisting of M3 and M4. This is the first stage of the amplifier and the gain \( g_m = g_m \cdot R_i \). \( g_m = g_m' = g_m'' \) and \( R_i = R_{i1} || R_{i2} \).

3. M6 is a common source amplifier with a constant sink load to get a high gain hopefully.

4. M8 acts as a resistor AC wise to create nulling zeros with 4
1) Power consumption consideration:

\[ [2.5 - (-2.5)] I_{total} = 1 \text{ mW} \]

\[ \Rightarrow I_{total} \leq 200 \mu A \]

2) Phase margin \( > 60^\circ \) \( \Rightarrow \) \( C_C > 0.2 \Omega \ C_L \)

Now \( C_L = 10 \mu F \) \( \Rightarrow \) \( C_C > 2, \Omega \ P F \)

Let's use \( C_C = 3 \mu F \)

3) Slow Rate Consideration:

\[ BR = \frac{\delta \tau}{C_C} = \frac{I_5}{3 \mu F} \approx 10 \ V/\mu s \]

\[ \Rightarrow I_5 \geq 30 \mu A \]

Let's use \( I_5 = 30 \mu A \)

then the output stage current \( I_{Q6}, I_{Q7} \) are choose to be \( 5 I_5 = 150 \mu A \)

then we have use \( 180 \mu A \) now.
(4) **Output Stage**

**OVSR:**

\[ V_{\text{OVS}} = 2.5 - V_{\text{OS}} \text{ (cont.)} \]

\[ 150 = \frac{55.3}{2} \times 100 (\Delta V)^2 \]

\[ \Delta V = 0.927 \]

\[ \text{ie } V_{\text{OVS}} = 2.273 \]

\[ V_{\text{OVS}} = -2.5 + V_{\text{OS}} \text{ (cont.)} \]

\[ 150 = \frac{149.86}{2} \times 100 \times (\Delta V)^2 \]

\[ \Delta V = 0.142 \]

\[ \text{ie } V_{\text{OVS}} = -2.5 + 0.142 = -2.358 \]

Therefore, **OVSR** = $2.73 + 2.358 = 4.631 > 4.5 \quad \text{(OK)}$

For \( V_o = 0 \), normal bias operation.

**M6:**

\[ 150 = \frac{58.3}{2} \times 100 \times \left[ V_{\text{G6}} - 0.866 \right]^2 \left( 1 + 0.105 \times 2.1 \right) \]

\[ 3 = 18.2 \times \left[ V_{\text{G6}} - 0.866 \right]^2 \times 1.2625 \Rightarrow V_{\text{G6}} = 1.066 \]

\[ \text{ie } V_{\text{G6}} = 2.5 - 1.066 = 1.434 \text{ V} \]

**M7:**

\[ 150 = \frac{149.86}{2} \times 100 \times \left[ V_{\text{G7}} - 0.662 \right]^2 \left( 1 + 0.026 \times 2.4 \right) \]

\[ 3 = 149.86 \times \left[ V_{\text{G7}} - 0.662 \right]^2 \times 1.05 \Rightarrow V_{\text{G7}} = 0.8 \]

\[ \text{ie } V_{\text{G7}} = -2.5 + 0.8 = -1.7 \text{ V} \]
\[ V_{IC\left(MIN\right)} = -2.5 + V_{DS\left(S\left(x1\right)\right)} + V_{GS1} \]

\[ \beta_0 = \frac{1.046}{2} \times 20 \times V_{S}^2 \Rightarrow V_{GON} = 0.142 \]

\[ I_S = \frac{0.386 \times 0.103 \times (V_{GSO} - 0.683)^2}{V_{DS1} = 0.707} \]

\[ V_{GSO} = -2.5 + 0.142 + 0.707 = -1.651 \]

\[ V_{IC\left(MAX\right)} = 2.5 - V_{GSO\left(S\left(x3\right)\right)} + V_{T,\text{N}} \]

\[ I_S = \frac{58.3}{2} \times 1 \times V_{ON}^2 \Rightarrow V_{ON} = 0.717 \]

\[ V_{IC\left(MAX\right)} = 2.5 - 0.717 + 0.682 \]

\[ = 1.445 \]

\[ ICMR = 1.445 + 1.651 = 4.096 \geq 3 \text{ (OK)} \]
(6) GB checking:

\[ GB = \frac{g_{m1}}{C_c} \]

\[ g_{m1} = \frac{V_{ds1}}{V_{gs1}} = 0.666 \, \text{mS} \]

\[ GB = \frac{0.666 \, \text{mS}}{3 \, \text{pF}} = 0.22 \times 10^8 \, \text{mS} = 22 \, \text{MHz} > 25 \, \text{MHz} \]

(7) Avd(w) checking:

\[ g_{m2} = g_{m6} = 0.666 \, \text{mS} \]

\[ R_I = Y_{ds1} || Y_{ds2} = 5.08 \times 10^3 \, \text{K}\Omega \]

\[ R_I = Y_{ds1} || Y_{ds2} = 5.08 \times 10^3 \, \text{K}\Omega \]

\[ R_D = Y_{ds6} || Y_{ds7} = 5.08 \times 10^3 \, \text{K}\Omega \]

\[ A_{vd} = g_{m2} R_D \leq 0.666 \times 5.08 \times 1.32 \leq 0.8 \]

\[ = 2.7 \times 10^4 \geq 2.7 \times 10^4 > 10^4 \]
(10) check phase margin:

\[ \phi = 180° - \tan^{-1} \left[ \frac{6B}{|P_{1}|} \right] - \tan^{-1} \left[ \frac{6B}{|P_{3}|} \right] \]

\[ = 180° - \tan^{-1} \left[ \frac{2.22 \times 10^8}{686.7} \right] - \tan^{-1} \left[ \frac{6B}{131} \right] \]

\[ = 180° - 89.9° - \tan^{-1} \left[ -\frac{6B}{131} \right] \]

\[ A_{BA} = 100 \times 10^{-6} \text{ m}^2, \quad A_{P_{3}} = 100 \times 10^{-6} \text{ m}^2 \quad \text{(ignore c四个方面)} \]

\[ C_{2} = C_{dK} + C_{gK} + C_{dA} + C_{gK} + C_{gK} \approx 0.482 \text{ pF} \]

\[ F_{P_{3}} = \frac{1}{2 \pi R_{K} C_{2}} = \frac{1}{2 \pi \times 3.28 \times 0.004 \times 0.482 \text{ pF}} = 100.6 \text{ MHz} \]

\[ \therefore \phi = 180° - 89.9° - \tan^{-1} \left[ \frac{31.3 \text{ MHz}}{100.6 \text{ MHz}} \right] \]

\[ = 70.76° \]
(2) pole & zero

\[ p_1 = -\frac{g_{m1}}{A/C_c} = -\frac{0.666 \times 10^{-2}}{3.32 \times 10^4 \times 3 \times 10^{12}} = -\frac{0.666 \times 10^{-5}}{3.32 \times 10^5} \text{ rps} \]

\[ p_1 = 668.61 \text{ rps} = 1.06 \text{ kHz} \]

\[ p_2 = -\frac{g_{m6}}{C_L} = -\frac{1.32 \times 10^{-3}}{10^{-11}} = -1.32 \times 10^8 \text{ rps} \]

Note \[ g_6B = 2.42 \times 10^8 \text{ rps} \] ie \[ |p_2| < g_6B \] Need zero-nulling to gain - phase margin

(3) zero-nulling

\[ \text{zero-pole & cancellation} \Rightarrow \text{zero} \Theta \frac{-1}{R_2C_c - C_c/g_{m6}} \]

\[ \frac{-1}{R_2C_c - C_c/g_{m6}} - \frac{g_{m6}}{C_L} \Rightarrow g_{m6}R_2C_c - C_c = C_L \]

\[ R_2 = \frac{C_L + C_c}{g_{m6}C_c} = \frac{1.32 \times 10^{12}}{3.32 \times 10^4 \times 3 \times 10^{12}} = 3.28 \text{ k\Omega} \]

\[ K_z = \frac{1}{K_p \Delta (V_o - V_{in})} \]

\[ V_{S(1kHz)} = 1.9 \]

\[ V_{S(0.8kHz, 0.65V)} = 1.63 \]

\[ V_{S(1kHz, 0.87V)} = 0.87 \]

\[ V_{S(0.8kHz, 0.65V)} \]

\[ 3.28 \times 10^{12} \times \frac{1}{3.28 \times 10^{-6} \times 0.8(3.32 \times 1.864)} \]

\[ S_8 = \frac{10^3}{1.83 \times 3 \times 78 \times 2.16} = 2 \Rightarrow \frac{W}{L} = 2 \]
All bulk for NMOS $\rightarrow -2.5\, V$

All bulk for PMOS $\rightarrow +2.5\, V$

M3, M4, M6, M7, M8 are tuned so that the input offset voltage is not needed. It does not affect the circuit performance as long as $V_i = 0, V_c = 0$.

A) (R1, R2) 3pF pads are biased at the correct operating points.
All bulk for NMOS $\rightarrow -2.5\, V$

All bulk for PMOS $\rightarrow +2.5\, V$