LECTURE 060 – PUSH-PULL OUTPUT STAGES

Objective
The objective of this presentation is:
1.) Provide sufficient output power in the form of voltage or current.
2.) Avoid signal distortion.
3.) Be efficient
4.) Provide protection from abnormal conditions (short circuit, over temperature, etc.)

Outline
• Push-Pull MOS (Class B)
• Push-Pull BJT (Class B)
• Summary

PUSH-PULL MOS OUTPUT STAGES (Class AB and B)

Push-Pull Source Follower
Can both sink and source current and provide a slightly lower output resistance.

Efficiency:
Depends on how the transistors are biased.
• Class B - one transistor has current flow for only 180° of the sinusoid (half period)

\[
\text{Efficiency} = \frac{P_{RL}}{P_{VDD}} = \frac{v_{OUT}(\text{peak})^2}{2R_L} \leq \frac{\pi}{2} \frac{v_{OUT}(\text{peak})}{\sqrt{V_{DD}^2 - V_{SS}^2}}
\]

Maximum efficiency occurs when \( v_{OUT}(\text{peak}) = V_{DD} \) and is 78.5%
• Class AB - each transistor has current flow for more than 180° of the sinusoid.
Maximum efficiency is between 25% and 78.5%
**Illustration of Class B and Class AB Push-Pull, Source Follower**

Output current and voltage characteristics of the push-pull, source follower ($R_L = 1\, \text{k}\Omega$):

![Graph of Class B and Class AB push-pull, source follower](image)

**Comments:**
- Note that $v_{OUT}$ cannot reach the extreme values of $V_{DD}$ and $V_{SS}$
- $I_{OUT}^+(\text{max})$ and $I_{OUT}^-(\text{max})$ is always less than $V_{DD}/R_L$ or $V_{SS}/R_L$
- For $v_{OUT} = 0\, \text{V}$, there is quiescent current flowing in M1 and M2 for Class AB
- Note that there is significant distortion at $v_{IN} = 0\, \text{V}$ for the Class B push-pull follower

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**Small-Signal Performance of the Push-Pull Follower**

**Model:**

![Small-Signal Model Diagram](image)

\[
\frac{v_{out}}{v_{in}} = \frac{g_{m1} + g_{m2}}{g_{ds1} + g_{ds2} + g_{m1} + g_{mbs1} + g_{m2} + g_{mbs2} + G_L}
\]

\[
R_{out} = \frac{1}{g_{ds1} + g_{ds2} + g_{m1} + g_{mbs1} + g_{m2} + g_{mbs2}} \quad \text{(does not include } R_L)\]

If $V_{DD} = -V_{SS} = 2.5\, \text{V}$, $V_{out} = 0\, \text{V}$, $I_{D1} = I_{D2} = 500\, \mu\text{A}$, and $W/L = 20\mu\text{m}/2\mu\text{m}$, $A_v = 0.787$ ($R_L = \infty$) and $R_{out} = 448\, \Omega$.

A zero and pole are located at

\[
z = \frac{-(g_{m1} + g_{m2})}{C_1}, \quad p = \frac{-(g_{ds1} + g_{ds2} + g_{m1} + g_{mbs1} + g_{m2} + g_{mbs2} + G_L)}{C_1 + C_2}.
\]

These roots will be high-frequency because the associated resistances are small.
**Push-Pull, Common Source Amplifiers**

Similar to the class A but can operate as class B providing higher efficiency.

![Fig. 060-04](image)

**Comments:**
- The batteries $V_{TR1}$ and $V_{TR2}$ are necessary to control the bias current in M1 and M2.
- The efficiency is the same as the push-pull, source follower.

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**Practical Implementation of the Push-Pull, Common Source Amplifier**

![Fig. 060-05](image)

$V_{GG3}$ and $V_{GG4}$ can be used to bias this amplifier in class AB or class B operation. Note, that the bias current in M6 and M8 is not dependent upon $V_{DD}$ or $V_{SS}$ (assuming $V_{GG3}$ and $V_{GG4}$ are not dependent on $V_{DD}$ and $V_{SS}$).
**Illustration of Class B and Class AB Push-Pull, Inverting Amplifier**

Output current and voltage characteristics of the push-pull, inverting amplifier ($R_L = 1\, \text{k}\Omega$):

![Graph of Class B and Class AB Push-Pull, Inverting Amplifier](image)

**Comments:**

- Note that there is significant distortion at $v_{IN} = 0\, \text{V}$ for the Class B inverter.
- Note that $v_{OUT}$ cannot reach the extreme values of $V_{DD}$ and $V_{SS}$.
- $I_{OUT}^\text{+}(\text{max})$ and $I_{OUT}^\text{−}(\text{max})$ is always less than $V_{DD}/R_L$ or $V_{SS}/R_L$.
- For $v_{OUT} = 0\, \text{V}$, there is quiescent current flowing in M1 and M2 for Class AB.

**Use of Negative, Shunt Feedback to Reduce the Output Resistance**

**Concept:**

![Diagram of Negative, Shunt Feedback](image)

$$R_{out} = \frac{r_{ds1}||r_{ds2}}{1+\text{Loop \text{Gain}}}$$.  

**Comments:**

- Can achieve output resistances as low as $10\, \Omega$.
- If the error amplifiers are not balanced, it is difficult to control the quiescent current in M1 and M2.
- Great linearity because of the strong feedback.
- Can be efficient if operated in class B or class AB.
Simple Implementation of Neg., Shunt Feedback to Reduce the Output Resistance

![Fig. 060-08](image)

Loop gain
\[
\text{Loop gain} \approx \left| \frac{R_1}{R_1+R_2} \left( \frac{g_{m1}+g_{m2}}{g_{ds1}+g_{ds2}+G_L} \right) \right|
\]

\[
R_{out} = \frac{r_{ds1}r_{ds2}}{1+\left( \frac{R_1}{R_1+R_2} \left( \frac{g_{m1}+g_{m2}}{g_{ds1}+g_{ds2}+G_L} \right) \right)}
\]

Let \( R_1 = R_2, R_L = \infty, I_{Bias} = 500\mu A, W_1/L_1 = 100\mu m/1\mu m \) and \( W_2/L_2 = 200\mu m/1\mu m \).

Thus, \( g_{m1} = 3.316\text{mS}, g_{m2} = 3.162\text{mS}, r_{ds1} = 50k\Omega \) and \( r_{ds2} = 40k\Omega \).

\[
R_{out} = \frac{50k\Omega \cdot 40k\Omega}{1+0.5(143.9)} = 22.22k\Omega \approx 304\Omega \quad (R_{out} = 5.42k\Omega \text{ if } R_L = 1k\Omega)
\]

What about the use of BJTs in CMOS Technology?

![Fig. 060-09](image)

Comments:
- Can use either substrate or lateral BJTs.
- Small-signal output resistance is \( 1/g_m \) which can easily be less than \( 100\Omega \).
- Unfortunately, only PNP or NPN BJTs are available but not both on a standard CMOS technology.
- In order for the BJT to sink (or source) large currents, the base current, \( i_B \), must be large. Providing large currents as the voltage gets to extreme values is difficult for MOSFET circuits to accomplish.
- If one considers the MOSFET driver, the emitter can only pull to within \( v_{BE}+V_{ON} \) of the power supply rails. This value can be \( 1V \) or more.
PUSH-PULL BJT OUTPUT STAGES (Class AB and B)

Simple Class B Output Stage

Class B operation: Two active devices are used to deliver the power instead of one. Each device conducts for alternate half cycles.
Efficiency can approach 78.5%
Can suffer from crossover distortion - the transition from one device to the other.

Class AB Output Stage

$I_Q$ sets up the bias current in Q1 and Q2 when there is no input signal.
Each transistor is biased so that there is a region in the middle where both are on (Class AB)
**Power Considerations in the Class B Output Stage**

Voltage and current waveforms for a Class B amplifier:

![Class B Amplifier Diagram](image)

Efficiency Considerations of the Class-B Push-Pull Output Stage

Load line for one device in a class-B stage:

![Load Line Diagram](image)

Efficiency:

\[ P_L = \frac{1}{2} \frac{[V_{out}(\text{peak})]^2}{R_L} \]

and \( P_{\text{supply}} = 2V_{CC}I_{\text{supply}} = 2V_{CC} \left( \frac{1}{T} \int_0^T i_C(t) \, dt \right) = 2V_{CC} \left( \frac{I_C(\text{peak})}{\pi} \right) = \frac{2}{\pi} \frac{V_{CC}}{R_L} V_{out}(\text{peak}) \)

\[ \therefore \eta = \frac{P_L}{P_{\text{supply}}} = \frac{\pi}{4} \frac{V_{out}(\text{peak})}{V_{CC}} \Rightarrow \eta_{\max} = \frac{\pi}{4} = 78.6\% \]

Max. efficiency for the above class-B push-pull output stage is \( \eta_{\max} = \frac{\pi}{4} \frac{V_{CC} - V_{CE(\text{sat})}}{V_{CC}} \)
709 Output Stage

This stage assumes that feedback will be used around the amplifier which will linearize the nonlinearity of the output stage.

709 Output Stage Voltage Transfer Function

```
709 Output Stage Voltage Transfer Function
.MODEL BJTN NPN IS=1E-14 BF=100 VAF=50
.MODEL BJTP PNP IS=1E-14 BF=50 VAF=50
Q1 4 3 2 BJTN
Q2 5 3 2 BJTP
Q3 3 1 5 BJTN
VCC 4 0 DC 10V
VEE 5 0 DC -10V
VIN 1 5
RL 2 0 1KILOHM
R1 4 3 20KILOHM
.DC VIN 0.60 0.67 0.001
.PRINT DC V(2)
.PROBE
.END
```

741 Output Stage

```
741 Output Stage Voltage Transfer Function - RL = 1Kiloohm
.MODEL BJTN NPN IS=1E-14 BF=100 VAF=50
.MODEL BJTP PNP IS=1E-14 BF=50 VAF=50
Q23 8 1 3 BJTP
Q20 8 3 2 BJTP
Q14 7 5 2 BJTN
Q17 1 9 8 BJTN
Q18 5 4 3 BJTN
Q19 5 5 4 BJTN
Q13A 5 6 7 BJTP
Q13B 1 6 7 BJTP 3.0
Q13C 6 6 7 BJTP
VCC 7 0 DC 15V
VEE 8 0 DC -15V
IBIAS 6 0 220UA
VIN 9 8 DC 0.645
R10 4 3 40KILOHM
RL 2 0 1KILOHM
.DC VIN 0.625 0.665 0.0005
.PRINT DC V(2)
.PROBE
.END
```
**Quasi-Complementary Output Stages**

Quasi-complementary connections are used to improve the performance of the PNP or PMOS transistor.

Composite connections:

![Composite Connections Diagram](image)

**PNP Equivalent:**

\[ I_C = (1 + \beta_2) I_{C1} = (1 + \beta_2) I_s \exp \left( \frac{V_{EB}}{V_T} \right) \]

**PMOS Equivalent:**

\[ I_D = (1 + \beta_2) I_{D1} = (1 + \beta_2) \left( \frac{K_P' W_1}{2L_1} \right) (V_{GS} - V_T)^2 \]

\[ \beta \quad \text{NPN} \]

\[ \beta' \quad \text{enhanced K'} \]

**Overload Protection**

For circuits that can provide large amounts of output current, it is necessary to provide short-circuit current protection.

**Example:**

![Overload Protection Diagram](image)

\[ i_{OUT} = i_{C1} + i_{C2} = i_{C1} \quad \therefore \quad i_{OUT} = \beta_1 i_{B1} = \beta_1(i_i - i_{C2}) \]

But \[ i_{C2} \approx I_s \exp \left( \frac{V_{BE2}}{V_T} \right) \approx I_s \exp \left( \frac{V_{EL}}{V_T} \right) \]

\[ \therefore \quad i_{OUT} = \beta_1 i_i - I_s \exp \left( \frac{V_{EL}}{V_T} \right) \]

As \( i_{OUT} \) increases, Q2 turns on and pulls base current away from Q1 limiting the output current.
SUMMARY

Requirements of Output Stages

• The objectives are to provide output power in form of voltage and/or current.
• In addition, the output amplifier should be linear and be efficient.
• Low output resistance is required to provide power efficiently to a small load resistance.
• High source/sink currents are required to provide sufficient output voltage rate due to large load capacitances.
• Types of output stages considered:
  - Class B or AB stage with push-pull (maximum efficiency was 78.6%)
  - Quasi-complementary devices help improve the performance of the p-type devices
  - Protection circuits prevent large currents from flowing in the output devices
• For large load capacitors all that is required from an output stage is large current, the output resistance does not have to be small