LECTURE 190 – CASCODE OP AMPS I
(READING: GHLM – 443-453, AH – 293-309)

Objective

The objective of this presentation is:

1.) Develop cascode op amp architectures

2.) Show how to design with the cascode op amps

Outline

- Op amps with cascoding in the first stage
- Op amps with cascoding in the second stage
- Folded cascode op amp
- Summary

Why Cascode Op Amps?

- Control of the frequency behavior
- Can get more gain by increasing the output resistance of a stage
- In the past section, *PSRR* of the two-stage op amp was insufficient for many applications
- A two-stage op amp can become unstable for large load capacitors (if nulling resistor is not used)
- We will see in future sections that the cascode op amp leads to wider *ICMR* and/or smaller power supply requirements

Where Should the Cascode Technique be Used?

- First stage -
  - Good noise performance
  - Requires level translation to second stage
  - Degrades the Miller compensation
- Second stage -
  - Self compensating
  - Increases the efficiency of the Miller compensation
  - Increases *PSRR*

Use of Cascoding in the First Stage of the Two-Stage Op Amp

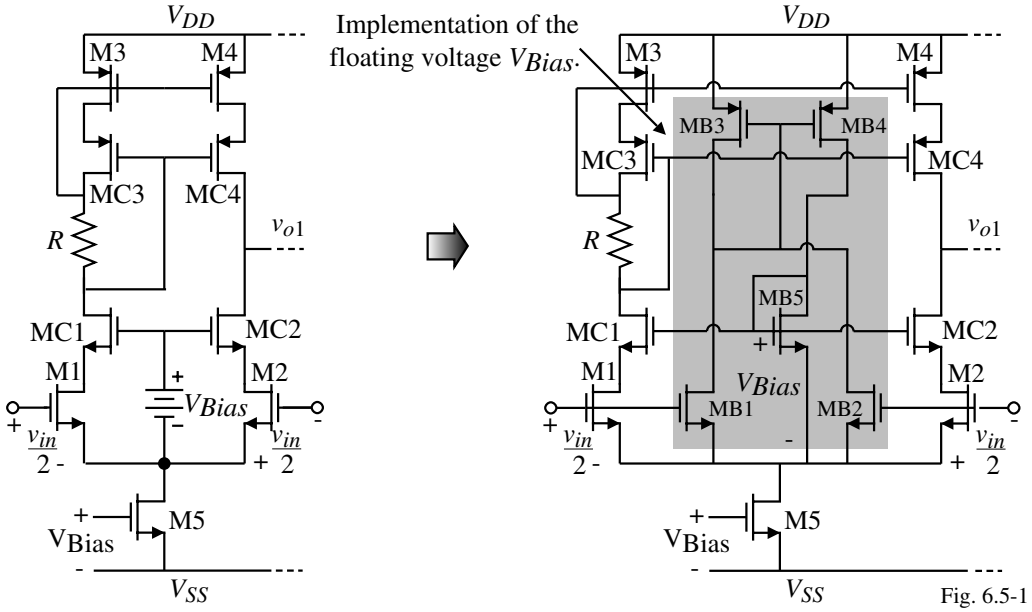


Fig. 6.5-1

R_{out} of the first stage is $R_I \approx (g_{mC2}r_{dsC2}r_{ds2})\|(g_{mC4}r_{dsC4}r_{ds4})$

Voltage gain $= \dfrac{v_{o1}}{v_{in}} = g_{m1}R_I$ [The gain is increased by approximately $0.5(g_{MC}r_{dsC})$]

As a single stage op amp, the compensation capacitor becomes the load capacitor.

Example 1 Single-Stage, Cascode Op Amp Performance

Assume that all W/L ratios are 10 μm/1 μm, and that $I_{DS1} = I_{DS2} =$ 50 μA of single stage op amp. Find the voltage gain of this op amp and the value of C_I if GB = 10 MHz. Use the model parameters of Table 3.1-2.

Solution

The device transconductances are

$g_{m1} = g_{m2} = g_{mI} = 331.7\ \mu S$

$g_{mC2} = 331.7 \mu S$

$g_{mC4} = 223.6\ \mu S.$

The output resistance of the NMOS and PMOS devices is 0.5 MΩ and 0.4 MΩ, respectively.

$\therefore$ $R_I = 25$ MΩ

$A_v(0) = 8290$ V/V.

For a unity-gain bandwidth of 10 MHz, the value of C_I is 5.28 pF.

What happens if a 100pF capacitor is attached to this op amp?

GB goes from 10MHz to 0.53MHz.

Two-Stage Op Amp with a Cascoded First-Stage

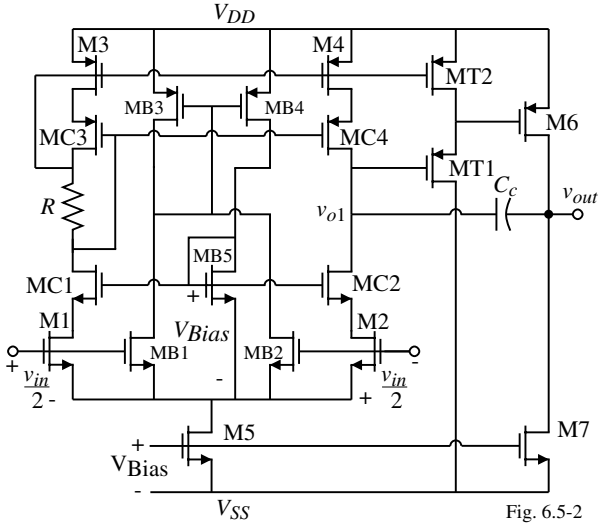


Fig. 6.5-2

- MT1 and MT2 are required for level shifting from the first-stage to the second.
- The $PSRR^+$ is improved by the presence of MT1
- Internal loop pole at the gate of M6 may cause the Miller compensation to fail.
- The voltage gain of this op amp could easily be 100,000V/V

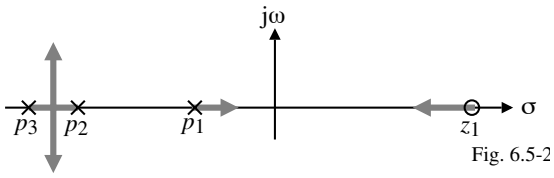


Fig. 6.5-2

Two-Stage Op Amp with a Cascode Second-Stage

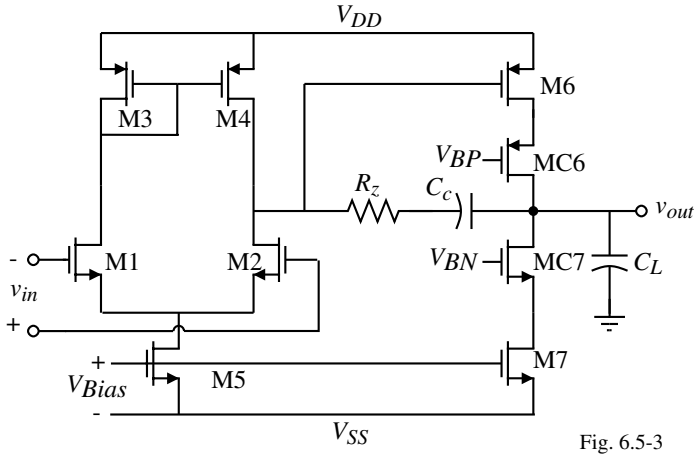


Fig. 6.5-3

$$A_v = g_{mI}g_{mII}R_IR_{II} \quad \text{where} \quad g_{mI} = g_{m1} = g_{m2}, \quad g_{mII} = g_{m6},$$

$$R_I = \frac{1}{g_{ds2} + g_{ds4}} = \frac{2}{(\lambda_2 + \lambda_4)I_{D5}} \quad \text{and} \quad R_{II} = (g_{mC6}r_{dsC6}r_{ds6})\|(g_{mC7}r_{dsC7}r_{ds7})$$

Comments:

- The second-stage gain has greatly increased improving the Miller compensation
- The overall gain is approximately $(g_m r_{ds})^3$ or very large
- Output pole, p_2, is approximately the same if C_c is constant
- The RHP is the same if C_c is constant

A Balanced, Two-Stage Op Amp using a Cascode Output Stage

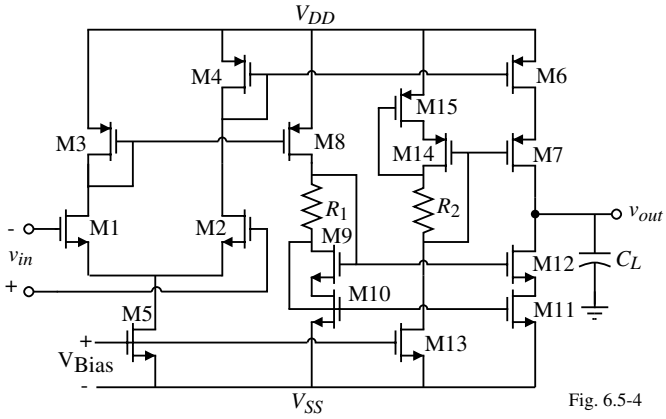


Fig. 6.5-4

$$v_{out} = \left(\frac{g_{m1}g_{m8}}{g_{m3}}\frac{v_{in}}{2} + \frac{g_{m2}g_{m6}}{g_{m4}}\frac{v_{in}}{2}\right) R_{II}$$

$$= \left(\frac{g_{m1}}{2} + \frac{g_{m2}}{2}\right) k v_{in}\, R_{II} = g_{m1} \cdot k \cdot R_{II}\, v_{in}$$

where

$$R_{II} = (g_{m7}r_{ds7}r_{ds6}) \| (g_{m12}r_{ds12}r_{ds11})$$

and

$$k = \frac{g_{m8}}{g_{m3}} = \frac{g_{m6}}{g_{m4}}$$

Note that this op amp is balanced because the drain-to-ground loads for M1 and M2 are identical.

TABLE 1 - Pertinent Design Relationships for Balanced, Cascode Output Stage Op Amp.

Slew rate $= \frac{I_{out}}{C_L}$	$GB = \frac{g_{m1}g_{m8}}{g_{m3}C_L}$	$A_v = \frac{1}{2}\left(\frac{g_{m1}g_{m8}}{g_{m3}} + \frac{g_{m2}g_{m6}}{g_{m4}}\right) R_{II}$
$V_{in}(\max) = V_{DD} - \left[\frac{I_5}{\beta_3}\right]^{1/2} - \lvert V_{TO3}\rvert(\max) + V_{T1}(\min)$		$V_{in}(\min) = V_{SS} + V_{DS5} + \left[\frac{I_5}{\beta_1}\right]^{1/2} + V_{T1}(\min)$

Example 2 - Design of Balanced, Cascoded Output Stage Op Amp

The balanced, cascoded output stage op amp is a useful alternative to the two-stage op amp. Its design will be illustrated by this example. The pertinent design equations for the op amp were given above. The specifications of the design are as follows:

$V_{DD} = -V_{SS} = 2.5$ V	Slew rate = 5 V/μs with a 50 pF load
GB = 10 MHz with a 10 pF load	$A_v \geq 5000$
Input CMR = −1V to +1.5 V	Output swing = ±1.5 V

Use the parameters of Table 3.1-2 and let all device lengths be 1 μm.

Solution

While numerous approaches can be taken, we shall follow one based on the above specifications. The steps will be numbered to help illustrate the procedure.

1.) The first step will be to find the maximum source/sink current. This is found from the slew rate.

$$I_{source}/I_{sink} = C_L \times \text{slew rate} = 50\text{ pF}(5\text{ V}/\mu\text{s}) = 250\ \mu\text{A}$$

2.) Next some W/L constraints based on the maximum output source/sink current are developed. Under dynamic conditions, all of I_5 will flow in M4; thus we can write

$$\text{Max. } I_{out}(\text{source}) = (S_6/S_4)I_5 \quad \text{and} \quad \text{Max. } I_{out}(\text{sink}) = (S_8/S_3)I_5$$

The maximum output sinking current is equal to the maximum output sourcing current if

$$S_3 = S_4, \quad S_6 = S_8, \text{ and } S_{10} = S_{11}$$

Example 2 - Continued

3.) Choose I_5 as 100 μA. This current (which can be changed later) gives

$$S_6 = 2.5S_4 \text{ and } S_8 = 2.5S_3$$

Note that S_8 could equal S_3 if $S_{11} = 2.5S_{10}$. This would minimize the power dissipation.

4.) Next design for ±1.5 V output capability. We shall assume that the output must source or sink the 250μA at the peak values of output. First consider the negative output peak. Since there is 1 V difference between V_{SS} and the minimum output, let $V_{DS11}(\text{sat}) = V_{DS12}(\text{sat}) = 0.5$ V (we continue to ignore the bulk effects). Under the maximum negative peak assume that $I_{11} = I_{12} = 250$ μA. Therefore

$$0.5 = \sqrt{\frac{2I_{11}}{K'_N S_{11}}} = \sqrt{\frac{2I_{12}}{K'_N S_{12}}} = \sqrt{\frac{500\ \mu\text{A}}{(110\ \mu\text{A/V}^2)S_{11}}}$$

which gives $S_{11} = S_{12} = 18.2$ and $S_9 = S_{10} = 18.2$. For the positive peak, we get

$$0.5 = \sqrt{\frac{2I_6}{K'_P S_6}} = \sqrt{\frac{2I_7}{K'_P S_7}} = \sqrt{\frac{500\ \mu\text{A}}{(50\ \mu\text{A/V}^2)S_6}}$$

which gives $S_6 = S_7 = S_8 = 40$ and $S_3 = S_4 = (40/2.5) = 16$.

5.) Next the values of R_1 and R_2 are designed. For the resistor of the self-biased cascode we can write $R_1 = V_{DS12}(\text{sat})/250\mu\text{A} = 2\text{k}\Omega$ and $R_2 = V_{SD7}(\text{sat})/250\mu\text{A} = 2\text{k}\Omega$

Example 2 - Continued

Using this value of R_1 (R_2) will cause M11 to slightly be in the active region under quiescent conditions. One could redesign R_1 to avoid this but the minimum output voltage under maximum sinking current would not be realized.

6.) Now we must consider the possibility of conflict among the specifications.

First consider the input CMR. S_3 has already been designed as 16. Using ICMR relationship, we find that S_3 should be at least 4.1. A larger value of S_3 will give a higher value of $V_{in}(\text{max})$ so that we continue to use $S_3 = 16$ which gives $V_{in}(\text{max}) = 1.95$V.

Next, check to see if the larger W/L causes a pole below the gainbandwidth. Assuming a C_{ox} of 0.4fF/μm^2 gives the first-stage pole of

$$p_3 = \frac{-g_{m3}}{C_{gs3}+C_{gs8}} = \frac{-\sqrt{2K'_P S_3 I_3}}{(0.667)(W_3L_3+W_8L_8)C_{ox}} = 33.15\text{x}10^9 \text{ rads/sec or } 5.275\text{GHz}$$

which is much greater than 10GB.

7.) Next we find g_{m1} (g_{m2}). There are two ways of calculating g_{m1}.

(a.) The first is from the A_v specification. The gain is

$$A_v = (g_{m1}/2g_{m4})(g_{m6} + g_{m8})\, R_{II}$$

Note, a current gain of k could be introduced by making S_6/S_4 ($S_8/S_3 = S_{11}/S_3$) equal to k.

$$\frac{g_{m6}}{g_{m4}} = \frac{g_{m11}}{g_{m3}} = \sqrt{\frac{2K_P'\cdot S_6\cdot I_6}{2K_P'\cdot S_4\cdot I_4}} = k$$

Example 2 - Continued

Calculating the various transconductances we get g_{m4} = 282.4 μS, $g_{m6} = g_{m7} = g_{m8}$ = 707 μS, $g_{m11} = g_{m12}$ = 707 μS, $r_{ds6} = r_{d7}$ = 0.16 MΩ, and $r_{ds11} = r_{ds12}$ = 0.2 MΩ. Assuming that the gain A_v must be greater than 5000 and k = 2.5 gives g_{m1} > 72.43 μS.

(b.) The second method of finding g_{m1} is from the *GB* specifications. Multiplying the gain by the dominant pole ($1/C_{II}R_{II}$) gives

$$GB = \frac{g_{m1}(g_{m6} + g_{m8})}{2g_{m4}C_L}$$

Assuming that C_L= 10 pF and using the specified *GB* gives g_{m1} = 251 μS.

Since this is greater than 72.43μS, we choose $g_{m1} = g_{m2}$ = 251μS. Knowing I_5 gives $S_1 = S_2$ = 11.45 ≈ 12.

8.) The next step is to check that S_1 and S_2 are large enough to meet the −1V input CMR specification. Use the saturation formula we find that V_{DS5} is 0.5248 V. This gives S_5 = 6.6 ≈ 7. The gain becomes A_v = 6,925V/V and *GB* = 10 MHz for a 10 pF load. We shall assume that exceeding the specifications in this area is not detrimental to the performance of the op amp.

9.) With S_5 = 7 then we can design S_{13} from the relationship

$$S_{13} = \frac{I_{13}}{I_5} S_5 = \frac{125\mu A}{100\mu A} 7 = 8.75$$

Example 2 - Continued

10.) Finally we need to design the value of V_{Bias}, which can be done with the values of S_5 and I_5 known. However, M5 is usually biased from a current source flowing into a MOS diode in parallel with the gate-source of M5. The value of the current source compared with I_5 would define the W/L ratio of the MOS diode.

Table 2 summarizes the values of *W*/*L* that resulted from this design procedure. The power dissipation for this design is seen to be 2 mW. The next step would be begin simulation.

Table 2 - Summary of W/L Ratios for Example 2

$S_1 = S_2 = 12$
$S_3 = S_4 = 16$
$S_5 = 7$
$S_6 = S_7 = S_8 = S_{14} = S_{15} = 40$
$S_9 = S_{10} = S_{11} = S_{12} = 18.2$
$S_{13} = 8.75$

Technological Implications of the Cascode Configuration

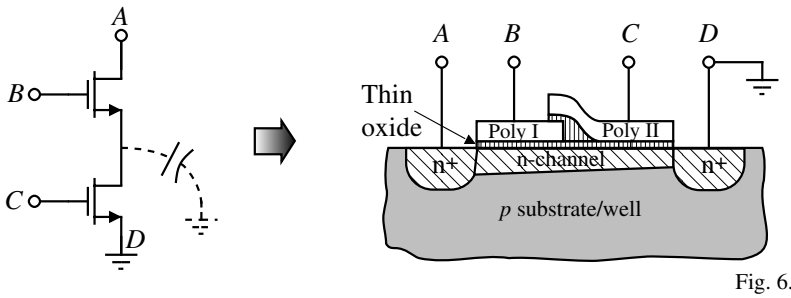


Fig. 6.5-5

If a double poly CMOS process is available, internode parasitics can be minimized.

As an alternative, one should keep the drain/source between the transistors to a minimum area.

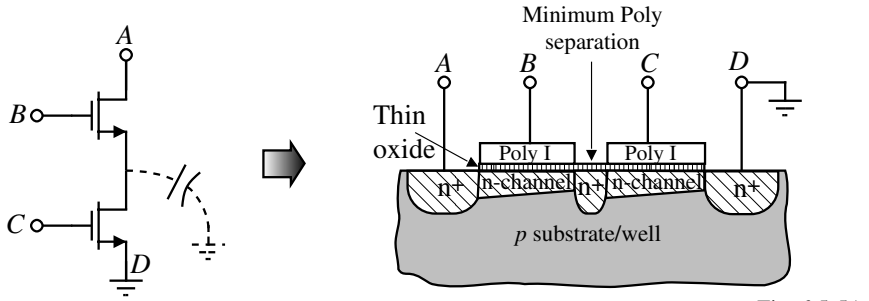
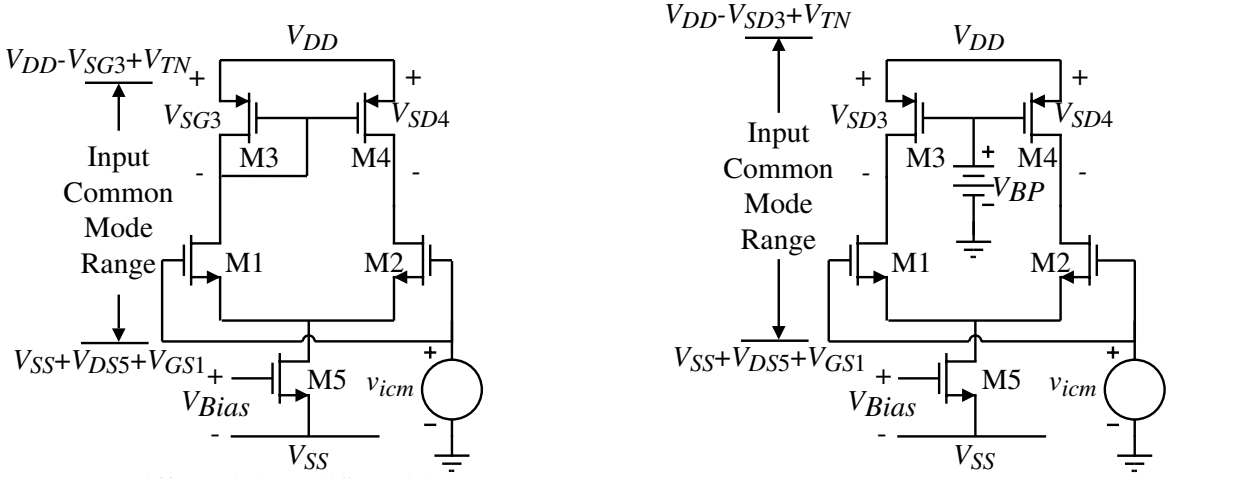


Fig. 6.5-5A

Input Common Mode Range for Two Types of Differential Amplifier Loads



Differential amplifier with a current mirror load.

Differential amplifier with current source loads.

Fig. 6.5-6

In order to improve the ICMR, it is desirable to use current source (sink) loads without losing half the gain.

The resulting solution is the *folded* cascode op amp.

The Folded Cascode Op Amp

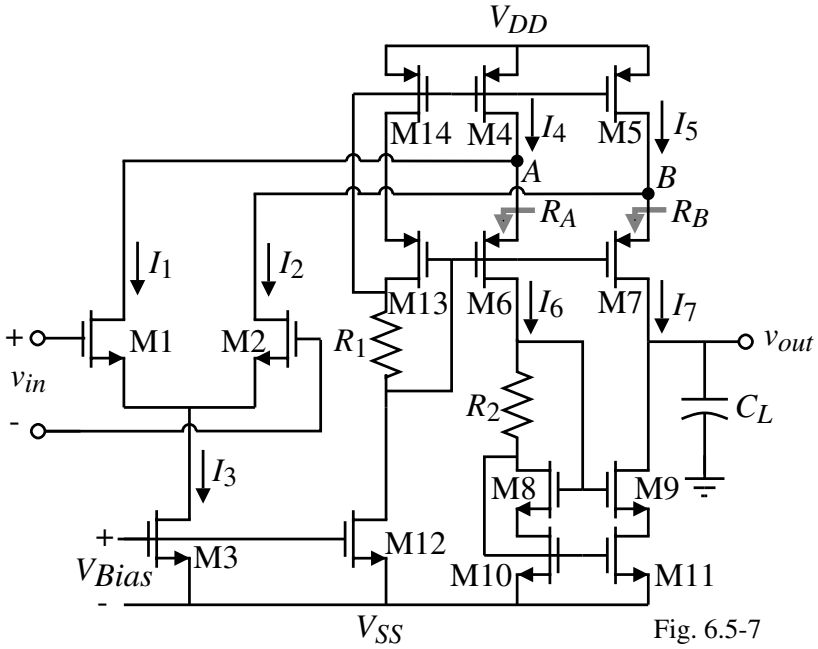


Fig. 6.5-7

We have examined the small signal performance and the frequency response in an earlier lecture.

PSRR of the Folded Cascode Op Amp

Consider the following circuit used to model the $PSRR^-$:

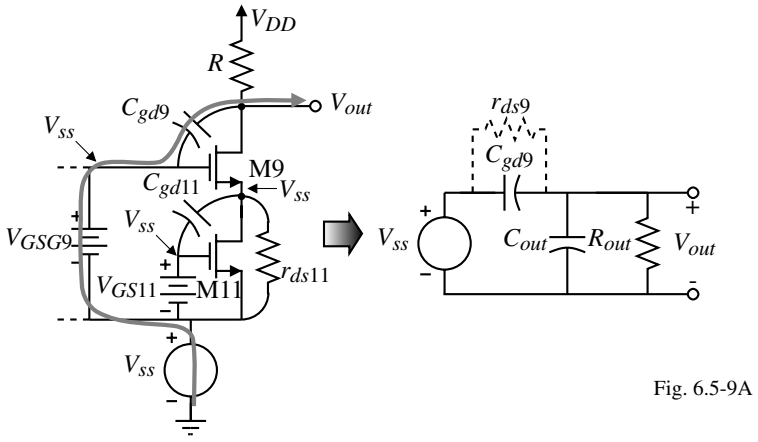


Fig. 6.5-9A

This model assumes that gate, source and drain of M11 and the gate and source of M9 all vary with V_{SS}.

We shall examine V_{out}/V_{ss} rather than $PSRR^-$. (Small V_{out}/V_{ss} will lead to large $PSRR^-$.)

The transfer function of V_{out}/V_{ss} can be found as

$$\frac{V_{out}}{V_{ss}} \approx \frac{sC_{gd9}R_{out}}{sC_{out}R_{out}+1} \quad \text{for } C_{gd9} < C_{out}$$

The approximate $PSRR^-$ is sketched on the next page.

Frequency Response of the PSRR- of the Folded Cascode Op Amp

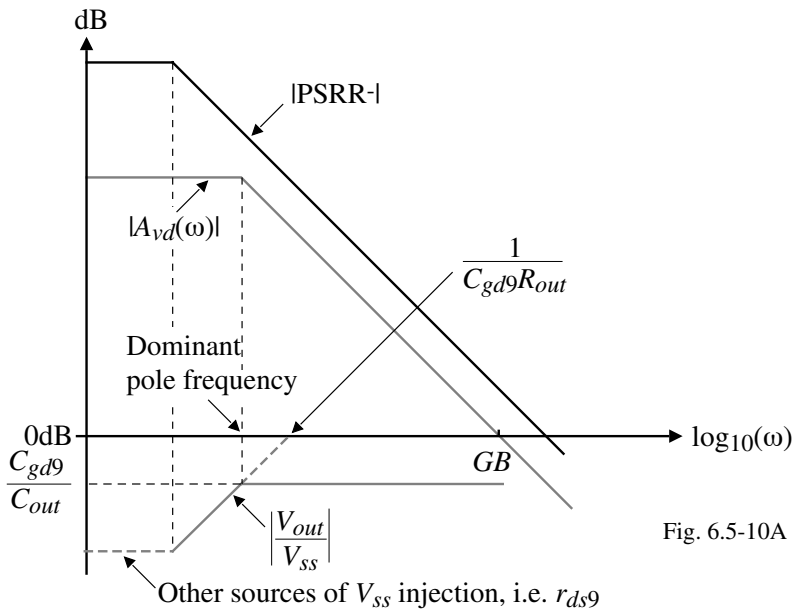


Fig. 6.5-10A

We see that the PSRR of the cascode op amp is much better than the two-stage op amp.

Design Approach for the Folded-Cascode Op Amp

Step	Relationship/ Requirement	Design Equation/Constraint	Comments
1	Slew Rate	$I_3 = SR \cdot C_L$	
2	Bias currents in output cascodes	$I_4 = I_5 = 1.2I_3$ to $1.5I_3$	Avoid zero current in cascodes
3	Maximum output voltage, v_{out}(max)	$S_5=\frac{2I_5}{K_P' V_{SD5}^2}$, $S_7=\frac{2I_7}{K_P' V_{SD7}^2}$ Let $S_4=S_{14}=S_5$ & $S_{13}=S_6=S_7$	$V_{SD5}(\text{sat}) = V_{SD7}(\text{sat}) = 0.5[V_{DD}-V_{out}(\text{min})]$
4	Minimum output voltage, v_{out}(min)	$S_{11}=\frac{2I_{11}}{K_N' V_{DS11}^2}$, $S_9 = \frac{2I_9}{K_N' V_{DS9}^2}$ Let $S_{10}=S_{11}$ & $S_8=S_9$	$V_{DS9}(\text{sat}) = V_{DS11}(\text{sat}) = 0.5(V_{out}(\text{min})-\lvert V_{SS}\rvert)$
5	Self-bias cascode	$R_1 = V_{SD14}(\text{sat})/I_{14}$ and $R_2 = V_{DS8}(\text{sat})/I_6$	
6	$GB = \frac{g_{m1}}{C_L}$	$S_1=S_2=\frac{g_{m1}^2}{K_N' I_3}=\frac{GB^2 C_L^2}{K_N' I_3}$	
7	Minimum input CM	$S_3 = \frac{2I_3}{K_N'\left(V_{in}(\text{min})-V_{SS}-\sqrt{\frac{I_3}{K_N' S_1}}-V_{T1}\right)^2}$	
8	Maximum input CM	$S_4 = S_5 = \frac{2I_4}{K_P'(V_{DD}-V_{in}(\text{max})+V_{T1})}$	S_4 and S_5 must meet or exceed the value in step 3
9	Differential Voltage Gain	$\frac{v_{out}}{v_{in}} = \left(\frac{g_{m1}}{2}+\frac{g_{m2}}{2(1+k)}\right)R_{out} = \left(\frac{2+k}{2+2k}\right) g_{mI} R_{out}$	
10	Power dissipation	$P_{diss} = (V_{DD}-V_{SS})(I_3+I_{12}+I_{10}+I_{11})$	

Example 3 - Design of a Folded-Cascode Op Amp

Follow the procedure given to design the folded-cascode op amp when the slew rate is 10V/μs, the load capacitor is 10pF, the maximum and minimum output voltages are ±2V for ±2.5V power supplies, the *GB* is 10MHz, the minimum input common mode voltage is -1.5V and the maximum input common mode voltage is 2.5V. The differential voltage gain should be greater than 5,000V/V and the power dissipation should be less than 5mW. Use channel lengths of 1μm.

Solution

Following the approach outlined above we obtain the following results.

$$I_3 = SR \cdot C_L = 10\text{x}10^6 \cdot 10^{-11} = 100\mu\text{A}$$

Select $I_4 = I_5 = 125\mu\text{A}$.

Next, we see that the value of $0.5(V_{DD}\text{-}V_{out}(\text{max}))$ is 0.5V/2 or 0.25V. Thus,

$$S_4 = S_5 = S_{14} = \frac{2 \cdot 125\mu\text{A}}{50\mu\text{A/V}^2 \cdot (0.25\text{V})^2} = \frac{2 \cdot 125 \cdot 16}{50} = 80$$

and assuming worst case currents in M6 and M7 gives,

$$S_6 = S_7 = S_{13} = \frac{2 \cdot 125\mu\text{A}}{50\mu\text{A/V}^2 (0.25\text{V})^2} = \frac{2 \cdot 125 \cdot 16}{50} = 80$$

The value of $0.5(V_{out}(\text{min})\text{-}|V_{SS}|)$ is also 0.25V which gives the value of S_8, S_9, S_{10} and S_{11} as $S_8 = S_9 = S_{10} = S_{11} = \frac{2 \cdot I_8}{K_N' V_{DS8}^2} = \frac{2 \cdot 125}{110 \cdot (0.25)^2} = 36.36$

Example 3 - Continued

The value of R_1 and R_2 is equal to 0.25V/125μA or 2kΩ. In step 6, the value of *GB* gives S_1 and S_2 as

$$S_1 = S_2 = \frac{GB^2 \cdot C_L^2}{K_N' I_3} = \frac{(20\pi\text{x}10^6)^2 (10^{-11})^2}{110\text{x}10^{-6} \cdot 100\text{x}10^{-6}} = 35.9$$

The minimum input common mode voltage defines S_3 as

$$S_3 = \frac{2I_3}{K_N'\left(V_{in}(\text{min})\text{-}V_{SS}\text{-}\sqrt{\frac{I_3}{K_N' S_1}} - V_{T1}\right)^2} = \frac{200\text{x}10^{-6}}{110\text{x}10^{-6}\left(-1.5+2.5-\sqrt{\frac{100}{110 \cdot 35.9}} -0.75\right)^2} = 20$$

We need to check that the values of S_4 and S_5 are large enough to satisfy the maximum input common mode voltage. The maximum input common mode voltage of 2.5 requires

$$S_4 = S_5 \geq \frac{2I_4}{K_P'[V_{DD}\text{-}V_{in}(\text{max})+V_{T1}]} = \frac{2 \cdot 125\mu\text{A}}{50\text{x}10^{-6}\mu\text{A/V}^2[0.7\text{V}]^2} = 10.2$$

which is much less than 80. In fact, with $S_4 = S_5 = 80$, the maximum input common mode voltage is 3V. Finally, S_{12}, is given as

$$S_{12} = \frac{125}{100} S_3 = 25$$

The power dissipation is found to be

$$P_{diss} = 5\text{V}(125\mu\text{A}+125\mu\text{A}+125\mu\text{A}) = 1.875\text{mW}$$

Example 3 - Continued

The small-signal voltage gain requires the following values to evaluate:

S_4, S_5, S_{13}, S_{14}: $g_m = \sqrt{2 \cdot 125 \cdot 50 \cdot 80} = 1000\mu S$ and $g_{ds} = 125 \times 10^{-6} \cdot 0.05 = 6.25\mu S$

S_6, S_7: $g_m = \sqrt{2 \cdot 75 \cdot 50 \cdot 80} = 774.6\mu S$ and $g_{ds} = 75 \times 10^{-6} \cdot 0.05 = 3.75\mu S$

S_8, S_9, S_{10}, S_{11}: $g_m = \sqrt{2 \cdot 75 \cdot 110 \cdot 36.36} = 774.6\mu S$ and $g_{ds} = 75 \times 10^{-6} \cdot 0.04 = 3\mu S$

S_1, S_2: $g_{mI} = \sqrt{2 \cdot 50 \cdot 110 \cdot 35.9} = 628\mu S$ and $g_{ds} = 50 \times 10^{-6}(0.04) = 2\mu S$

Thus,

$$R_{II} \approx g_{m9} r_{ds9} r_{ds11} = (774.6\mu S)\left(\frac{1}{3\mu S}\right)\left(\frac{1}{3\mu S}\right) = 86.07M\Omega$$

$$R_{out} \approx 86.07M\Omega \| (774.6\mu S)\left(\frac{1}{3.75\mu S}\right)\left(\frac{1}{2\mu S + 6.25\mu S}\right) = 19.40M\Omega$$

$$k = \frac{R_{II}(g_{ds2} + g_{ds4})}{g_{m7} r_{ds7}} = \frac{86.07M\Omega(2\mu S + 6.25\mu S)(3.75\mu S)}{774.6\mu S} = 3.4375$$

The small-signal, differential-input, voltage gain is

$$A_{vd} = \left(\frac{2+k}{2+2k}\right) g_{mI} R_{out} = \left(\frac{2+3.4375}{2+6.875}\right) 0.628 \times 10^{-3} \cdot 19.40 \times 10^{6} = 7{,}464 \text{ V/V}$$

The gain is larger than required by the specifications which should be okay.

Comments on Folded Cascode Op Amps

- Good PSRR
- Good ICMR
- Self compensated
- Can cascade an output stage to get extremely high gain with lower output resistance (use Miller compensation in this case)
- Need first stage gain for good noise performance
- Widely used in telecommunication circuits where large dynamic range is required

SUMMARY

- Cascode op amps offer an alternate architecture to the two-stage op amp
- The cascode op amp is typically self-compensating
- The cascode op amp generally has better PSRR