LECTURE 210 – DC ANALYSIS OF THE 741 OP AMP
(READING: GHLM – 454-462)

Objective

The objective of this presentation is to:

1.) Identify the devices, circuits, and stages in the 741 operational amplifier

2.) Perform a dc bias analysis

3.) Compare hand calculations of dc analyses with PSpice simulations

Outline

- 741 circuit topology and analysis
- PSpice analysis techniques and results
- Summary

741 OPERATIONAL AMPLIFIER

Circuit

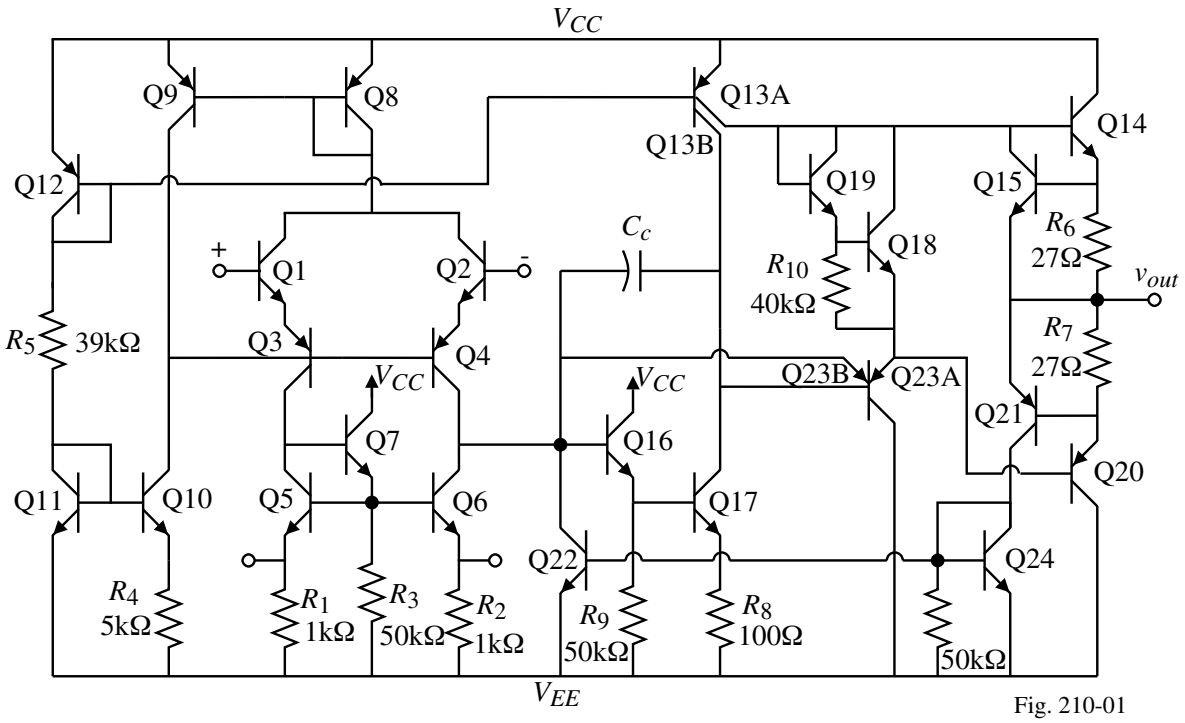


Fig. 210-01

The 741 op amp is typical of a widely used stand-alone operational amplifiers.

Simplified, Conceptual Schematic Diagram of the 741 Op Amp

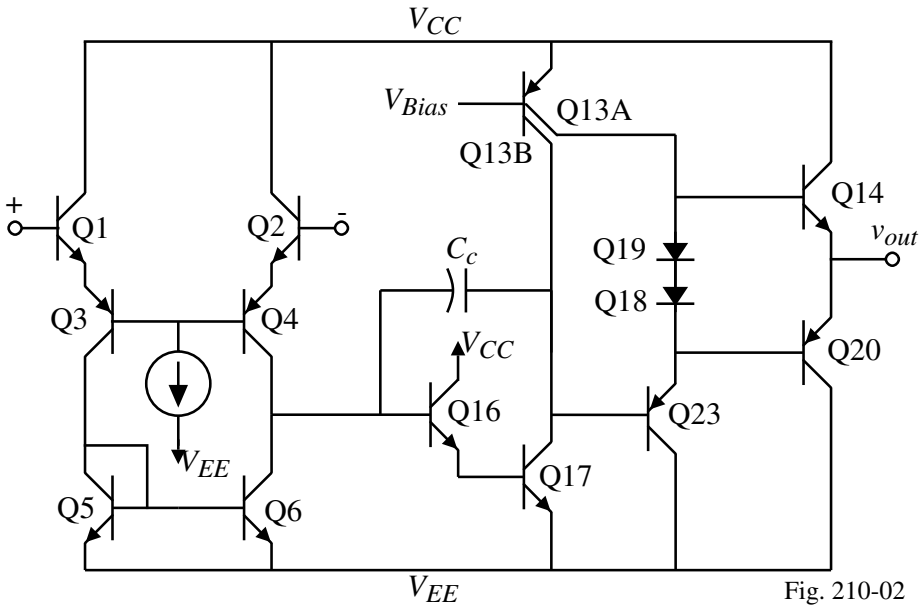
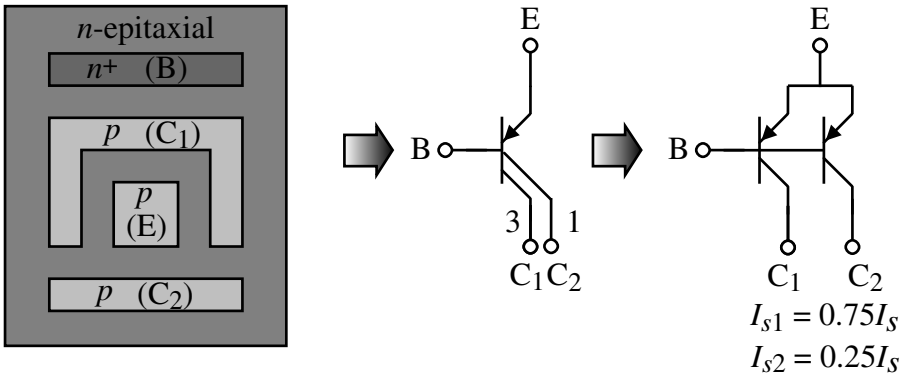


Fig. 210-02

Multicollector Lateral PNP



$I_{s1} = 0.75I_S$

$I_{s2} = 0.25I_S$

I_S is the saturation current of the structure with both collectors connected together.

Fig. 210-03

DC Analysis of the 741 Op Amp

Bias circuitry:

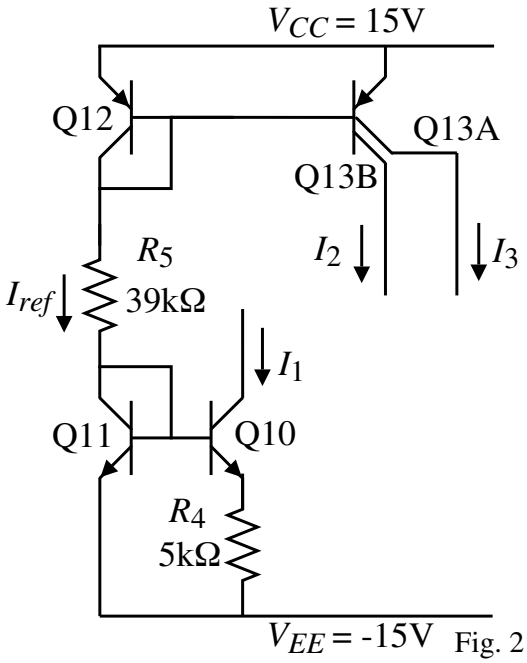


Fig. 210-04

$$I_{ref} = \frac{V_{CC}\text{-}V_{EE}\text{-}2V_{BE}}{R_5} = 733\mu A$$

$$I_2 = I_{13B} = 0.75 I_{ref} = 550\mu A$$

$$I_3 = I_{13A} = 0.25 I_{ref} = 180\mu A$$

$$I_1 = I_{10} = \frac{V_t}{R_4}\left[ln(I_{ref}) - ln(I_1)\right] = 19\mu A$$

Simplified Schematic of the 741 Op Amp with Idealized Biasing

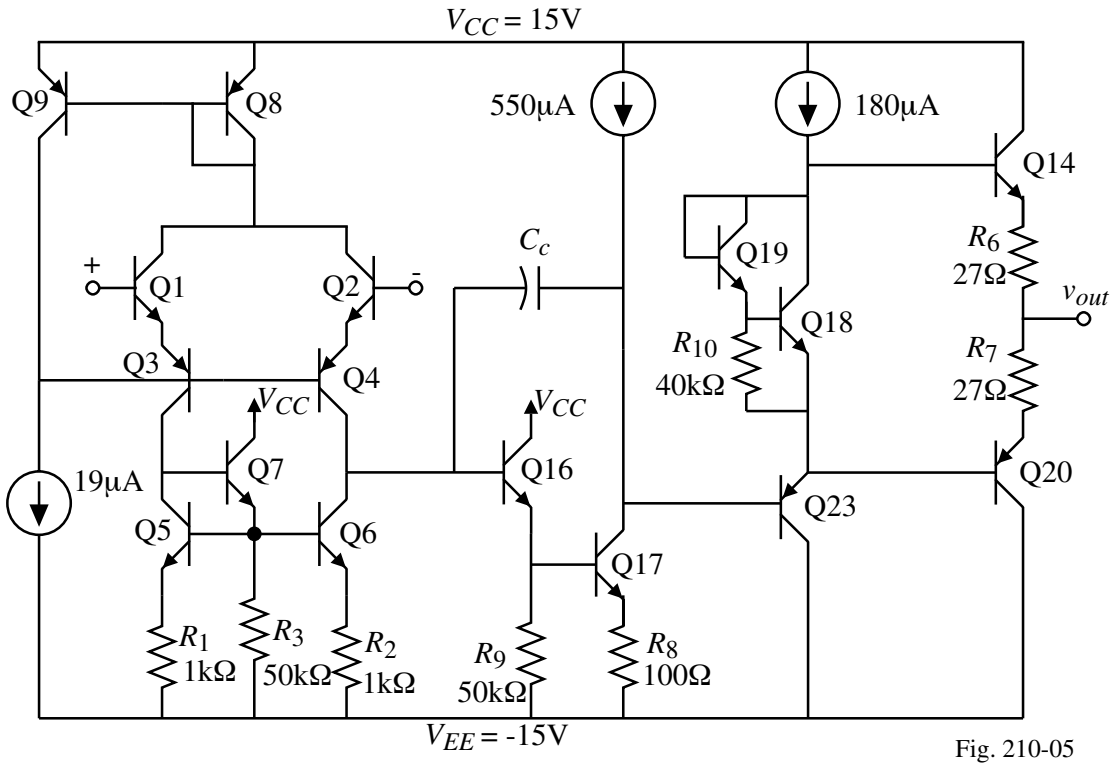


Fig. 210-05

Input Stage Biasing of the 741 Op Amp

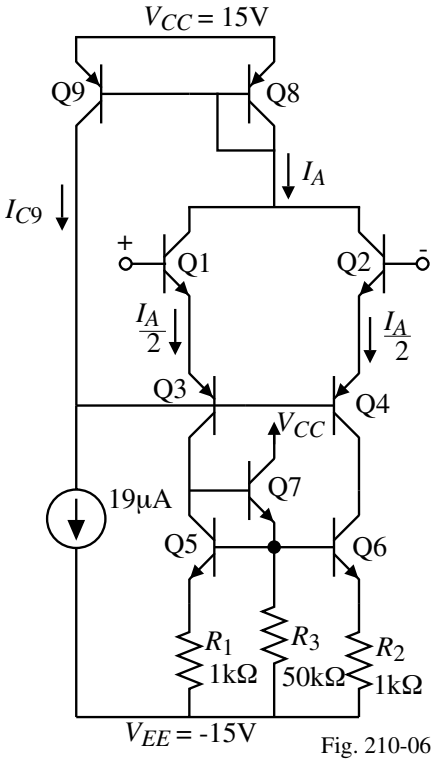


Fig. 210-06

$$I_A = I_8 = I_9 = 19\mu A$$

$$\frac{I_A}{2} = 9.5\mu A$$

$$V_{BE5} = V_t \, ln\left(\frac{9.5\mu A}{I_{SNPN}}\right) = 0.553V$$

$$I_{SNPN} = 5fA$$

$$V_{BE5} = 0.555V$$

$$V_{B5} = V_{BE5} + R_1 \cdot 9.5\mu A = 0.565V$$

$$I_{R3} = I_7 = \frac{V_{B5}}{R_3} = 11.3\mu A$$

Darlington Gain Stage Biasing

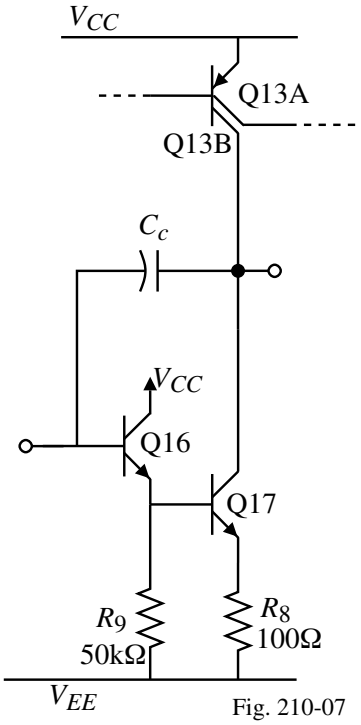


Fig. 210-07

$$V_{BE17} = V_t \, ln\left(\frac{550\mu A}{I_{SNPN}}\right)$$

$$V_{B17} = V_{BE17} + R_8 \cdot 550\mu A = 0.716V$$

$$I_{R9} = \frac{V_{B17}}{R_9} = 14.3\mu A$$

$$I_{B17} = \frac{550\mu A}{\beta+1} = 2.2\mu A$$

$$I_{16} = I_{B17} + I_{R9} = 16.5\mu A$$

Output Stage Biasing of the 741 Op Amp

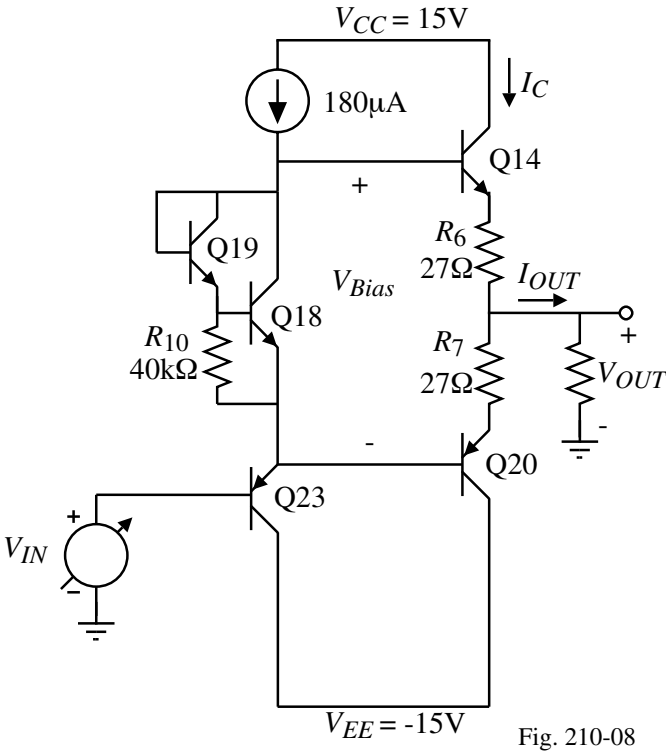


Fig. 210-08

$$I_{19} = \frac{V_t}{R_{10}} ln\left(\frac{I_{18}}{I_{SNPN}}\right)$$

$$I_{18} + I_{19} = 180\mu A$$

$$I_{18} = 164\mu A$$

$$I_{19} = 15.7\mu A$$

$$V_{BE18} + V_{BE19} \approx V_{BE14} + |V_{BE20}|$$

$$\frac{I_{18}\, I_{19}}{I_{SNPN18} I_{SNPN19}} = \frac{I_{14}^2}{I_{SNPN14} I_{SNPN20}}$$

$$I_{SNPN14} = 4.5\, I_{SNPN}$$

$$I_{S20} = 10fA$$

$$I_{14} = 150\mu A$$

741 Circuit for SPICE Simulation

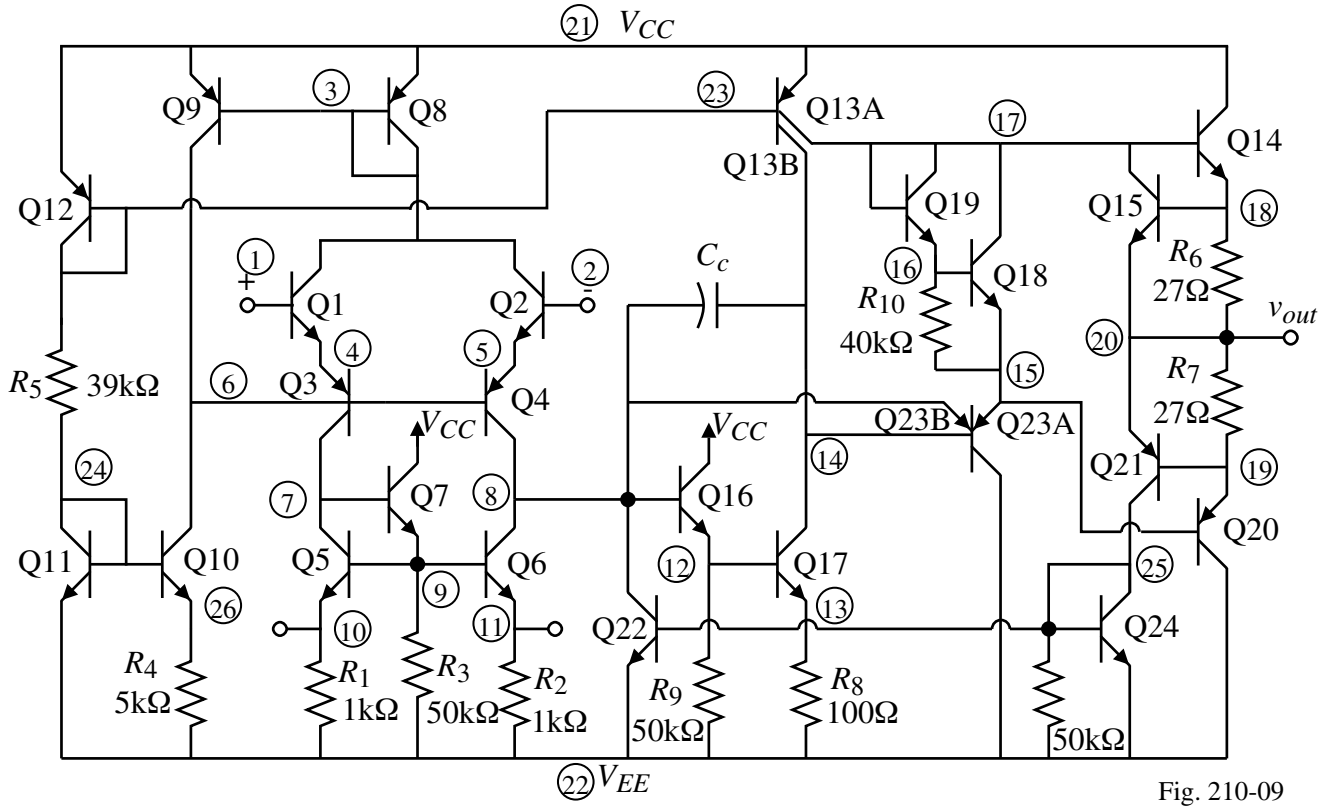


Fig. 210-09

Spice Simulations of the 741 Op Amp

```
uA741 Operational Amp Spice File
** 741 OP AMP **
* BIAS CIRCUIT *
Q12 23 23 21 PNP
Q11 24 24 22 NPN
Q10 6 24 26 NPN
Q13A 17 23 21 PNP 1
Q13B 14 23 21 PNP 3
Q15 17 18 20 NPN
Q21 25 19 20 PNP
Q22 8 25 22 NPN
Q24 25 25 22 NPN
Q23B 22 14 8 PNP
R5 23 24 39K
R4 26 22 5K
R11 25 22 50K
CC 14 8 30PF
*
* DIFF AMP *
Q1 3 1 4 NPN
Q2 3 2 5 NPN
Q3 7 6 4 PNP
Q4 8 6 5 PNP
Q5 7 9 10 NPN
Q6 8 9 11 NPN
Q7 21 7 9 NPN
Q8 3 3 21 PNP
Q9 6 3 21 PNP
R1 10 22 1K
R2 11 22 1K
R3 9 22 50K
* DARLINGTON **
Q16 21 8 12 NPN
Q17 14 12 13 NPN
R9 12 22 50K
R8 13 22 100
* OUTPUT STAGE *
Q19 17 17 16 NPN
Q18 17 16 15 NPN
Q23A 22 14 15 PNP
Q14 21 17 18 NPN 3
Q20 22 15 19 SPNP
R10 16 15 40K
R6 18 20 27
R7 20 19 22
* POWER SUPPLY *
VCC 21 0 DC=15
VEE 22 0 DC=-15
*
** ANALYSIS **
*DC Sweep to find input offset voltage
*Connect output to inverting input for unity gain buffer
*Rshort 20 2  0.001
*VIN+ 1 0 DC 0 AC 0
*.DC VIN+ -15V +15V .1V
* Now provide input offset voltage
*VIN- 2 0 DC=851.325UV AC=0
*Open Loop Gain
*Remove Rshort
*VIN+ 1 0 AC=1
*VIN- 2 0 DC=851.325UV AC=0
*.AC DEC 20 1 10MEG
```


SPICE File - Continued

```
*.TF V(20) VIN+
*Slew Rate - Connect output (node 20 to node 2 with +Rshort)
*VIN+ 1 0 PULSE (0 1 10us .001us .001us 10us 30us)
*.TRAN .5us 30us
*
.MODEL NPN NPN(IS=5E-15 RB=200 RC=250 BF=250 +BR=2 RE=2 VA=130 TF=.35NS CJE=1PF PE=.7V ME=.33
+CJC=.3PF PC=.55V MC=.5 CCS=3PF PS=.52 MS=.5V)
*
.MODEL PNP PNP(IS=2E-15 RB=300 RC=300 RE=10 +BF=50 BR=4 VA=50 TF=30NS CJE=.3PF PE=.55V ME=.5
+CJC=2PF PC=.55V MC=.5 CCS=3PF PS=.52V MS=.5V)
.MODEL SPNP PNP(IS=1E-14 RB=150 RC=50 RE=2 BR=4 BF=50 VA=50 TF=20NS CJE=.5PF PE=.55V ME=.5
+CJC=2PF PC=.52V MC=.5 CCS=3PF PS=.52V MS=.5V)
*
.OPTIONS LIMPTS=0
.PROBE
.END
```


Node Voltages

****** SMALL SIGNAL BIAS SOLUTION TEMPERATURE = 27.000 DEG C ******

NODE	VOLTAGE	NODE	VOLTAGE	NODE	VOLTAGE	NODE	VOLTAGE	NODE	VOLTAGE
(1)	0.0000	(2)	851.3E-06	(3)	14.4120	(4)	-0.5442	(5)	-0.5437
(6)	-1.1088	(7)	-13.8950	(8)	-13.4680	(9)	-14.4460	(10)	-14.9920
(11)	-14.9920	(12)	-14.0460	(13)	-14.7480	(14)	-1.3208	(15)	-0.6239
(16)	0.0454	(17)	0.6180	(18)	0.0079	(19)	-0.0064	(20)	-5.094E-06
(21)	15.0000	(22)	-15.0000	(23)	14.3030	(24)	-14.3330	(25)	-15.0000
(26)	-14.9020								

Bipolar Junction Transistors

NAME	Q1	Q2	Q3	Q4	Q5
MODEL	NPN	NPN	PNP	PNP	NPN
IB	3.44E-08	3.48E-08	-1.20E-07	-1.23E-07	3.74E-08
IC	**7.63E-06**	**7.73E-06**	**-7.55E-06**	**-7.65E-06**	**7.50E-06**
VBE	5.44E-01	5.45E-01	-5.65E-01	-5.65E-01	5.46E-01
VBC	-1.44E+01	-1.44E+01	1.28E+01	1.24E+01	-5.51E-01
VCE	1.50E+01	1.50E+01	-1.34E+01	-1.29E+01	1.10E+00
BETADC	2.22E+02	2.22E+02	6.28E+01	6.24E+01	2.01E+02
GM	2.95E-04	2.99E-04	2.92E-04	2.95E-04	2.90E-04
RPI	7.53E+05	7.43E+05	2.15E+05	2.11E+05	6.92E+05
RX	2.00E+02	2.00E+02	3.00E+02	3.00E+02	2.00E+02
RO	1.89E+07	1.87E+07	8.32E+06	8.16E+06	1.74E+07
CBE	1.59E-12	1.59E-12	9.40E-12	9.52E-12	1.59E-12
CBC	5.75E-14	5.75E-14	4.06E-13	4.13E-13	2.12E-13
CJS	5.60E-13	5.60E-13	5.70E-13	5.78E-13	4.31E-11
BETAAC	2.22E+02	2.22E+02	6.28E+01	6.23E+01	201.00
FT/FT2	2.85E+07	2.88E+07	4.73E+06	4.74E+06	2.5600e+07

NAME	Q6	Q7	Q8	Q9	Q16
MODEL	NPN	NPN	PNP	PNP	NPN
IC	**7.52E-06**	**1.11E-05**	**-1.48E-05**	**-1.93E-05**	**3.04E-05**

Bipolar Junction Transistors - Continued

NAME	Q12	Q11	Q10	Q13A	Q13B
MODEL	PNP	NPN	NPN	PNP	PNP
IB	-1.34E-05	3.66E-06	8.88E-08	-1.28E-05	-3.8200e-05
IC	**-6.70E-04**	**7.31E-04**	**1.96E-05**	**-8.13E-04**	**-2.50E-03**
VBE	-6.97E-01	6.67E-01	5.69E-01	-6.97E-01	-0.69700
VBC	0.00E+00	0.00E+00	-1.32E+01	1.37E+01	1.56E+01
VCE	-6.97E-01	6.67E-01	1.38E+01	-1.44E+01	0.0000
BETADC	4.98E+01	2.00E+02	2.20E+02	6.34E+01	0.0000
GM	2.59E-02	2.82E-02	7.57E-04	3.14E-02	0.096500
RPI	1.92E+03	7.07E+03	2.91E+05	2.02E+03	677.00
RX	3.00E+02	2.00E+02	2.00E+02	3.00E+02	100.00

NAME	Q17	Q19	Q18	Q23A	Q14	Q20
MODEL	NPN	NPN	NPN	PNP	NPN	SNPN
IC	**2.51E-03**	**2.06E-05**	**7.91E-04**	**-8.04E-04**	**2.90E-04**	**-2.87E-04**
VBE	7.02E-01	5.73E-01	6.69E-01	-6.97E-01	6.10E-01	6.10E-01

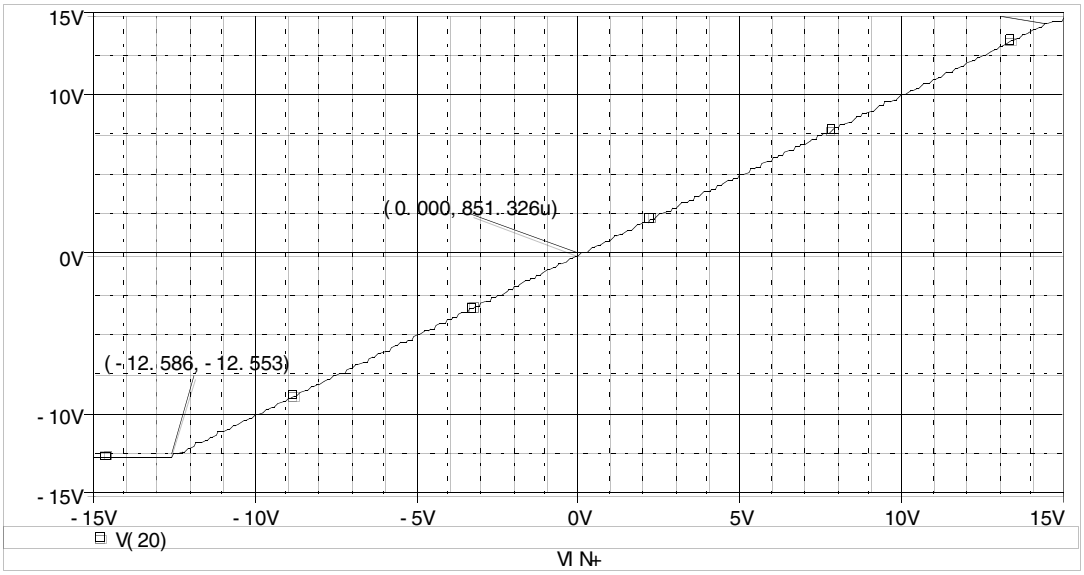
Comparison:

Transistor	Q1	Q2	Q3	Q4	Q5	Q6	Q7	Q8	Q9	Q10	Q11
Caculated	9.5μA	9.5μA	9.5μA	9.5μA	9.5μA	9.5μA	11.3μA	19μA	19μA	19μA	733μA
SPICE	7.63μA	7.73μA	7.75μA	7.65μA	7.50μA	7.52μA	11.1μA	14.8μA	19.3μA	19.6μA	731μA

Transistor	Q11	Q12	Q12	Q13A	Q13B	Q14	Q16	Q17	Q18	Q19	Q20
Caculated	733μA	733μA	733μA	813μA	550μA	150μA	16.5μA	550μA	164μA	15.7μA	150μA
SPICE	731μA	670μA	670μA	813μA	2500μA	290μA	30μA	2510μA	791μA	20.6μA	287μA

741 PSpice Simulation Results

Dynamic Range and Input Offset Voltage:



SUMMARY

- The 741 is a classic Op Amp that exemplifies many of our ECE 6412 circuit concepts
- DC bias in almost all transistors is set by R_5
- Hand calculated and PSpice bias currents compare favorably (except for Q13B)