LECTURE 220 – AC ANALYSIS OF THE 741 OP AMP
(READING: GHLM – 462-472)

Objective

The objective of this presentation is to:

1.) Identify the devices, circuits, and stages in the 741 operational amplifier

2.) Perform a small-signal analysis

3.) Compare hand calculations of small-signal analyses with PSpice simulations

Outline

- Small-signal analysis
- Frequency Compensation of 741
- PSpice analysis techniques and results
- Summary

741 OPERATIONAL AMPLIFIER

Circuit

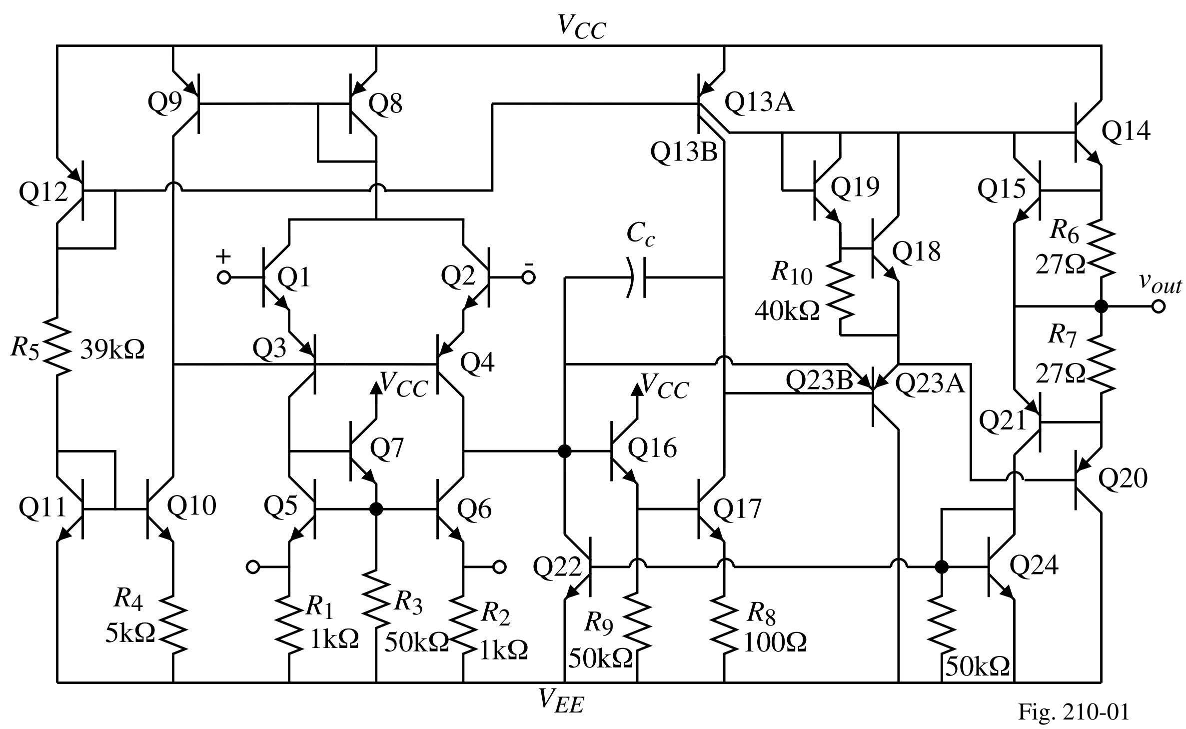


Fig. 210-01

Simplified Schematic of the 741 Op Amp with Idealized Biasing

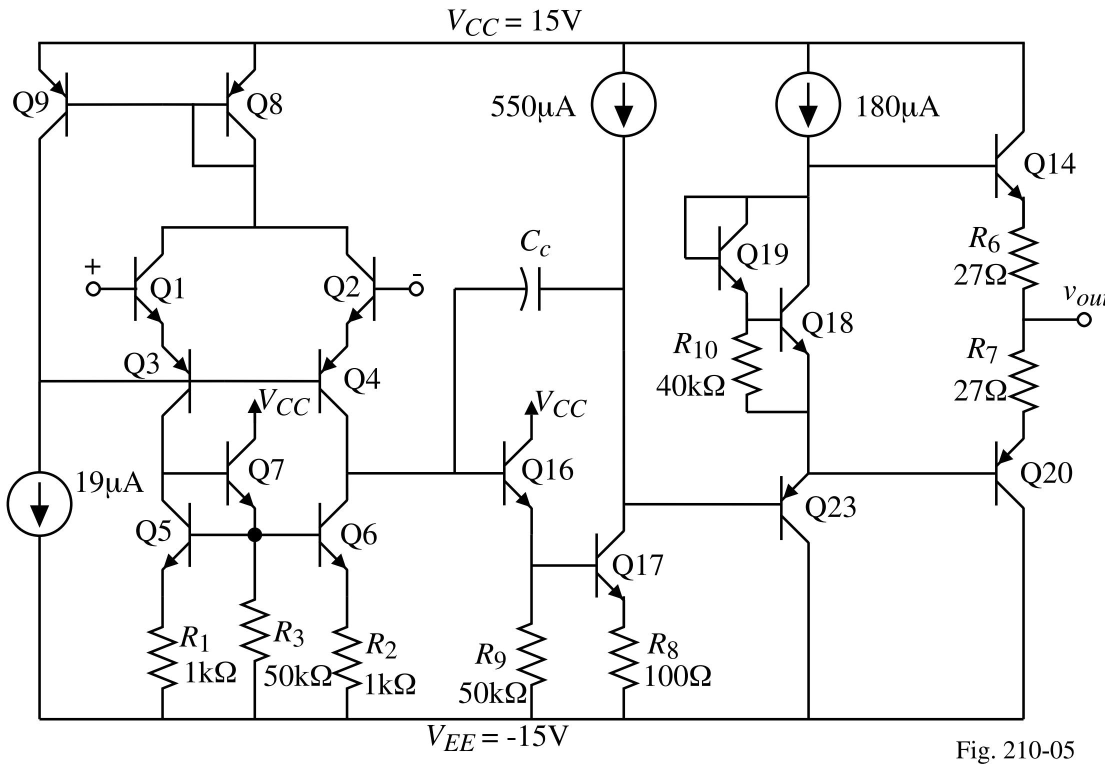


Fig. 210-05

SMALL-SIGNAL ANALYSIS OF THE 741 OP AMP

Input Stage

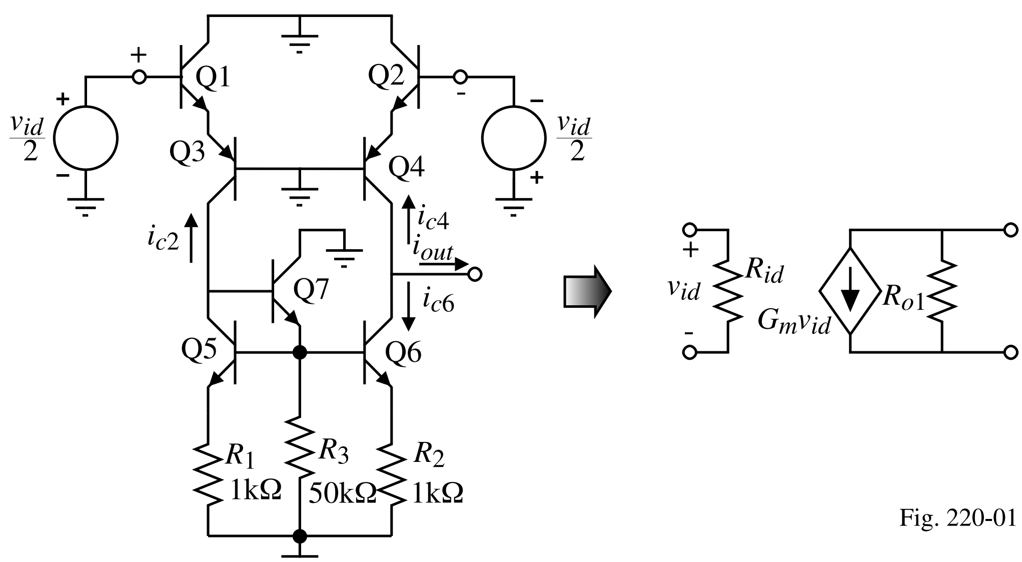


Fig. 220-01

Small-Signal Analysis of the Input Stage - Continued

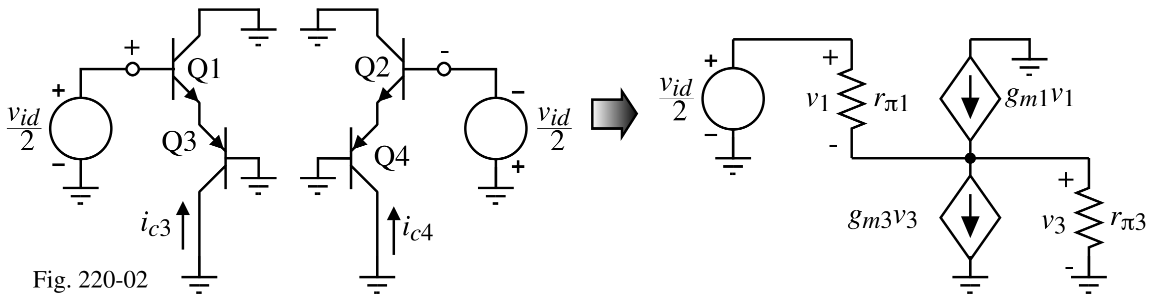


Fig. 220-02

Start with, $0.5v_{id} = v_1 + v_3$

KCL at the emitters gives,

$$g_{m1}v_1 + g_{\pi1}v_1 = g_{m3}v_3 + g_{\pi3}v_3 \quad \Rightarrow \quad g_{m1}v_1\left(1+\frac{1}{\beta_{o1}}\right) = g_{m3}v_3\left(1+\frac{1}{\beta_{o3}}\right)$$

$$\therefore \quad 0.5v_{id} = -v_3\left[\frac{g_{m3}(1+1/\beta_{o3})}{g_{m1}(1+1/\beta_{o1})} + 1\right]$$

Assuming that $g_{m1} = g_{m3}$ ($|I_{C1}| = |I_{C3}|$) and β_{o1}, $\beta_{o3} >> 1$, then

$v_3 = -v_{id}/4$ and $i_{c3} = -g_{m3}v_{id}/4$ and $i_{c4} = +g_{m4}v_{id}/4$ (symmetry)

$$\therefore \quad i_{out} = -i_{c4} + i_{c3} = -g_{m3}v_{id}/2 = -g_{m1}v_{id}/2$$

$$G_{m1} = -i_{out}/v_{id} = \frac{g_{m1}}{2} = \frac{9.5\mu A}{2(25.9mV)} = \frac{1}{5.4k\Omega} \quad \Rightarrow \quad G_{m1} = \underline{\underline{183.4\mu S}}$$

Small-Signal Analysis of the Input Stage - Continued

The input resistance can be written as

$$R_{id} = 2\left[r_{\pi1} + \frac{(\beta_N+1)r_{\pi3}}{\beta_P+1}\right]$$

Calculating the small-signal model parameters,

$$r_{\pi1} = \frac{\beta_N V_t}{I_{C1}} = 684k\Omega, \quad g_{m1} = \frac{I_{C1}}{V_t} = 365\mu S, \quad r_{\pi3} = \frac{\beta_P V_t}{I_{C3}} = 137k\Omega, \quad g_{m3} = \frac{I_{C3}}{V_t} = 365\mu S$$

$$\therefore \quad R_{id} = 2\left[r_{\pi1} + \frac{(\beta_N+1)r_{\pi3}}{\beta_P+1}\right] = \underline{\underline{2.72M\Omega}}$$

where $\beta_N \approx 250$ and $\beta_P \approx 50$

Calculation of the Input Stage Output Resistance

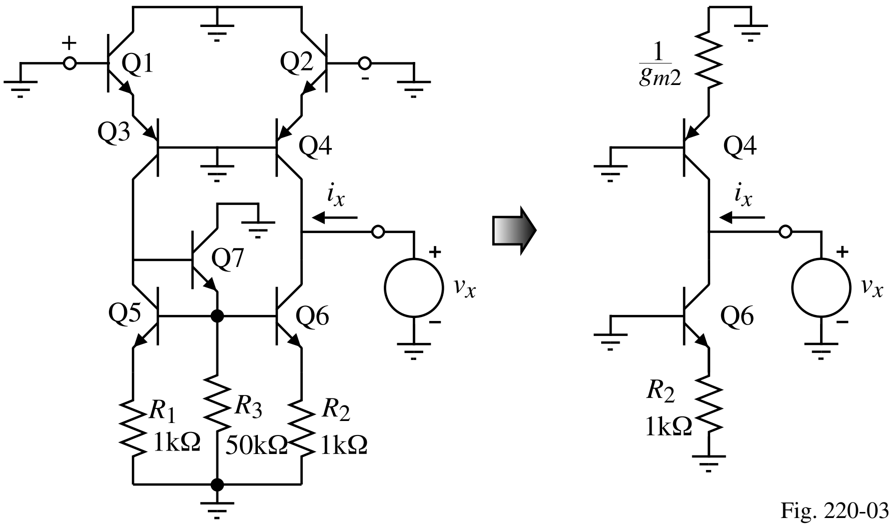


Fig. 220-03

$$r_{o4} = \frac{V_{AP}}{I_{C4}} = 5.26\text{M}\Omega \qquad r_{o4T} = r_{o4}\left(1+\frac{g_{m4}}{g_{m2}}\right) = 10.53\text{M}\Omega$$

$$r_{o6} = \frac{V_{AN}}{I_{C6}} = 13.7\text{M}\Omega \qquad r_{o6T} = r_{o6}(1+g_{m2}R_2) = 18.7\text{M}\Omega$$

$$R_{o1} = r_{o4T}||r_{o6T} = \underline{\underline{6.8\text{M}\Omega}}$$

Two-Port Equivalent Network for the Input Stage

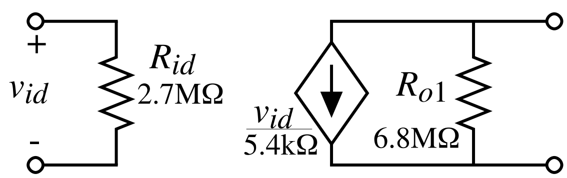


Fig. 220-04

Small-Signal Equivalent Model for the Second Stage

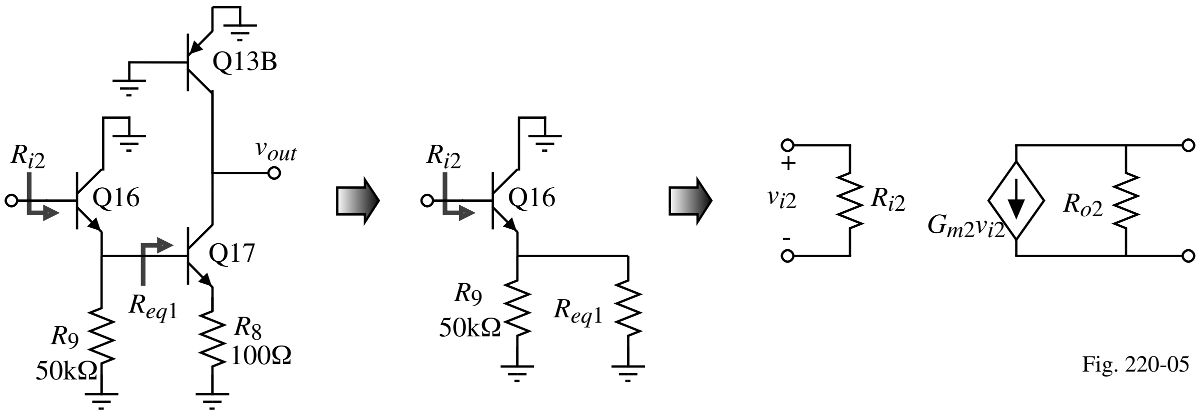


Fig. 220-05

Output Resistance:

$$r_{\pi 17} = \frac{\beta_N V_t}{I_{C17}} = 11.8\text{k}\Omega \qquad R_{eq1} = r_{\pi 17} + (\beta_N + 1)R_8 = 36.9\text{k}\Omega \qquad r_{\pi 16} = \frac{\beta_N V_t}{I_{C16}} = 394\text{k}\Omega$$

$R_{i2} = r_{\pi 16} + (\beta_N + 1)(R_9 || R_{eq1}) = \underline{5.72\text{M}\Omega}$

$\therefore$ The first-stage load is $R_{Load1} = R_{o1} || R_{i2} = 3.1\text{M}\Omega$

$A_{v1} = G_{m1}R_{Load1} = 565 \Rightarrow 55\text{dB}$

Small-Signal Equivalent Model for the Second Stage - Continued

Transconductance:

$$G_{m2} = \frac{g_{m17}}{1+g_{m17}R_8} = \underline{6.79\text{mS}} \qquad \frac{1}{G_{m2}} = \underline{147\Omega}$$

$$R_{o2} = r_{o13B} || \left[r_{o17} \left(1 + \frac{g_{m17}R_8}{1 + \frac{g_{m17}R_8}{\beta_0}} \right) \right] \approx r_{o13B} || [r_{o17}(1+g_{m17}R_8)] \quad \text{if } \beta_0 >> g_{m17}R_8$$

[Recall that the output resistance of a BJT cascoding a resistor R_E is $\approx r_o(1+g_mR_E)$]

$r_{o13B} = V_{AP}/I_{C13B} = 50\text{V}/550\mu\text{A} = 90.9\text{k}\Omega$

$r_{o17} = V_{AN}/I_{C17} = 130\text{V}/550\mu\text{A} = 236.4\text{k}\Omega$

$r_{o17T} = r_{o17}(1+g_{m17}R_8) = 732.3\text{k}\Omega \qquad R_{o2} = r_{o13B} || r_{o17T} = \underline{80.9\text{k}\Omega}$

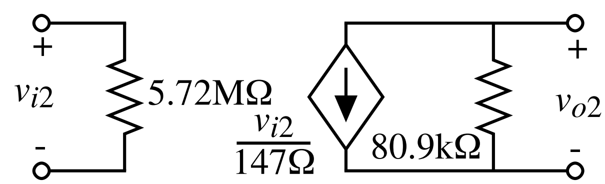


Fig. 220-09

Simplified Output-Stage Circuit

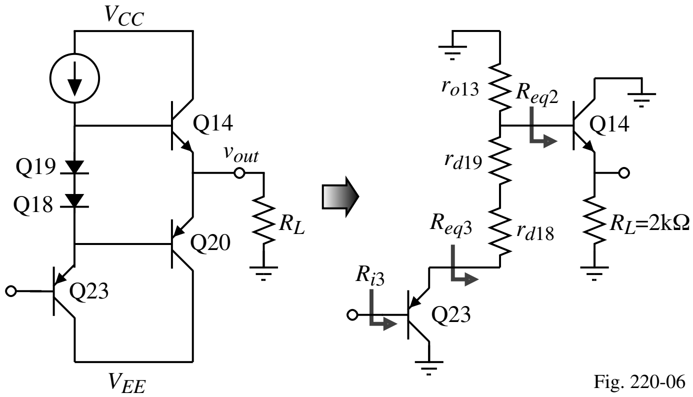


Fig. 220-06

Finding the Loading of the Output Stage on the Second Stage:

Assume a nominal load resistance of $R_L = 2\text{k}\Omega$ and that Q_{14} is supplying a 2mA current to this load. Further assume that Q_{20} is conducting very little current at this point in time.

$$r_{\pi 14} = \frac{\beta_N V_t}{I_{C14}} = 3.25\text{k}\Omega \quad (I_{C14} \approx 2\text{mA}) \qquad R_{eq2} = r_{\pi 14} + (\beta_{N14}+1)R_L = 505.3\text{k}\Omega$$

$$r_{o13A} = V_{AP}/I_{C13A} = 50\text{V}/180\mu\text{A} = 272.7\text{k}\Omega \qquad R_{eq3} \approx R_{eq2} || r_{o13A} = 177.1\text{k}\Omega$$

$$r_{\pi 23} = \frac{\beta_P V_t}{I_{C13A}} = 7.1\text{k}\Omega \qquad R_{i3} = r_{\pi 23} + (\beta_P + 1)R_{eq3} = \underline{\underline{9.04\text{M}\Omega}}$$

Output-Stage Circuit - Continued

The effective load on the second stage is therefore

$$R_{Load2} = R_{i3} || R_{o2} = 80.15\text{k}\Omega$$

$$A_{v2} = G_{m2} R_{Load2} = 544.2 \Rightarrow 54.7\text{dB}$$

$$A_{vT} = A_{v1} A_{v2} = (565.1)(544.4) = 307{,}700 \Rightarrow 109.8\text{dB}$$

Equivalent Circuit for Calculation of the Output Resistance:

$$R_{eq4} = r_{o13A} || [r_{d19} + r_{d18} + \frac{R_{o2} + r_{\pi 23A}}{(\beta+1)}] = 2.00\text{k}\Omega$$

$$R_{out} = \frac{R_{eq4} + r_{\pi 14}}{\beta + 1} = 21\Omega$$

$$R_{outtotal} = 21\Omega + 27\Omega = 48\Omega$$

Voltage gain:

Assume the voltage gain is 1.

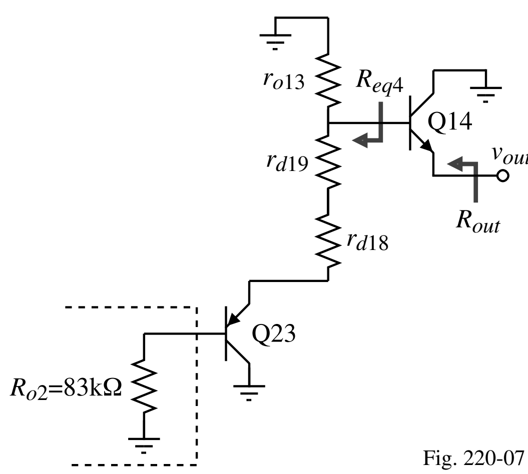


Fig. 220-07

Small-Signal Equivalent Circuit for the Complete 741 Op Amp

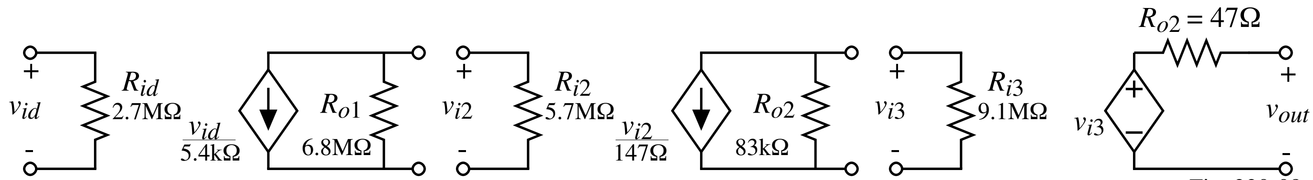


Fig. 220-08

Voltage gain = 109.8dB

Differential input resistance = 2.72MΩ

Output resistance = 48Ω

741 Circuit for SPICE Simulation

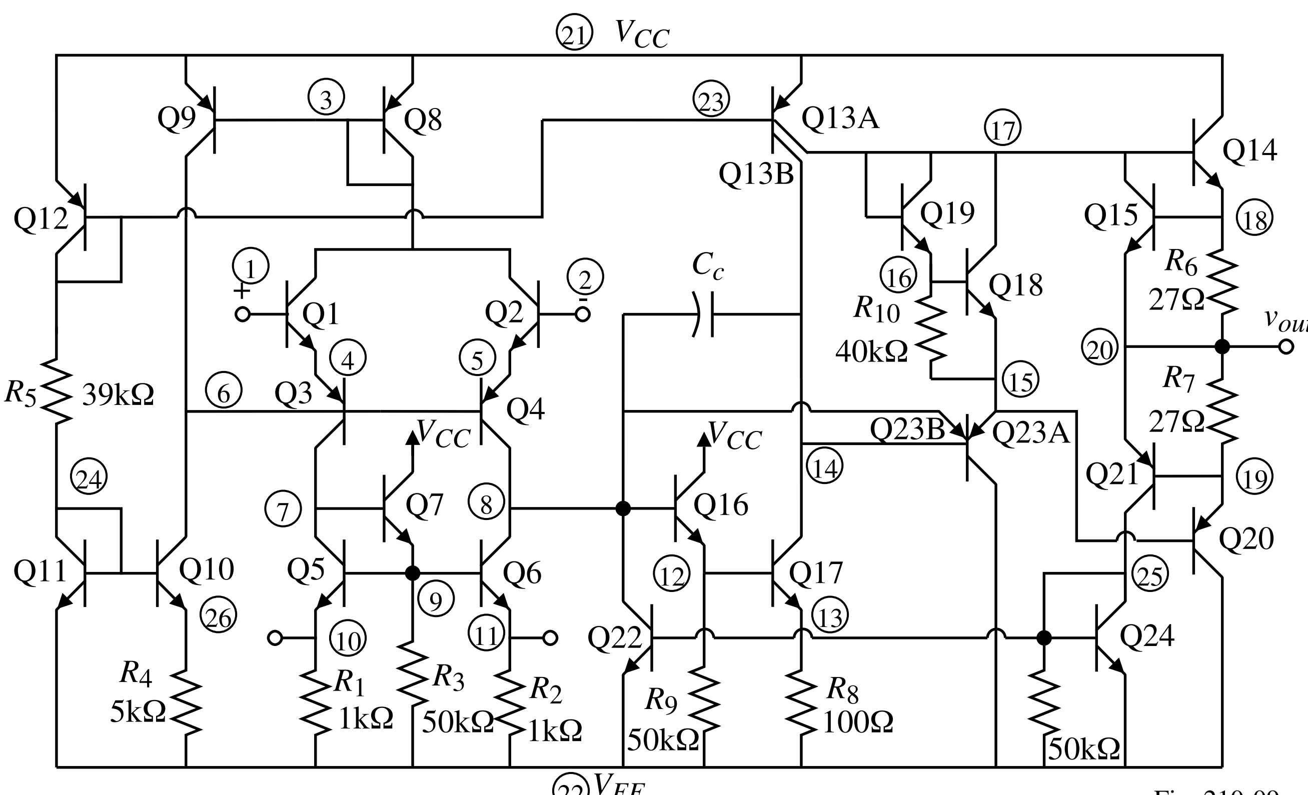


Fig. 210-09

Spice Simulations of the 741 Op Amp

```
uA741 Operational Amp Spice File
** 741 OP AMP **
* BIAS CIRCUIT *
Q12 23 23 21 PNP
Q11 24 24 22 NPN
Q10 6 24 26 NPN
Q13A 17 23 21 PNP 1
Q13B 14 23 21 PNP 3
Q15 17 18 20 NPN
Q21 25 19 20 PNP
Q22 8 25 22 NPN
Q24 25 25 22 NPN
Q23B 22 14 8 PNP
R5 23 24 39K
R4 26 22 5K
R11 25 22 50K
CC 14 8 30PF
*
* DIFF AMP *
Q1 3 1 4 NPN
Q2 3 2 5 NPN
Q3 7 6 4 PNP
Q4 8 6 5 PNP
Q5 7 9 10 NPN
Q6 8 9 11 NPN
Q7 21 7 9 NPN
Q8 3 3 21 PNP
Q9 6 3 21 PNP
R1 10 22 1K
R2 11 22 1K
R3 9 22 50K
* DARLINGTON **
Q16 21 8 12 NPN
Q17 14 12 13 NPN
R9 12 22 50K
R8 13 22 100
* OUTPUT STAGE *
Q19 17 17 16 NPN
Q18 17 16 15 NPN
Q23A 22 14 15 PNP
Q14 21 17 18 NPN 3
Q20 22 15 19 SPNP
R10 16 15 40K
R6 18 20 27
R7 20 19 22
* POWER SUPPLY *
VCC 21 0 DC=15
VEE 22 0 DC=-15
*
** ANALYSIS **
*DC Sweep to find input offset voltage
*Connect output to inverting input for unity gain buffer
*Rshort 20 2  0.001
*VIN+ 1 0 DC 0 AC 0
*.DC VIN+ -15V +15V .1V
* Now provide input offset voltage
*VIN- 2 0 DC=851.325UV AC=0
*Open Loop Gain
*Remove Rshort
*VIN+ 1 0 AC=1
*VIN- 2 0 DC=851.325UV AC=0
*.AC DEC 20 1 10MEG
```


SPICE File - Continued

```
*.TF V(20) VIN+
*Slew Rate - Connect output (node 20 to node 2 with +Rshort)
*VIN+ 1 0 PULSE (0 1 10us .001us .001us 10us 30us)
*.TRAN .5us 30us
*
.MODEL NPN NPN(IS=5E-15 RB=200 RC=250 BF=250 +BR=2 RE=2 VA=130 TF=.35NS CJE=1PF PE=.7V ME=.33
+CJC=.3PF PC=.55V MC=.5 CCS=3PF PS=.52 MS=.5V)
*
.MODEL PNP PNP(IS=2E-15 RB=300 RC=300 RE=10 +BF=50 BR=4 VA=50 TF=30NS CJE=.3PF PE=.55V ME=.5
+CJC=2PF PC=.55V MC=.5 CCS=3PF PS=.52V MS=.5V)
.MODEL SPNP PNP(IS=1E-14 RB=150 RC=50 RE=2 +BR=4 BF=50 VA=50 TF=20NS CJE=.5PF PE=.55V ME=.5
+CJC=2PF PC=.52V MC=.5 CCS=3PF PS=.52V MS=.5V)
*
.OPTIONS LIMPTS=0
.PROBE
.END
```

Node Voltages

****** SMALL SIGNAL BIAS SOLUTION TEMPERATURE = 27.000 DEG C ******

NODE	VOLTAGE	NODE	VOLTAGE	NODE	VOLTAGE	NODE	VOLTAGE	NODE	VOLTAGE
(1)	0.0000	(2)	851.3E-06	(3)	14.4120	(4)	-0.5442	(5)	-0.5437
(6)	-1.1088	(7)	-13.8950	(8)	-13.4680	(9)	-14.4460	(10)	-14.9920
(11)	-14.9920	(12)	-14.0460	(13)	-14.7480	(14)	-1.3208	(15)	-0.6239
(16)	0.0454	(17)	0.6180	(18)	0.0079	(19)	-0.0064	(20)	-5.094E-06
(21)	15.0000	(22)	-15.0000	(23)	14.3030	(24)	-14.3330	(25)	-15.0000
(26)	-14.9020								

Bipolar Junction Transistors

NAME	Q1	Q2	Q3	Q4	Q5
MODEL	NPN	NPN	PNP	PNP	NPN
IB	3.44E-08	3.48E-08	-1.20E-07	-1.23E-07	3.74E-08
IC	7.63E-06	7.73E-06	-7.55E-06	-7.65E-06	7.50E-06
VBE	5.44E-01	5.45E-01	-5.65E-01	-5.65E-01	5.46E-01
VBC	-1.44E+01	-1.44E+01	1.28E+01	1.24E+01	-5.51E-01
VCE	1.50E+01	1.50E+01	-1.34E+01	-1.29E+01	1.10E+00
BETADC	2.22E+02	2.22E+02	6.28E+01	6.24E+01	2.01E+02
GM	2.95E-04	2.99E-04	2.92E-04	2.95E-04	2.90E-04
RPI	7.53E+05	7.43E+05	2.15E+05	2.11E+05	6.92E+05
RX	2.00E+02	2.00E+02	3.00E+02	3.00E+02	2.00E+02
RO	1.89E+07	1.87E+07	8.32E+06	8.16E+06	1.74E+07
CBE	1.59E-12	1.59E-12	9.40E-12	9.52E-12	1.59E-12
CBC	5.75E-14	5.75E-14	4.06E-13	4.13E-13	2.12E-13
CJS	5.60E-13	5.60E-13	5.70E-13	5.78E-13	4.31E-11
BETAAC	2.22E+02	2.22E+02	6.28E+01	6.23E+01	201.00
FT/FT2	2.85E+07	2.88E+07	4.73E+06	4.74E+06	2.5600e+07

NAME	Q6	Q7	Q8	Q9	Q16
MODEL	NPN	NPN	PNP	PNP	NPN
IC	7.52E-06	1.11E-05	-1.48E-05	-1.93E-05	3.04E-05

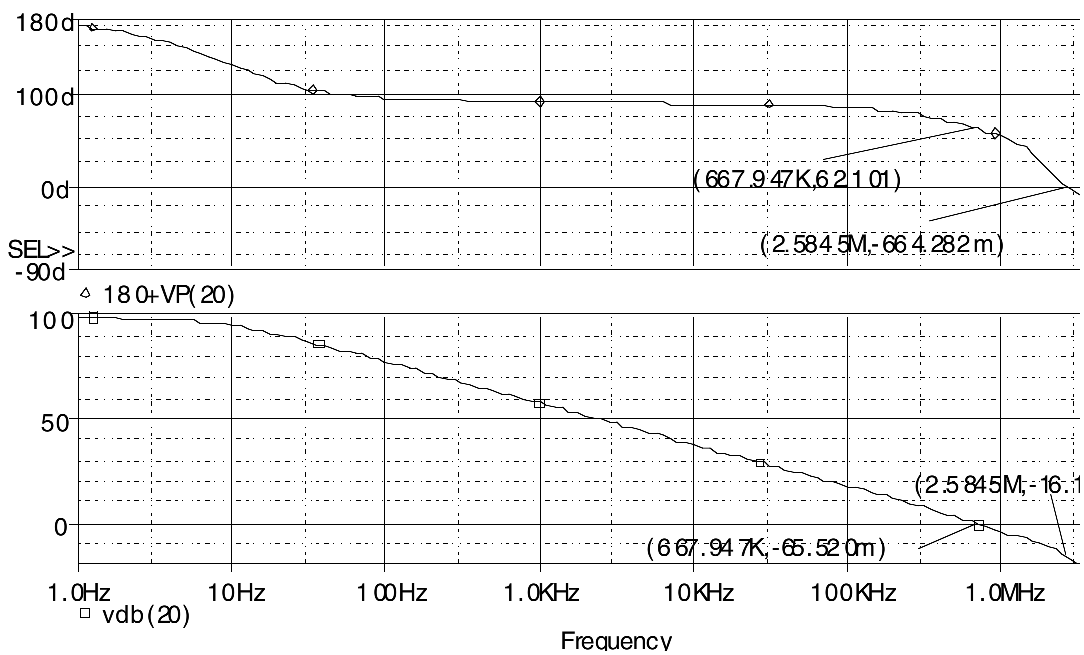
Bipolar Junction Transistors - Continued

NAME	Q12	Q11	Q10	Q13A	Q13B
MODEL	PNP	NPN	NPN	PNP	PNP
IB	-1.34E-05	3.66E-06	8.88E-08	-1.28E-05	-3.8200e-05
IC	-6.70E-04	7.31E-04	1.96E-05	-8.13E-04	-2.50E-03
VBE	-6.97E-01	6.67E-01	5.69E-01	-6.97E-01	-0.69700
VBC	0.00E+00	0.00E+00	-1.32E+01	1.37E+01	1.56E+01
VCE	-6.97E-01	6.67E-01	1.38E+01	-1.44E+01	0.0000
BETADC	4.98E+01	2.00E+02	2.20E+02	6.34E+01	0.0000
GM	2.59E-02	2.82E-02	7.57E-04	3.14E-02	0.096500
RPI	1.92E+03	7.07E+03	2.91E+05	2.02E+03	677.00
RX	3.00E+02	2.00E+02	2.00E+02	3.00E+02	100.00

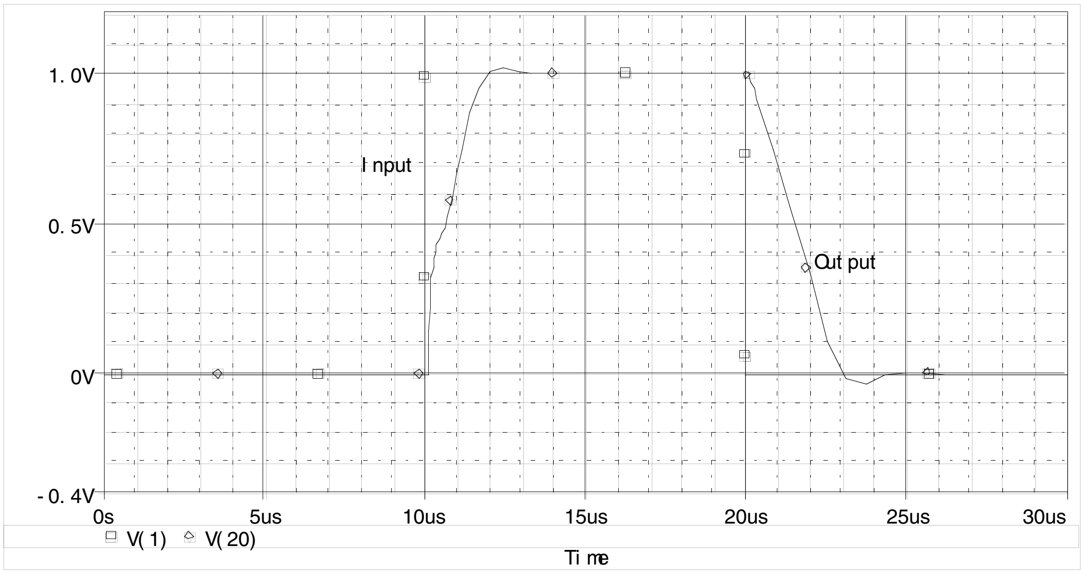
NAME	Q17	Q19	Q18	Q23A	Q14	Q20
MODEL	NPN	NPN	NPN	PNP	NPN	SNPN
IC	2.51E-03	2.06E-05	7.91E-04	-8.04E-04	2.90E-04	-2.87E-04
VBE	7.02E-01	5.73E-01	6.69E-01	-6.97E-01	6.10E-01	6.10E-01

741 PSPICE SIMULATION RESULTS

Open Loop Voltage Gain (Magnitude and Phase)



Closed Loop Step Response



SUMMARY

- The 741 is a classic Op Amp that exemplifies many of our ECE 6412 circuit concepts
- The PSpice voltage gain is lower than for hand calculations due to more complete model parameters
- The gain bandwidth product for the 741 is approximately 1 MHz
- The first 741 was designed, laid out, and fabricated by engineers without computers or calculators and has stood the test of time