LECTURE 240 – SIMULATION AND MEASUREMENTS OF OP AMPS
(READING: AH – 310-323)

Simulation and Measurement Considerations

Objectives:

- The objective of simulation is to verify and optimize the design.
- The objective of measurement is to experimentally confirm the specifications.

Similarity Between Simulation and Measurement:

- Same goals
- Same approach or technique

Differences Between Simulation and Measurement:

- Simulation can idealize a circuit
- Measurement must consider all nonidealities

Simulating or Measuring the Open-Loop Transfer Function of the Op Amp

Circuit (Darkened op amp identifies the op amp under test):

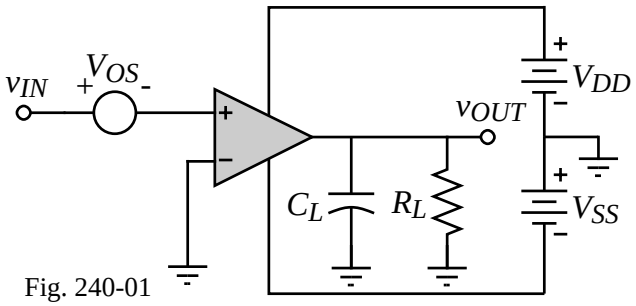


Fig. 240-01

Simulation:

This circuit will give the voltage transfer function curve. This curve should identify:

1.) The linear range of operation
2.) The gain in the linear range
3.) The output limits
4.) The systematic input offset voltage
5.) DC operating conditions, power dissipation
6.) When biased in the linear range, the small-signal frequency response can be obtained
7.) From the open-loop frequency response, the phase margin can be obtained ($F = 1$)

Measurement:

This circuit probably will not work unless the op amp gain is very low.

A More Robust Method of Measuring the Open-Loop Frequency Response

Circuit:

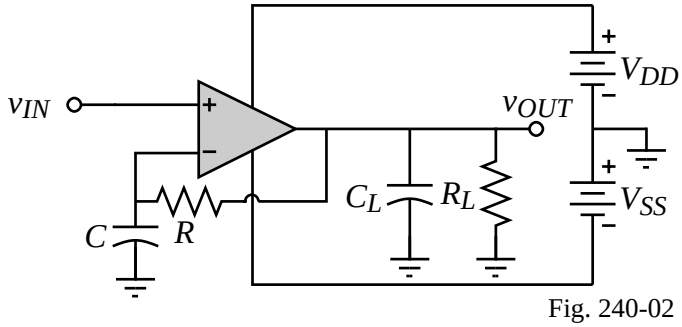


Fig. 240-02

Resulting Closed-Loop Frequency Response:

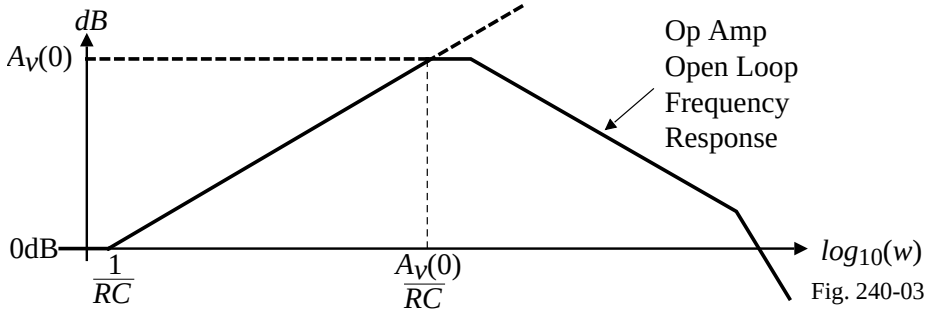


Fig. 240-03

Make the *RC* product as large as possible.

Simulation and Measurement of Open-Loop Frequency Response with Moderate Gain Op Amps

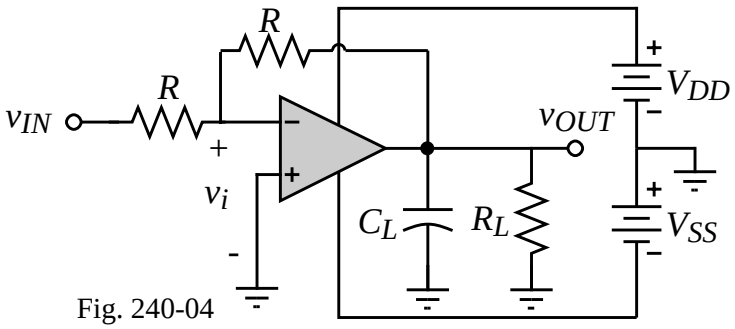


Fig. 240-04

Make *R* as large and measure v_{out} and v_i to get the open loop gain.

Simulation or Measurement of the Input Offset Voltage of an Op Amp

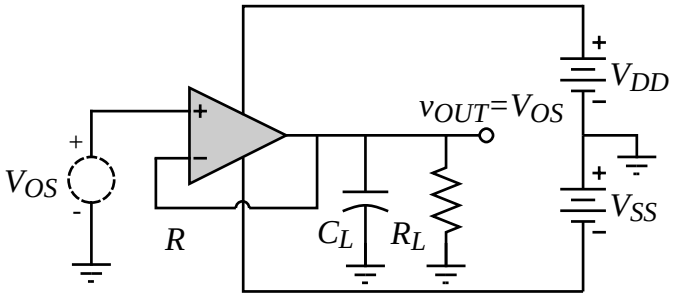


Fig. 240-05

Types of offset voltages:

1.) Systematic offset - due to mismatches in current mirrors, exists even with ideally matched transistors.

2.) Mismatch offset - due to mismatches in transistors (normally not available in simulation except through Monte Carlo methods).

Simulation of the Common-Mode Voltage Gain

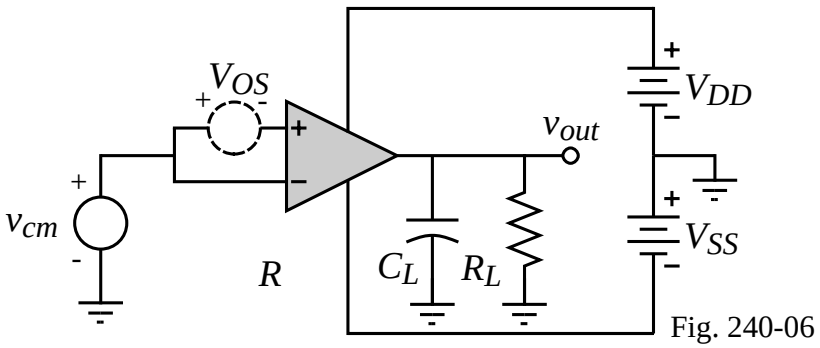


Fig. 240-06

Make sure that the output voltage of the op amp is in the linear region.

Measurement of CMRR and PSRR

Configuration:

Note that $v_I \approx \frac{v_{OS}}{1000}$ or $v_{OS} \approx 1000 v_I$

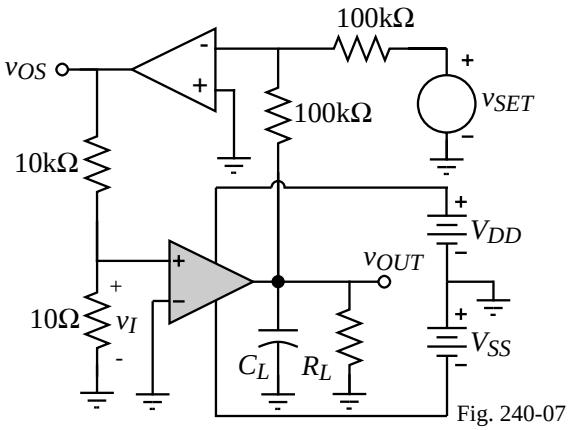


Fig. 240-07

How Does this Circuit Work?

CMRR:

1.) Set
$V_{DD}' = V_{DD} + 1V$
$V_{SS}' = V_{SS} + 1V$
$v_{OUT}' = v_{OUT} + 1V$

2.) Measure v_{OS} called v_{OS1}

3.) Set
$V_{DD}' = V_{DD} - 1V$
$V_{SS}' = V_{SS} - 1V$
$v_{OUT}' = v_{OUT} - 1V$

4.) Measure v_{OS} called v_{OS2}

5.) $\text{CMRR} = \frac{2000}{|v_{OS2} - v_{OS1}|}$

PSRR:

1.) Set
$V_{DD}' = V_{DD} + 1V$
$V_{SS}' = V_{SS}$
$v_{OUT}' = 0V$

2.) Measure v_{OS} called v_{OS3}

3.) Set
$V_{DD}' = V_{DD} - 1V$
$V_{SS}' = V_{SS}$
$v_{OUT}' = 0V$

4.) Measure v_{OS} called v_{OS4}

5.) $\text{PSRR}^+ = \frac{2000}{|v_{OS4} - v_{OS3}|}$

Note:

1.) PSRR^- can be measured similar to PSRR^+ by changing only V_{SS}.

2.) The ±1V perturbation can be replaced by a sinusoid to measure CMRR or PSRR as follows:

$\text{PSRR}^+ = \frac{1000 \cdot v_{dd}}{v_{os}}$, $\text{PSRR}^- = \frac{1000 \cdot v_{ss}}{v_{os}}$

and $\text{CMRR} = \frac{1000 \cdot v_{cm}}{v_{os}}$

How Does the Previous Idea Work?

A circuit is shown which is used to measure the *CMRR* and *PSRR* of an op amp. Prove that the *CMRR* can be given as

$$CMRR = \frac{1000\, v_{icm}}{v_{os}}$$

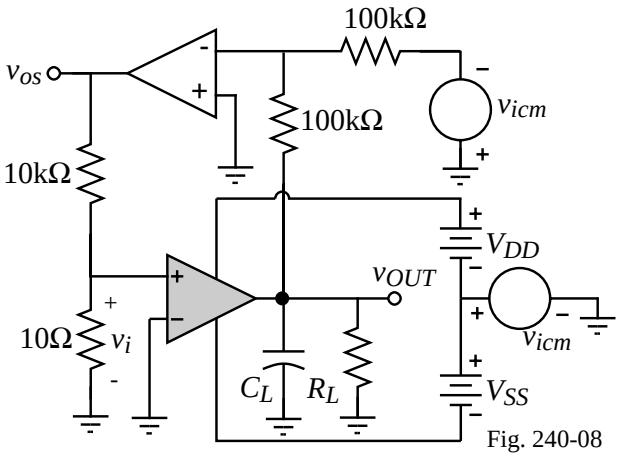


Fig. 240-08

Solution

The definition of the common-mode rejection ratio is

$$CMRR = \left|\frac{A_{vd}}{A_{cm}}\right| = \frac{(v_{out}/v_{id})}{(v_{out}/v_{icm})}$$

However, in the above circuit the value of v_{out} is the same so that we get

$$CMRR = \frac{v_{icm}}{v_{id}}$$

But $v_{id} = v_i$ and $v_{os} \approx 1000 v_i = 1000 v_{id} \Rightarrow v_{id} = \frac{v_{os}}{1000}$

Substituting in the previous expression gives, $CMRR = \frac{\frac{v_{icm}}{v_{os}}}{\frac{1}{1000}} = \frac{1000\, v_{icm}}{v_{os}}$

Simulation of CMRR of an Op Amp

None of the above methods are really suitable for simulation of *CMRR*.
Consider the following:

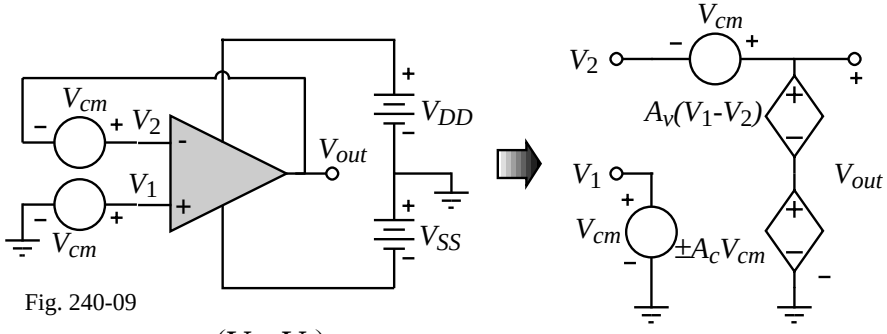


Fig. 240-09

$$V_{out} = A_v(V_1\text{-}V_2) \pm A_{cm}\left(\frac{V_1+V_2}{2}\right) = -A_v V_{out} \pm A_{cm} V_{cm}$$

$$V_{out} = \frac{\pm A_{cm}}{1+A_v} V_{cm} \approx \frac{\pm A_{cm}}{A_v} V_{cm}$$

$$\therefore \quad \boxed{|CMRR| = \frac{A_v}{A_{cm}} = \frac{V_{cm}}{V_{out}}}$$

(However, $PSRR^+ = PSRR^-$)

CMRR of Ex. 6.3-1 using the Above Method of Simulation

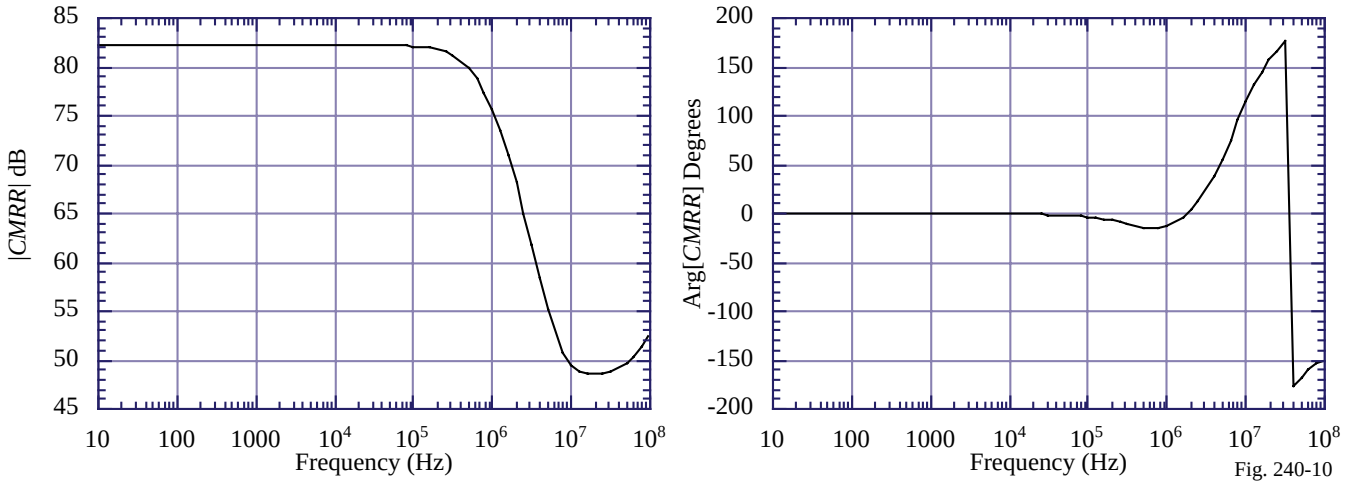


Fig. 240-10

Simulation or Measurement of *ICMR*

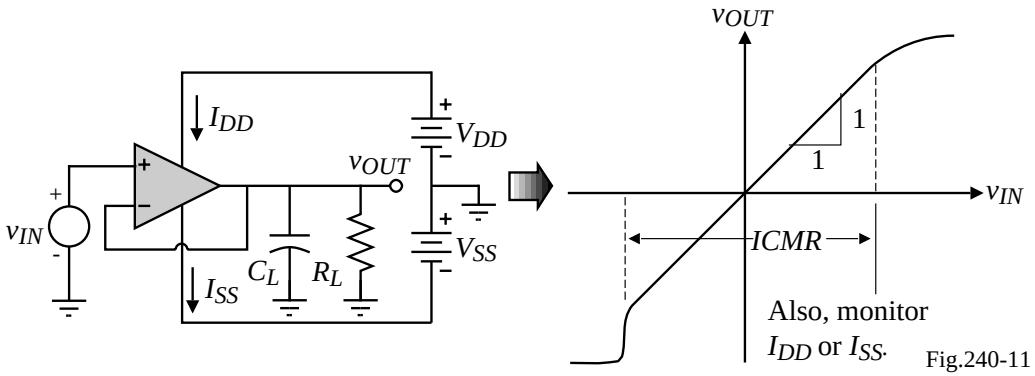


Fig.240-11

Initial jump in sweep is due to the turn-on of M5.

Should also plot the current in the input stage (or the power supply current).

Measurement or Simulation of the Open-Loop Output Resistance

Method 1:

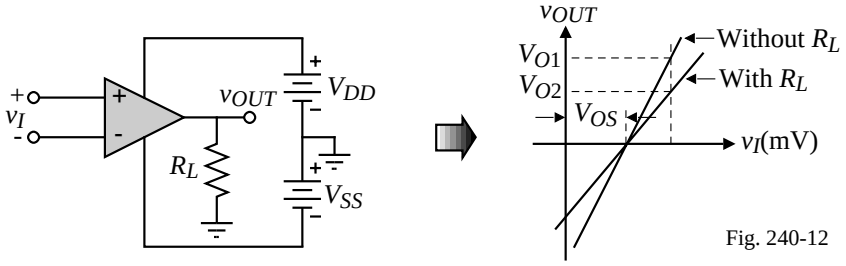


Fig. 240-12

$$R_{\text{out}} = R_L\left(\frac{V_{01}}{V_{02}} - 1\right) \qquad \text{or vary } R_L \text{ until } V_{O2} = 0.5V_{O1} \Rightarrow R_{out} = R_L$$

Method 2:

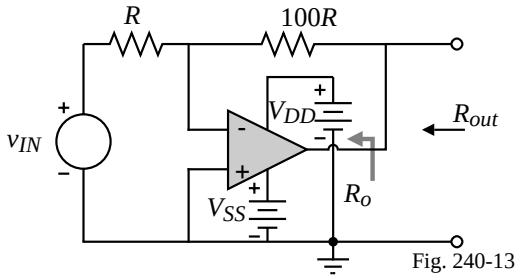


Fig. 240-13

$$R_{\text{out}} = \left(\frac{1}{R_o} + \frac{1}{100R} + \frac{A_v}{100R_o}\right)^{-1} \cong \frac{100R_o}{A_v}$$

Measurement or Simulation of Slew Rate and Settling Time

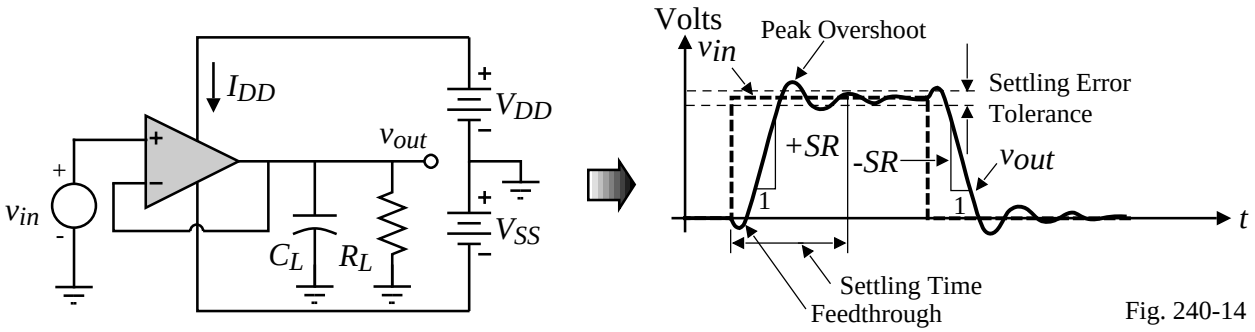


Fig. 240-14

If the slew rate influences the small signal response, then make the input step size small enough to avoid slew rate (i.e. less than 0.5V for MOS).

Phase Margin and Peak Overshoot Relationship

It can be shown (Appendix C) that:

$$\text{Phase Margin (Degrees)} = 57.2958 \cos^{-1}\left[\sqrt{4\zeta^4+1} - 2\zeta^2\right]$$

$$\text{Overshoot (\%)} = 100 \exp\left(\frac{-\pi\zeta}{\sqrt{1-\zeta^2}}\right)$$

For example, a 5% overshoot corresponds to a phase margin of approximately 64°.

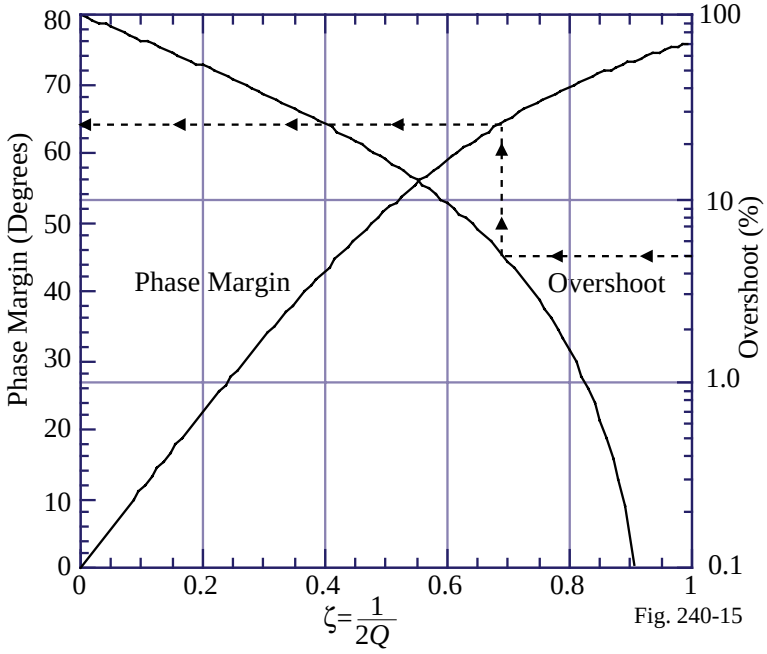


Fig. 240-15

Example 1 Simulation of the CMOS Op Amp of Ex. 6.3-1.

The op amp designed in Example 6.3-1 and shown in Fig. 6.3-3 is to be analyzed by SPICE to determine if the specifications are met. The device parameters to be used are those of Tables 3.1-2 and 3.2-1. In addition to verifying the specifications of Example 6.3-1, we will simulate PSRR+ and PSRR-.

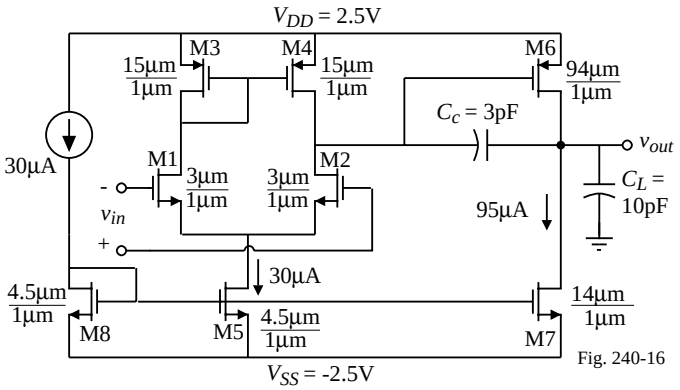


Fig. 240-16

Solution/Simulation

The op amp will be treated as a subcircuit in order to simplify the repeated analyses. The table on the next page gives the SPICE subcircuit description of Fig. 6.3-3. While the values of *AD*, *AS*, *PD*, and *PS* could be calculated if the physical layout was complete, we will make an educated estimate of these values by using the following approximations.

$$AS = AD \cong W[L1 + L2 + L3]$$

$$PS = PD \cong 2W + 2[L1 + L2 + L3]$$

where $L1$ is the minimum allowable distance between the polysilicon and a contact in the moat (Rule 5C of Table 2.6-1), $L2$ is the length of a minimum-size square contact to moat (Rule 5A of Table 2.6-1), and $L3$ is the minimum allowable distance between a contact to moat and the edge of the moat (Rule 5D of Table 2.6-1).

Example 1 - Continued

Op Amp Subcircuit:

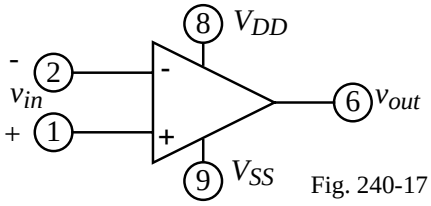


Fig. 240-17

```
.SUBCKT OPAMP 1 2 6 8 9
M1 4 2 3 3 NMOS1 W=3U L=1U AD=18P AS=18P PD=18U PS=18U
M2 5 1 3 3 NMOS1 W=3U L=1U AD=18P AS=18P PD=18U PS=18U
M3 4 4 8 8 PMOS1 W=15U L=1U AD=90P AS=90P PD=42U PS=42U
M4 5 4 8 8 PMOS1 W=15U L=1U AD=90P AS=90P PD=42U PS=42U
M5 3 7 9 9 NMOS1 W=4.5U L=1U AD=27P AS=27P PD=21U PS=21U
M6 6 5 8 8 PMOS1 W=94U L=1U AD=564P AS=564P PD=200U PS=200U
M7 6 7 9 9 NMOS1 W=14U L=1U AD=84P AS=84P PD=40U PS=40U
M8 7 7 9 9 NMOS1 W=4.5U L=1U AD=27P AS=27P PD=21U PS=21U
CC 5 6 3.0P
.MODEL NMOS1 NMOS VTO=0.70 KP=110U GAMMA=0.4 LAMBDA=0.04 PHI=0.7
+MJ=0.5 MJSW=0.38 CGBO=700P CGSO=220P CGDO=220P CJ=770U CJSW=380P
+LD=0.016U TOX=14N
.MODEL PMOS1 PMOS VTO=-0.7 KP=50U GAMMA=0..57 LAMBDA=0.05 PHI=0.8
+MJ=0.5 MJSW=.35 CGBO=700P CGSO=220P CGDO=220P CJ=560U CJSW=350P +LD=0.014U TOX=14N
IBIAS 8 7 30U
.ENDS
```


Example 1 - Continued

PSPICE Input File for the Open-Loop Configuration:

```
EXAMPLE 1 OPEN LOOP CONFIGURATION
.OPTION LIMPTS=1000
VIN+ 1 0 DC 0 AC 1.0
VDD 4 0 DC 2.5
VSS 0 5 DC 2.5
VIN - 2 0 DC 0
CL 3 0 10P
X1 1 2 3 4 5 OPAMP
      ⋮
(Subcircuit of previous slide)
      ⋮
.OP
.TF V(3) VIN+
.DC VIN+ -0.005 0.005 100U
.PRINT DC V(3)
.AC DEC 10 1 10MEG
.PRINT AC VDB(3) VP(3)
.PROBE      (This entry is unique to PSPICE)
.END
```


Example 1 - Continued

Open-loop transfer characteristic of Example 6.3-1:

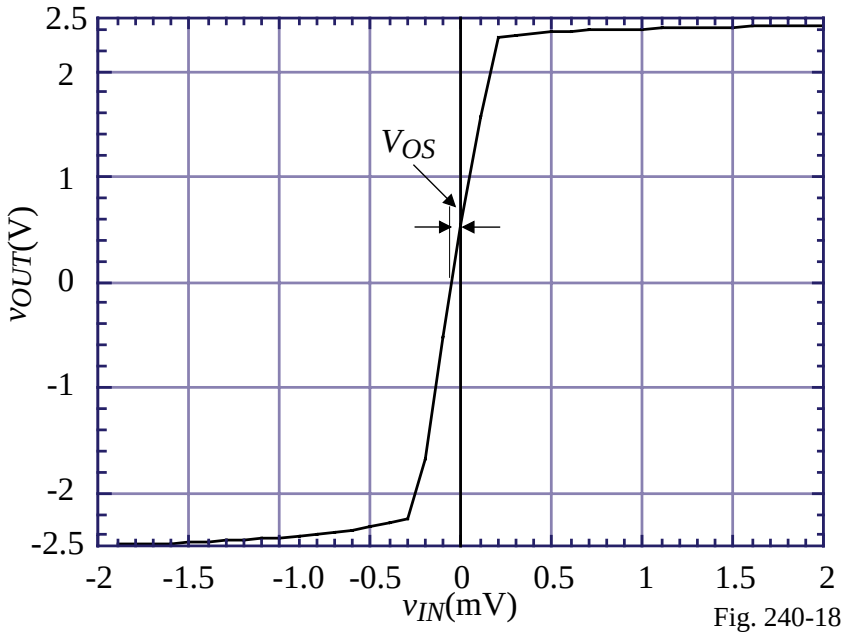
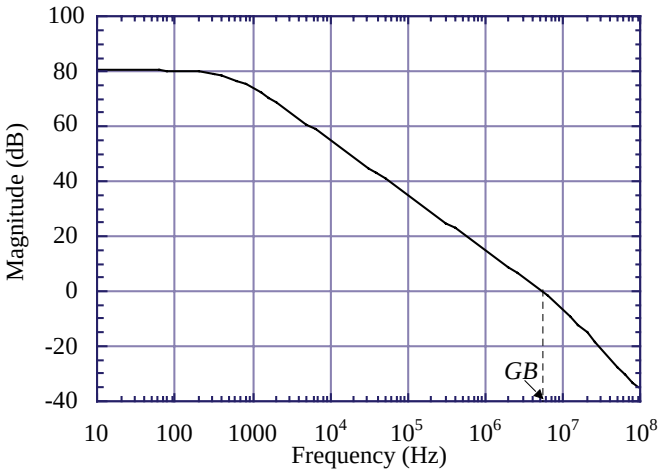


Fig. 240-18

Example 1 - Continued

Open-loop transfer frequency response of Example 6.3-1:



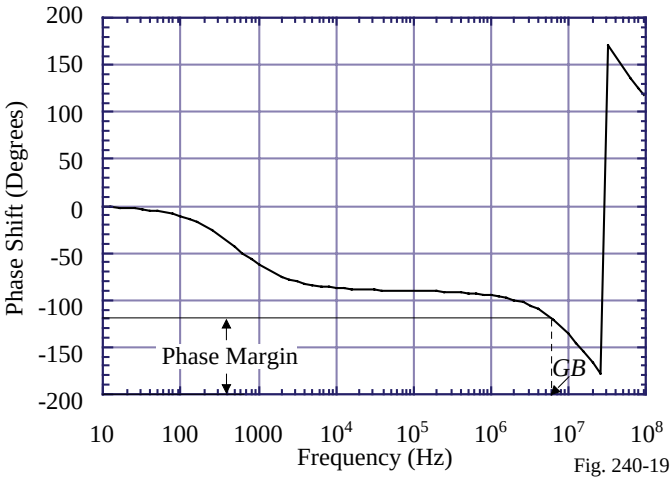


Fig. 240-19

Example 1 - Continued

Input common mode range of Example 6.3-1:

```
EXAMPLE 6.6-1 UNITY GAIN CONFIGURATION.
.OPTION LIMPTS=501
VIN+ 1 0 PWL(0 -2 10N -2 20N 2 2U 2 2.01U -2 4U  -2 4.01U
+ -.1 6U -.1 6.0 1U .1 8U .1 8.01U -.1  10U -.1)
VDD 4 0 DC 2.5 AC 1.0
VSS 0 5 DC 2.5
CL 3 0 20P
X1 1 3 3 4 5 OPAMP
        .
        .
        .
(Subcircuit of Table 6.6-1)
        .
        .
        .
.DC VIN+ -2.5 2.5  0.1
.PRINT DC V(3)
.TRAN 0.05U 10U 0 10N
.PRINT TRAN V(3) V(1)
.AC DEC 10 1 10MEG
.PRINT AC VDB(3) VP(3)
.PROBE   (This entry is unique to PSPICE)
.END
```

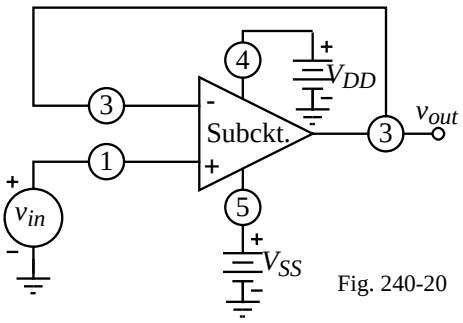


Fig. 240-20

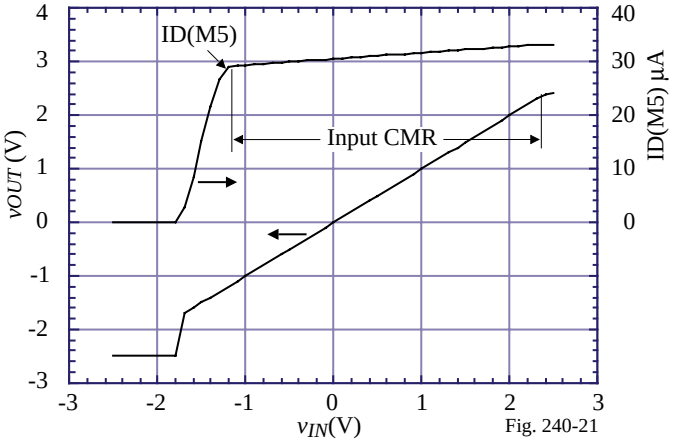


Fig. 240-21

Example 1 - Continued

Positive *PSRR* of Example 6.3-1:

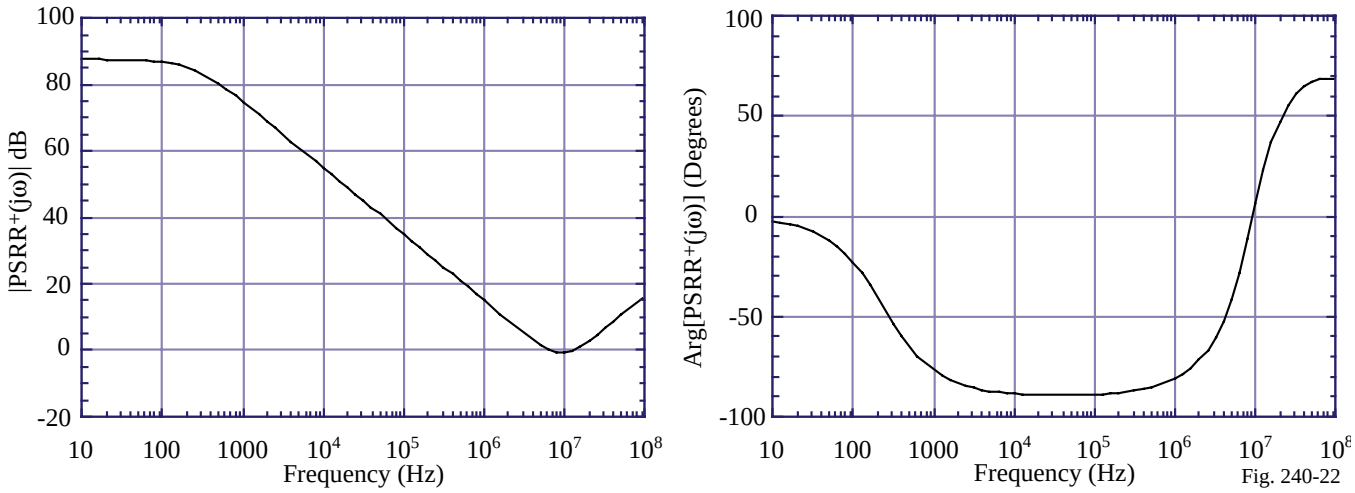


Fig. 240-22

Example 1 - Continued

Negative *PSRR* of Example 6.3-1:

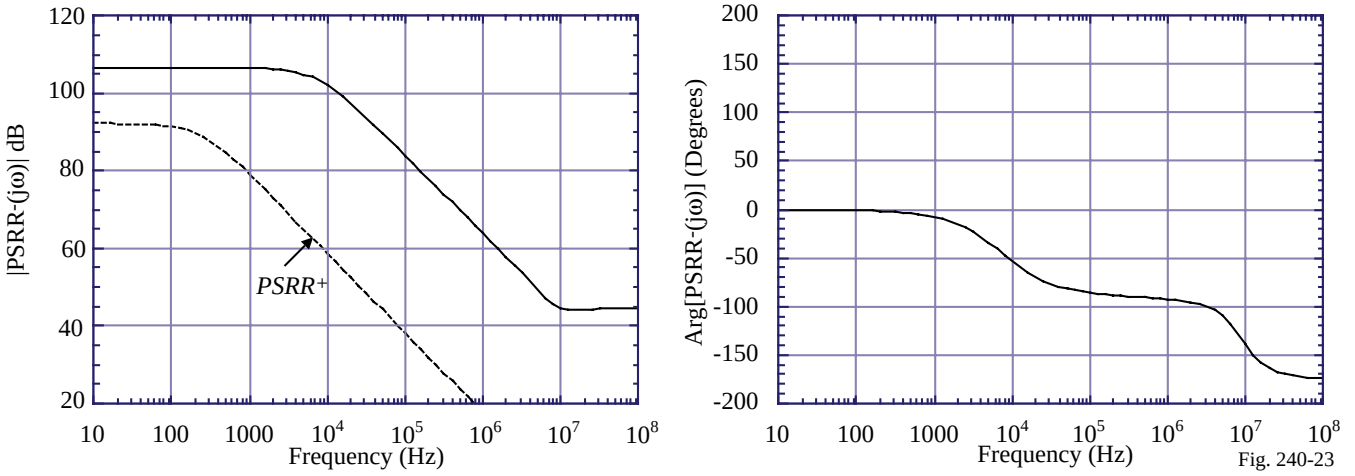


Fig. 240-23

Example 1 – Continued

Large-signal and small-signal transient response of Example 6.3-1:

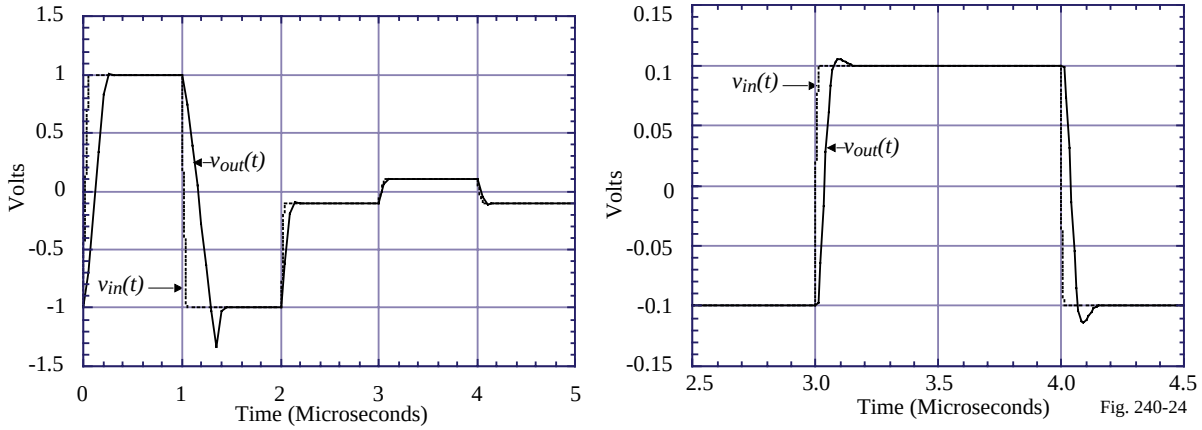


Fig. 240-24

Why the negative overshoot on the slew rate?

If M7 cannot sink sufficient current then the output stage slews and only responds to changes at the output via the feedback path which involves a delay.

Note that $-dv_{out}/dt \approx -2V/0.3\mu s = -6.67V/\mu s$. For a 10pF capacitor this requires 66.7µA and only 95µA-66.7µA = 28µA is available for C_c. For the positive slew rate, M6 can provide whatever current is required by the capacitors and can immediately respond to changes at the output.

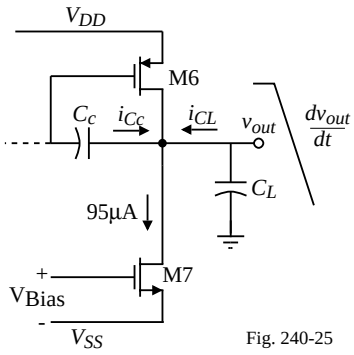


Fig. 240-25

Example 1 - Continued

Why is the negative-going overshoot larger than the positive-going overshoot on the small-signal transient response of the last slide?

Consider the following circuit and waveform:

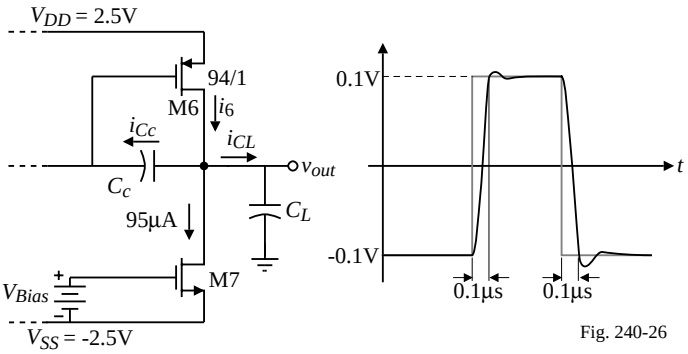


Fig. 240-26

During the rise time,

(The material beneath this box is part of a homework solution)

Example 1 - Continued

Comparison of the Simulation Results with the Specifications of Example 6.3-1:

Specification (Power supply = ±2.5V)	Design (Ex. 6.3-1)	Simulation (Ex. 1)
Open Loop Gain	>5000	10,000
GB (MHz)	5 MHz	5 MHz
Input CMR (Volts)	-1V to 2V	-1.2 V to 2.4 V,
Slew Rate (V/µsec)	>10 (V/µsec)	+10, -7(V/µsec)
P_{diss} (mW)	< 2mW	0.625mW
V_{out} range (V)	±2V	+2.3V, -2.2V
$PSRR^+$ (0) (dB)	-	87
$PSRR^-$ (0) (dB)	-	106
Phase margin (degrees)	60°	65°
Output Resistance (kΩ)	-	122.5kΩ

SUMMARY

Simulation is a key step in electrical design - it is the step to verify and optimize

Measurement is a key step in the overall design - electrical→physical→measurement

Similarities between simulation and measurement:

- Same desired responses
- Same general method to approach the result

Dissimilarities between simulation and measurement:

- Measurement using nonideal components and simulation has ideal components
- Can access internal nodes with simulation
- Can create artificial configurations with simulation
- Parasitics are a problem with measurement