LECTURE 300 – BUFFERED OP AMPS
(READING: AH – 352-368)

Objective

The objective of this presentation is:

1.) Illustrate the method of lowering the output resistance of simple op amps

2.) Show examples

Outline

- Open-loop, MOSFET buffered op amps
- Closed-loop MOSFET buffered op amps
- BJT output op amps
- Summary

Goal

To illustrate the degrees of freedom and choices of different circuit architectures that can enhance the performance of a given op amp.

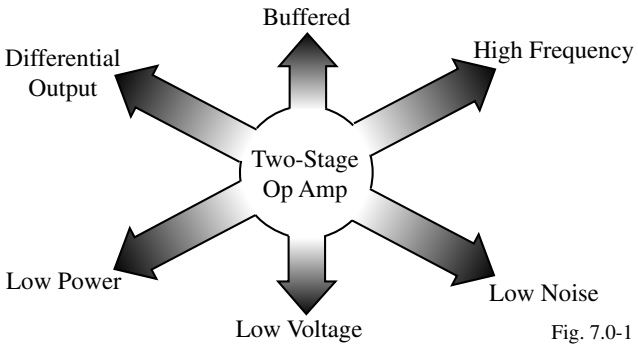


Fig. 7.0-1

What is a Buffered Op Amp?

A buffered op amp is an op amp with a low value of output resistance, R_O.

Typically, $10\Omega \leq R_O \leq 1000\Omega$

Requirements

Generally the same as for the output amplifier:

- Low output resistance
- Large output signal swing
- Low distortion
- High efficiency

Types of Buffered Op Amps

- Buffered op amps using MOSFETs
  With and without negative feedback
- Buffered op amps using BJTs

Source-Follower, Push-Pull Output Op Amp

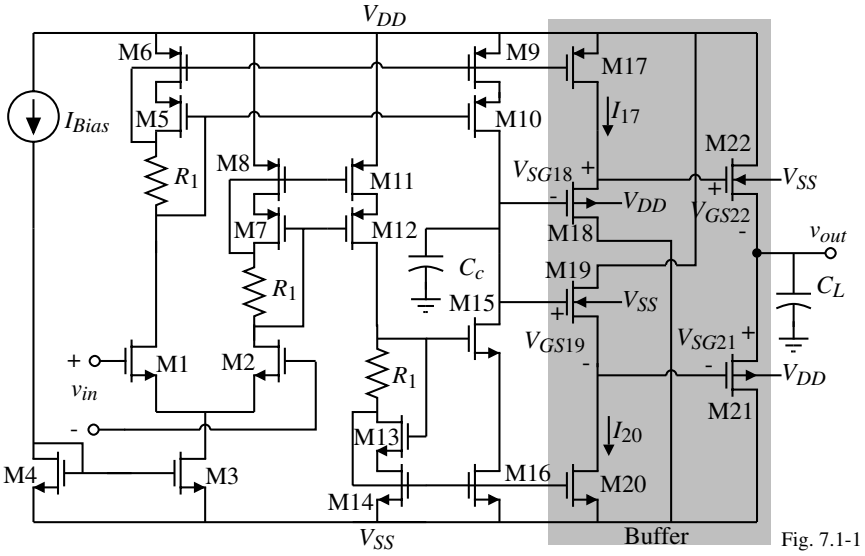


Fig. 7.1-1

$R_{out} = \frac{1}{g_{m21}+g_{m22}} \leq 1000\Omega$, $A_v(0) = 65\text{dB}$ (I_{Bias}=50μA), and $GB = 60\text{MHz}$ for $C_L = 1\text{pF}$

Output bias current?

M18-M19-M21-M22 loop $\Rightarrow V_{SG18}+V_{GS19} = V_{SG21}+V_{GS22}$

which gives $$\sqrt{\frac{2I_{18}}{K_P S_{18}}}+\sqrt{\frac{2I_{19}}{K_N S_{19}}}=\sqrt{\frac{2I_{21}}{K_P S_{21}}}+\sqrt{\frac{2I_{22}}{K_N S_{22}}}$$

Crossover-Inverter, Buffer Stage Op Amp

Principle: If the buffer has high output resistance and voltage gain (common source), this is okay if when loaded by a small R_L the gain of this stage is approximately unity.

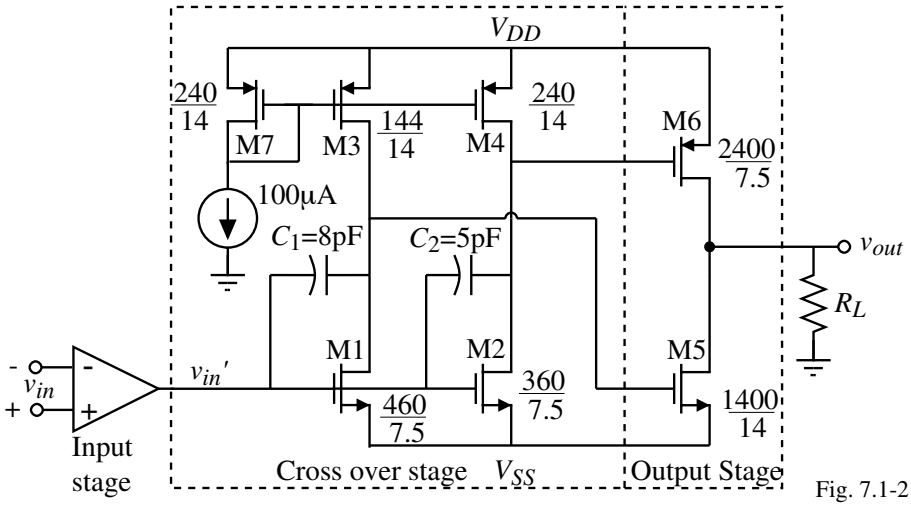


Fig. 7.1-2

This op amp is capable of delivering 160mW to a 100Ω load while only dissipating 7mW of quiescent power!

Crossover-Inverter, Buffer Stage Op Amp - Continued

How does the output buffer work?

The two inverters, M1-M3 and M2-M4 are designed to work over different regions of the buffer input voltage, v_{in}'.

Consider the idealized voltage transfer characteristic of the crossover inverters:

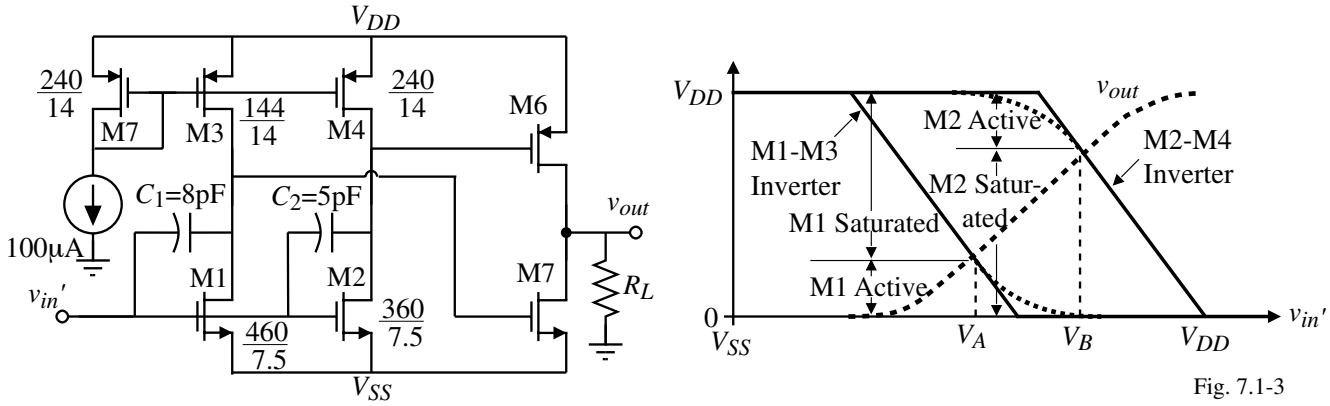


Fig. 7.1-3

Crossover voltage ≡ $V_C = V_B - V_A \geq 0$

V_C is designed to be small and positive for worst case variations in processing (Maximum value of $V_C \approx 110$mV)

Crossover-Inverter, Buffer Stage Op Amp - Continued

Performance Results for the Crossover-Inverter, Buffer Stage CMOS Op Amp

Specification	Performance
Supply Voltage	± 6 V
Quiescent Power	7 mW
Output Swing (100Ω Load)	8.1 Vpp
Open-Loop Gain (100Ω Load)	78.1 dB
Unity Gainbandwidth	260kHz
Voltage Spectral Noise Density at 1kHz	1.7 $\mu V/\sqrt{Hz}$
PSRR at 1kHz	55 dB
CMRR at 1kHz	42 dB
Input Offset Voltage (Typical)	10 mV

Compensation of Op Amps with Output Amplifiers

Compensation of a three-stage amplifier:

This op amp introduces a third pole, p'_3 (what about zeros?)

With no compensation,

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{-A_{vo}}{\left(\frac{s}{p'_1} - 1\right)\left(\frac{s}{p'_2} - 1\right)\left(\frac{s}{p'_3} - 1\right)}$$

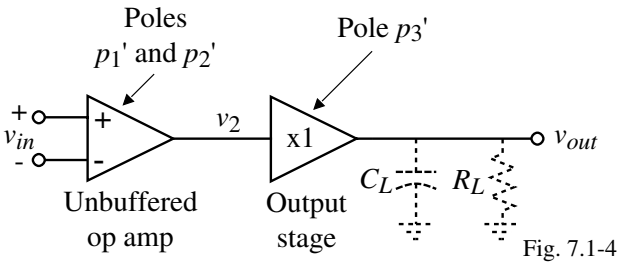
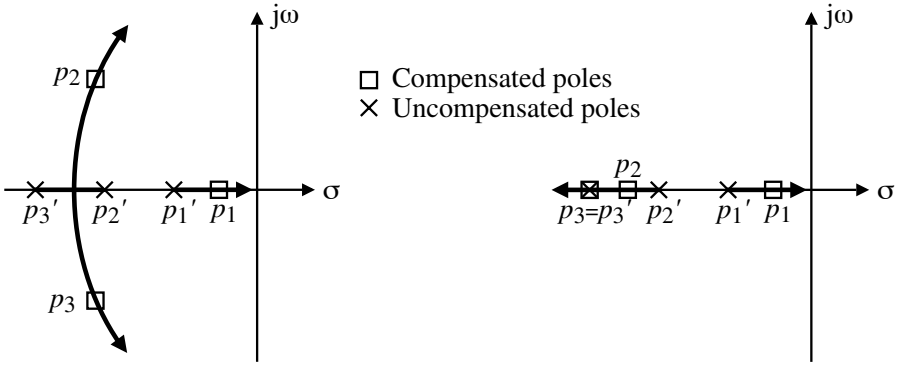


Fig. 7.1-4

Illustration of compensation choices:



Miller compensation applied around both the second and the third stage.

Miller compensation applied around the second stage only.

Fig. 7.1-5

Low Output Resistance Op Amp

To get low output resistance using MOSFETs, negative feedback must be used.

Ideal implementation:

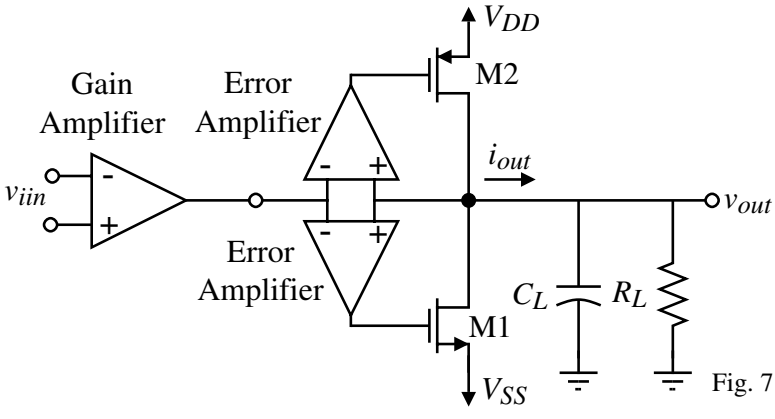


Fig. 7.1-5A

Comments:

- The output resistance will be equal to $r_{ds1} \| r_{ds2}$ divided by the loop gain
- If the error amplifiers are not perfectly matched, the bias current in M1 and M2 is not defined

Low Output Resistance Op Amp - Continued

Offset correction circuitry:

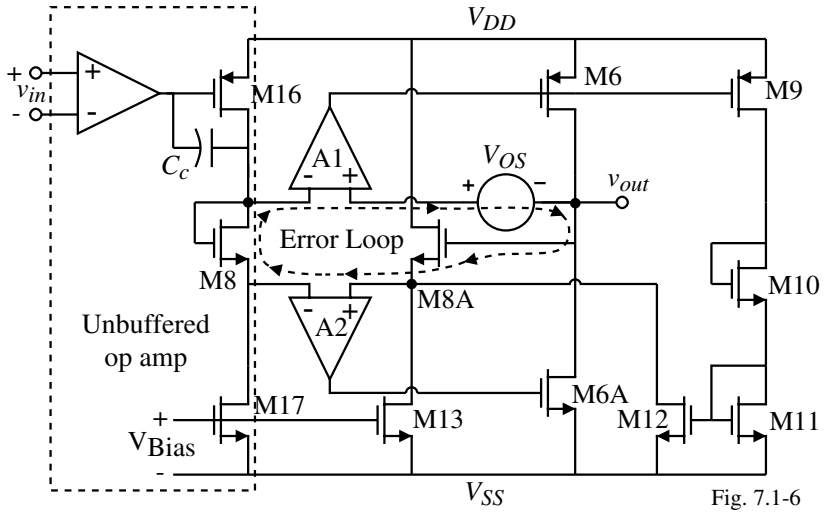


Fig. 7.1-6

The feedback circuitry of the two error amplifiers tries to insure that the voltages in the loop sum to zero. Without the M9-M12 feedback circuit, there is no way to adjust the output for any error in the loop. The circuit works as follows:

When V_{OS} is positive, M6 tries to turn off and so does M6A. I_{M9} reduces thus reducing I_{M12}. A reduction in I_{M12} reduces I_{M8A} thus decreasing V_{GS8A}. V_{GS8A} ideally decreases by an amount equal to V_{OS}. A similar result holds for negative offsets and offsets in *EA*2.

Low Output Resistance Op Amp - Continued

Error amplifiers:

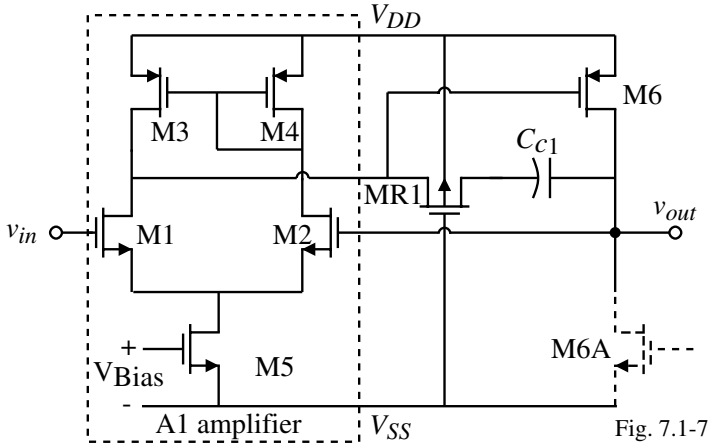


Fig. 7.1-7

Low Output Resistance Op Amp - Complete Schematic

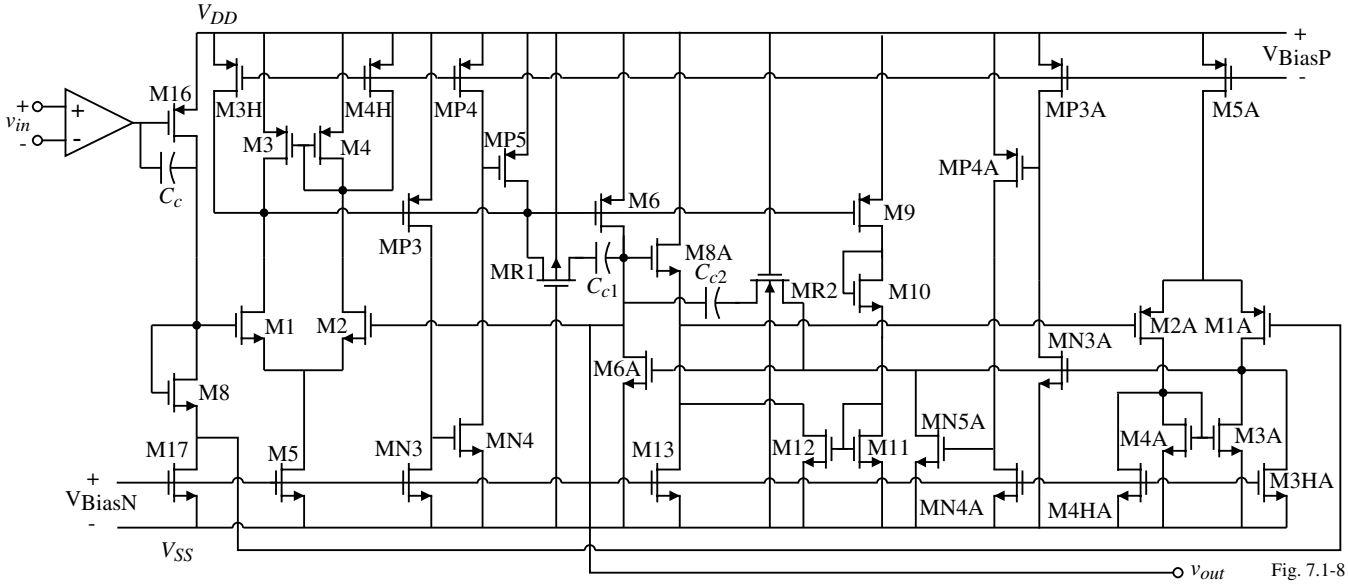


Fig. 7.1-8

Compensation:

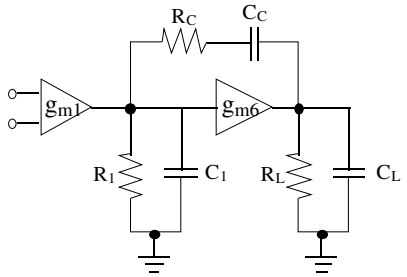
Uses nulling Miller compensation.

Short circuit protection:

MP3-MN3-MN4-MP4-MP5

MN3A-MP3A-MP4A-MN4A-MN5A

(max. output ±60mA)



Low Output Resistance Op Amp - Continued

Table 7.1-2 Performance Characteristics of the Low Output Resistance Op Amp:

Specification	Simulated Results	Measured Results
Power Dissipation	7.0 mW	5.0 mW
Open Loop Voltage Gain	82 dB	83 dB
Unity Gainbandwidth	500kHz	420 kHz
Input Offset Voltage	0.4 mV	1 mV
$PSRR^+(0)/PSRR^-(0)$	85 dB/104 dB	86 dB/106 dB
$PSRR^+(1kHz)/PSRR^-(1kHz)$	81 dB/98 dB	80 dB/98 dB
THD (V_{in} = 3.3V_{pp})		
R_L = 300Ω	0.03%	0.13%(1 kHz)
C_L = 1000pF	0.08%	0.32%(4 kHz)
THD (V_{in} = 4.0V_{pp})		
R_L = 15KΩ	0.05%	0.13%(1 kHz)
C_L = 200pF	0.16%	0.20%(4 kHz)
Settling Time (0.1%)	3 μs	<5 μs
Slew Rate	0.8 V/μs	0.6 V/μs
1/f Noise at 1kHz	-	130 nV/√Hz
Broadband Noise	-	49 nV/√Hz

$$R_{out} \approx \frac{r_{ds6} \| r_{ds6A}}{\text{Loop Gain}} \approx \frac{50\text{k}\Omega}{5000} = 10\Omega$$

Low-Output Resistance Op Amp - Continued

Component sizes for the low-resistance op amp:

Transistor/Capacitor	μm/μm or pF	Transistor/Capacitor	μm/μm or pF
M16	184/9	M8A	481/6
M17	66/12	M13	66/12
M8	184/6	M9	27/6
M1, M2	36/10	M10	6/22
M3, M4	194/6	M11	14/6
M3H, M4H	16/12	M12	140/6
M5	145/12	MP3	8/6
M6	2647/6	MN3	244/6
MRC	48/10	MP4	43/12
C_C	11.0	MN4	12/6
M1A, M2A	88/12	MP5	6/6
M3A, M4A	196/6	MN3A	6/6
M3HA, M4HA	10/12	MP3A	337/6
M5A	229/12	MN4A	24/12
M6A	2420/6	MP4A	20/12
C_F	10.0	MN5A	6/6

Simpler Implementation of Negative Feedback to Achieve Low Output Resistance

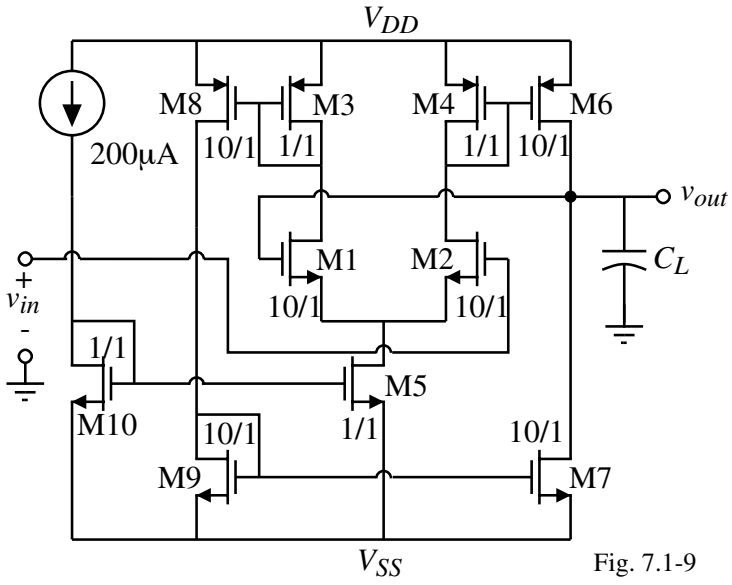


Fig. 7.1-9

Output Resistance:

$$R_{out} = \frac{R_o}{1+LG}$$

where

$$R_o = \frac{1}{g_{ds6}+g_{ds7}}$$

and

$$|LG| = \frac{g_{m2}}{2g_{m4}}(g_{m6}+g_{m7})R_o$$

Therefore, the output resistance is

$$R_{out} = \frac{1}{(g_{ds6}+g_{ds7})\left[1+\left(\frac{g_{m2}}{2g_{m4}}\right)(g_{m6}+g_{m7})R_o\right]}.$$

Example 7.1-1 - Low Output Resistance Using the Simple Shunt Negative Feedback Buffer

Find the output resistance of above op amp using the model parameters of Table 3.1-2.

Solution

The current flowing in the output transistors, M6 and M7, is 1mA which gives R_o of

$$R_o = \frac{1}{(\lambda_N+\lambda_P)1\text{mA}} = \frac{1000}{0.09} = 11.11\text{k}\Omega$$

To calculate the loop gain, we find that

$$g_{m2} = \sqrt{2K_N' \cdot 10 \cdot 100\mu\text{A}} = 469\mu\text{S}$$

$$g_{m4} = \sqrt{2K_P' \cdot 1 \cdot 100\mu\text{A}} = 100\mu\text{S}$$

and

$$g_{m6} = \sqrt{2K_P' \cdot 10 \cdot 1000\mu\text{A}} = 1\text{mS}$$

Therefore, the loop gain is

$$|LG| = \frac{469}{100}\ 12 \cdot 11.11 = 104.2$$

Solving for the output resistance, R_{out}, gives

$$R_{out} = \frac{11.11\text{k}\Omega}{1 + 104.2} = 106\Omega \quad \text{(Assumes that } R_L \text{ is large)}$$

BJTs Available in CMOS Technology

Illustration of an NPN substrate BJT available in a p-well CMOS technology:

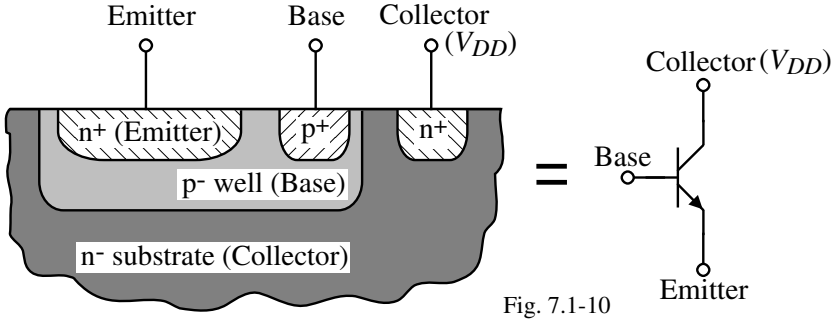


Fig. 7.1-10

Comments:

- g_m of the BJT is larger than the FET so that the output resistance w/o feedback is lower
- Can use the lateral or substrate BJT but since the collector is on ac ground, the substrate BJT is preferred
- Current is required to drive the BJT

Two-Stage Op Amp with a Class-A BJT Output Buffer Stage

Purpose of the M8-M9 source follower:

1.) Reduce the output resistance (includes whatever is seen from the base to ground divided by $1+\beta_F$)

2.) Reduces the output load at the drains of M6 and M7

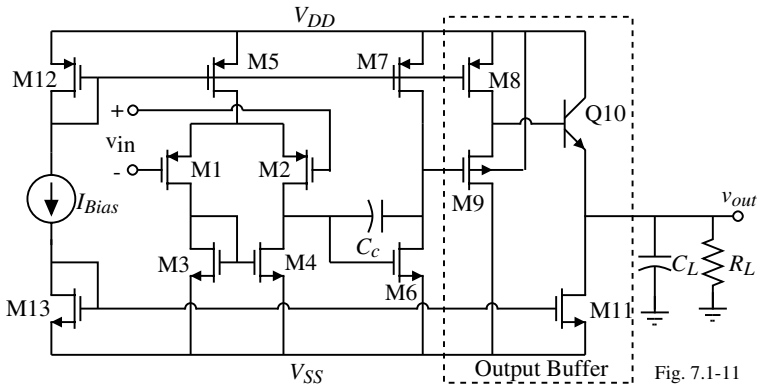


Fig. 7.1-11

Small-signal output resistance :

$$R_{out} \approx \frac{r_{\pi 10} + (1/g_{m9})}{1+\beta_F} = \frac{1}{g_{m10}} + \frac{1}{g_{m9}(1+\beta_F)}$$

$= 51.6\Omega + 6.7\Omega = 58.3\Omega$ where I_{10}=500μA, I_8=100μA, W_9/L_9=100 and β_F is 100

Maximum output voltage:

$$v_{OUT}(\max) = V_{DD} - V_{SD8}(\text{sat}) - v_{BE10} = V_{DD} - \sqrt{\frac{2K_P'}{I_8(W_8/L_8)}} - V_t \ln\left(\frac{I_{c10}}{I_{s10}}\right)$$

Voltage gain:

$$\frac{v_{out}}{v_{in}} = \left(\frac{g_{m1}}{g_{ds2}+g_{ds4}}\right)\left(\frac{g_{m6}}{g_{ds6}+g_{ds7}}\right)\left(\frac{g_{m9}}{g_{m9}+g_{mbs9}+g_{ds8}+g_{\pi 10}}\right)\left(\frac{g_{m10}R_L}{1+g_{m10}R_L}\right)$$

Compensation will be more complex because of the additional stages.

Example 7.1-2 - Designing the Class-A, Buffered Op Amp

Use the parameters of Table 3.1-2 along with the BJT parameters of $I_s = 10^{-14}$A and $\beta_F = 100$ to design the class-A, buffered op amp to give the following specifications. Assume the channel length is to be 1μm.

$V_{DD} = 2.5$V $V_{SS} = -2.5$V GB = 5MHz $A_{vd}(0) \geq 5000$V/V Slew rate ≥ 10V/μs

$R_L = 500\Omega$ $R_{out} \leq 100\Omega$ $C_L = 100$pF $ICMR = -1$V to 2V

Solution

Because the specifications above are similar to the two-stage design of Ex. 6.3-1, we can use these results for the first two stages of our design. However, we must convert the results of Ex. 6.3-1 to a PMOS input stage. The results of doing this give $W_1 = W_2 =$ 6μm, $W_3 = W_4 = 7$μm, $W_5 = 11$μm, $W_6 = 43$μm, and $W_7 = 34$μm.

BJT follower:

$SR = 10$V/μs and 100pF capacitor give $I_{11} = 1$mA.

$\therefore$ If $W_{13} = 44$μm, then $W_{11} = 44\text{μm}(1000\text{μA}/30\text{μA}) = 1467$μm.

$I_{11} = 1\text{mA} \Rightarrow 1/g_{m10} = 0.0258\text{V}/1\text{mA} = 25.8\Omega$

MOS follower:

To source 1mA, the BJT must provide 2mA which requires 20μA from the MOS follower. Therefore, select a bias current of 100μA for M8.

If $W_{12} = 44$μm, then $W_8 = 44\text{μm}(100\text{μA}/30\text{μA}) = 146$μm.

Example 7.1-2 - Continued

If $1/g_{m10}$ is 25.8Ω, then design g_{m9} as

$$g_{m9}=\frac{1}{(R_{out}-(1/g_{m10}))(1+\beta_F)}=\frac{1}{(100-25.8)(101)}=133.4\mu S \quad g_{m9} \text{ and } I_9 \Rightarrow W/L=0.809$$

Let us select W/L = 10 for M9 in order to make sure that the contribution of M9 to the output resistance is sufficiently small and to increase the gain closer to unity. This gives a transconductance of M9 of 469μS.

To calculate the voltage gain of the MOS follower we need to find g_{mbs9}.

$$\therefore \qquad g_{mbs9}=\frac{g_{m9}\gamma_N}{2\sqrt{2\phi_F+V_{BS9}}}=\frac{469\cdot 0.4}{2\sqrt{0.7+2}}=57.1\mu S$$

where we have assumed that the value of V_{SB9} is approximately 2V.

$$\therefore \qquad A_{MOS}=\frac{469\mu S}{469\mu S+57.1\mu S+4\mu S+5\mu S}=0.8765 \text{ V/V}.$$

The voltage gain of the BJT follower is

$$A_{BJT}=\frac{500}{25.8+500}=0.951 \text{ V/V}$$

Thus, the gain of the op amp is

$$A_{vd}(0)=(7777)(0.8765)(0.951)=6483 \text{ V/V}$$

The power dissipation of this amplifier is, $P_{diss.}=5V(1255\mu A)=6.27mW$

Two-Stage Op Amp with a Class-AB BJT Output Buffer Stage

This amplifier can reduce the quiescent power dissipation.

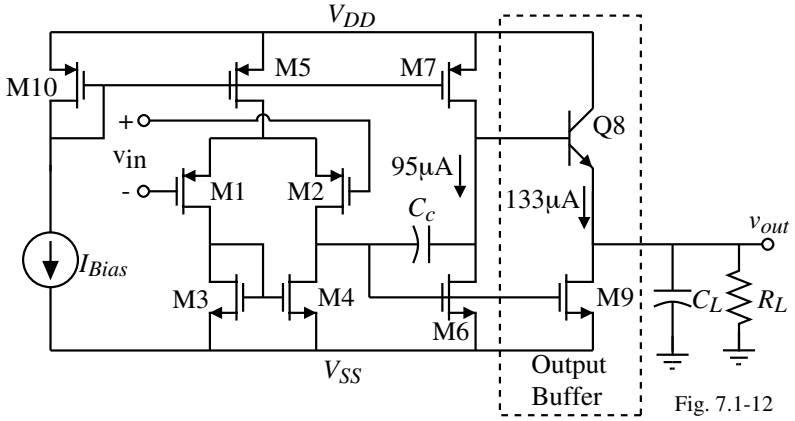


Fig. 7.1-12

Slew Rate:

$$SR^+=\frac{I_{OUT}^+}{C_L}=\frac{(1+\beta_F)I_7}{C_L} \qquad \text{and} \qquad SR^-=\frac{\beta_9(V_{DD}-1V+|V_{SS}|-V_{T0})^2}{2C_L}$$

If β_F = 100, C_L = 1000pF and I_7 = 95μA then SR^+ = 8.59V/μs.

Assuming a W_9/L_9 = 60 (I_9 = 133μA), ±2.5V power supplies and C_L = 1000pF gives SR^- = 35.9V/μs.

(The current is not limited by I_7 as it is for the positive slew rate.)

Two-Stage Op Amp with a Class-AB BJT Output Buffer Stage

Small-signal characteristics:

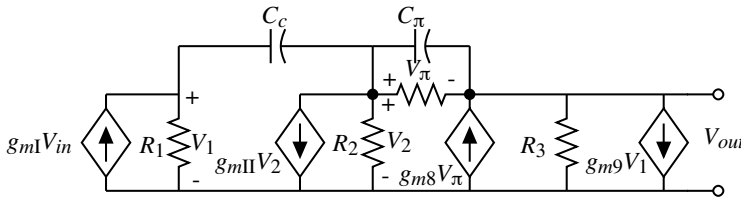


Fig. 7.1-13

Nodal equations:

$$g_{mI}V_{in} = (G_I + sC_c)V_1 - sC_cV_2 + 0V_{out}$$
$$0 = (g_{mII} - sC_c)V_1 + (G_{II} + g_\pi + sC_c + sC_\pi)V_2 - (g_\pi + sC_\pi)V_{out}$$
$$0 \cong g_{m9}V_1 - (g_{m13} + sC_\pi)V_2 + (g_{m13} + sC_\pi)V_{out} \qquad \text{where } g_\pi > G_3$$

The approximate voltage transfer function is:

$$\frac{V_9(s)}{V_{in}(s)} \approx A_{v0}\frac{((s/z_1) - 1)\,((s/z_2) - 1)}{((s/p_1) - 1)\,((s/p_2) - 1)}$$

where

$$A_{v0} = \frac{-g_{mI}g_{mII}}{G_IG_{II}} \qquad z_1 = \frac{1}{\dfrac{C_c}{g_{mII}} - \dfrac{C_\pi}{g_{m13}}\left[1 + \dfrac{g_{m9}}{g_{mII}}\right]} \qquad z_2 = -\frac{g_{m13}}{C_\pi} + \frac{g_{mII}}{C_c}\left[1 + \frac{g_{m9}}{g_{mII}}\right]$$

$$p_1 = \frac{-G_IG_{II}}{g_{mII}C_c}\left[1 + \frac{g_{m9}}{\beta_F g_{mII}} + \frac{C_\pi}{C_c}\left(\frac{G_IG_{II}}{g_{m13}g_{mII}}\right)\right]^{-1} \qquad p_2 \cong \frac{-g_{m13}g_{mII}}{(g_{mII} + g_{m9})C_\pi}$$

Two-Stage Op Amp with a Class-AB BJT Output Buffer Stage - Continued

Output stage current, I_{C8}:

$$I_{C8} = I_{D9} = \frac{S_9}{S_6}I_{D6} = \frac{60}{43}95\mu A = 133\mu A$$

Small-signal output resistance:

$$r_{out} = \frac{r_\pi + R_{II}}{1 + \beta_F} = \frac{19.668k\Omega + 116.96k\Omega}{101} = 1353\Omega$$

if $I_6 = I_7 = 95\mu A$, and $\beta_F = 100$.

Loading effect of R_L on the voltage transfer curve (increasing W_9/L_9 will improve the negative part of the cost of power dissipation):

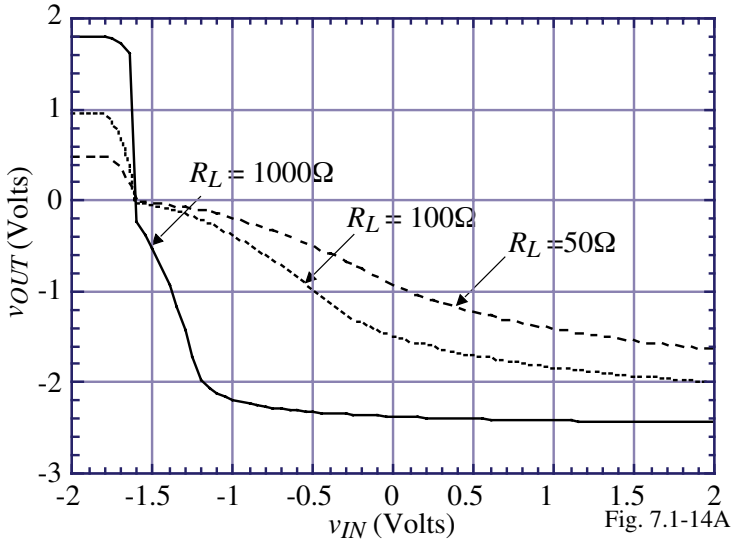


Fig. 7.1-14A

Example 7.1-3 - Performance of the Two-Stage, Class AB Output Buffer

Using the transistor currents given above for the output stages (output stage of the two-stage op amp and the buffer stage), find the small-signal output resistance and the maximum output voltage when R_L = 50Ω. Use the W/L values of Example 7.1-2 and assume that the NPN BJT has the parameters of β_F = 100 and I_S = 10fA.

Solution

It was shown on the previous slide that the small-signal output resistance is

$$r_{out} = \frac{r_\pi + r_{ds6} \| r_{ds7}}{1+\beta_F} = \frac{19.668\text{k}\Omega + 116.96\text{k}\Omega}{101} = 1353\Omega$$

Obviously, the MOS buffer of Fig. 7.1-11 would decrease this value.

The maximum output voltage is given above is only valid if the load current is small. If this is not the case, then a better approach is to assume that all of the current in M7 becomes base current for Q8. This base current is multiplied by $1+\beta_F$ to give the sourcing current. If M9 is off, then all this current flows through the load resistor to give an output voltage of

$$v_{OUT}(\text{max}) \approx (1+\beta_F) I_7 R_L$$

If the value of v_{OUT}(max) is close to V_{DD}, then the source-drain voltage across M7 may be too small to be in saturation causing I_7 to decrease. Using the above equation, we calculate v_{OUT}(max) as (101)·95μA·50Ω or 0.48V which is close to the simulation results shown using the parameters of Table 3.1-2.

SUMMARY

- A buffered op amp requires an output resistance between $10\Omega \le R_O \le 1000\Omega$
- Output resistance using MOSFETs only can be reduced by,
  - Source follower output ($1/g_m$)
  - Negative shunt feedback (frequency is a problem in this approach)
- Use of substrate (or lateral) BJT's can reduce the output resistance because g_m is larger than the g_m of a MOSFET
- Adding a buffer stage to lower the output resistance will most like complicate the compensation of the op amp

