LECTURE 300 – BUFFERED OP AMPS  
(READING: AH – 352-368)

Objective
The objective of this presentation is:
1.) Illustrate the method of lowering the output resistance of simple op amps
2.) Show examples

Outline
• Open-loop, MOSFET buffered op amps
• Closed-loop MOSFET buffered op amps
• BJT output op amps
• Summary

Goal
To illustrate the degrees of freedom and choices of different circuit architectures that can enhance the performance of a given op amp.

What is a Buffered Op Amp?
A buffered op amp is an op amp with a low value of output resistance, $R_O$.
Typically, $10\,\Omega \leq R_O \leq 1000\,\Omega$

Requirements
Generally the same as for the output amplifier:
• Low output resistance
• Large output signal swing
• Low distortion
• High efficiency

Types of Buffered Op Amps
• Buffered op amps using MOSFETs
  With and without negative feedback
• Buffered op amps using BJTs
Source-Follower, Push-Pull Output Op Amp

\[ R_{out} = \frac{1}{g_{m21} + g_{m22}} \leq 1000 \Omega, \ A_v(0) = 65 \text{dB} \ (I_{Bias}=50 \mu A), \ \text{and} \ GB = 60 \text{MHz for} \ C_L = 1 \text{pF} \]

Output bias current?

M18-M19-M21-M22 loop \[ \Rightarrow V_{SG18} + V_{GS19} = V_{SG21} + V_{GS22} \]

which gives \[ \sqrt{\frac{2I_{18}}{K_{PS18}}} + \sqrt{\frac{2I_{19}}{K_{NS19}}} = \sqrt{\frac{2I_{21}}{K_{PS21}}} + \sqrt{\frac{2I_{22}}{K_{NS22}}} \]

Crossover-Inverter, Buffer Stage Op Amp

Principle: If the buffer has high output resistance and voltage gain (common source), this is okay if when loaded by a small \( R_L \) the gain of this stage is approximately unity.

This op amp is capable of delivering 160mW to a 100\( \Omega \) load while only dissipating 7mW of quiescent power!
Crossover-Inverter, Buffer Stage Op Amp - Continued

How does the output buffer work?

The two inverters, M1-M3 and M2-M4 are designed to work over different regions of the buffer input voltage, $v_{in'}$.

Consider the idealized voltage transfer characteristic of the crossover inverters:

Crossover voltage $V_C = V_B - V_A \geq 0$

$V_C$ is designed to be small and positive for worst case variations in processing (Maximum value of $V_C \approx 110$ mV)

Performance Results for the Crossover-Inverter, Buffer Stage CMOS Op Amp

<table>
<thead>
<tr>
<th>Specification</th>
<th>Performance</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage</td>
<td>± 6 V</td>
</tr>
<tr>
<td>Quiescent Power</td>
<td>7 mW</td>
</tr>
<tr>
<td>Output Swing (100Ω Load)</td>
<td>8.1 Vpp</td>
</tr>
<tr>
<td>Open-Loop Gain (100Ω Load)</td>
<td>78.1 dB</td>
</tr>
<tr>
<td>Unity Gainbandwidth</td>
<td>260kHz</td>
</tr>
<tr>
<td>Voltage Spectral Noise Density at 1kHz</td>
<td>$1.7 \mu V/\sqrt{Hz}$</td>
</tr>
<tr>
<td>PSRR at 1kHz</td>
<td>55 dB</td>
</tr>
<tr>
<td>CMRR at 1kHz</td>
<td>42 dB</td>
</tr>
<tr>
<td>Input Offset Voltage (Typical)</td>
<td>10 mV</td>
</tr>
</tbody>
</table>
**Compensation of Op Amps with Output Amplifiers**

Compensation of a three-stage amplifier:

This op amp introduces a third pole, $p'_{3}$ (what about zeros?)

With no compensation,

$$\frac{V_{\text{out}}(s)}{V_{\text{in}}(s)} = \frac{-A_{\text{VO}}}{\left(\frac{s}{p'_{1}} - 1\right)\left(\frac{s}{p'_{2}} - 1\right)\left(\frac{s}{p'_{3}} - 1\right)}$$

Illustration of compensation choices:

Muller compensation applied around both the second and the third stage.

Muller compensation applied around the second stage only.

**Low Output Resistance Op Amp**

To get low output resistance using MOSFETs, negative feedback must be used.

Ideal implementation:

Comments:

- The output resistance will be equal to $r_{ds1}||r_{ds2}$ divided by the loop gain
- If the error amplifiers are not perfectly matched, the bias current in M1 and M2 is not defined
Low Output Resistance Op Amp - Continued

Offset correction circuitry:

The feedback circuitry of the two error amplifiers tries to insure that the voltages in the loop sum to zero. Without the M9-M12 feedback circuit, there is no way to adjust the output for any error in the loop. The circuit works as follows:

When $V_{OS}$ is positive, M6 tries to turn off and so does M6A. $I_{M9}$ reduces thus reducing $I_{M12}$. A reduction in $I_{M12}$ reduces $I_{M8A}$ thus decreasing $V_{GS8A}$. $V_{GS8A}$ ideally decreases by an amount equal to $V_{OS}$. A similar result holds for negative offsets and offsets in $E_{A2}$.

Low Output Resistance Op Amp - Continued

Error amplifiers:
Low Output Resistance Op Amp - Complete Schematic

Compensation:
Uses nulling Miller compensation.

Short circuit protection:
MP3-MN3-MN4-MP4-MP5
MN3A-MP3A-MP4A-MN4A-MN5A
(max. output ±60mA)

Table 7.1-2 Performance Characteristics of the Low Output Resistance Op Amp:

<table>
<thead>
<tr>
<th>Specification</th>
<th>Simulated Results</th>
<th>Measured Results</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power Dissipation</td>
<td>7.0 mW</td>
<td>5.0 mW</td>
</tr>
<tr>
<td>Open Loop Voltage Gain</td>
<td>82 dB</td>
<td>83 dB</td>
</tr>
<tr>
<td>Unity Gainbandwidth</td>
<td>500kHz</td>
<td>420 kHz</td>
</tr>
<tr>
<td>Input Offset Voltage</td>
<td>0.4 mV</td>
<td>1 mV</td>
</tr>
<tr>
<td>PSRR+(0)/PSRR-(0)</td>
<td>85 dB/104 dB</td>
<td>86 dB/106 dB</td>
</tr>
<tr>
<td>PSRR+(1kHz)/PSRR-(1kHz)</td>
<td>81 dB/98 dB</td>
<td>80 dB/98 dB</td>
</tr>
<tr>
<td>THD (Vin = 3.3Vpp)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>RL = 300Ω</td>
<td>0.03%</td>
<td>0.13%(1 kHz)</td>
</tr>
<tr>
<td>CL = 1000pF</td>
<td>0.08%</td>
<td>0.32%(4 kHz)</td>
</tr>
<tr>
<td>THD (Vin = 4.0Vpp)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>RL = 15KΩ</td>
<td>0.05%</td>
<td>0.13%(1 kHz)</td>
</tr>
<tr>
<td>CL = 200pF</td>
<td>0.16%</td>
<td>0.20%(4 kHz)</td>
</tr>
<tr>
<td>Settling Time (0.1%)</td>
<td>3 µs</td>
<td>&lt;5 µs</td>
</tr>
<tr>
<td>Slew Rate</td>
<td>0.8 V/µs</td>
<td>0.6 V/µs</td>
</tr>
<tr>
<td>1/f Noise at 1kHz</td>
<td>-</td>
<td>130 nV/√Hz</td>
</tr>
<tr>
<td>Broadband Noise</td>
<td>-</td>
<td>49 nV/√Hz</td>
</tr>
</tbody>
</table>

\[ R_{out} \approx \frac{r_{ds61}||r_{ds6A}}{\text{Loop Gain}} = \frac{50k\Omega}{5000} = 10\Omega \]
Low-Output Resistance Op Amp - Continued

Component sizes for the low-resistance op amp:

<table>
<thead>
<tr>
<th>Transistor/Capacitor</th>
<th>µm/µm or pF</th>
<th>Transistor/Capacitor</th>
<th>µm/µm or pF</th>
</tr>
</thead>
<tbody>
<tr>
<td>M16</td>
<td>184/9</td>
<td>M8A</td>
<td>481/6</td>
</tr>
<tr>
<td>M17</td>
<td>66/12</td>
<td>M13</td>
<td>66/12</td>
</tr>
<tr>
<td>M8</td>
<td>184/6</td>
<td>M9</td>
<td>27/6</td>
</tr>
<tr>
<td>M1, M2</td>
<td>36/10</td>
<td>M10</td>
<td>6/22</td>
</tr>
<tr>
<td>M3, M4</td>
<td>194/6</td>
<td>M11</td>
<td>14/6</td>
</tr>
<tr>
<td>M3H, M4H</td>
<td>16/12</td>
<td>M12</td>
<td>140/6</td>
</tr>
<tr>
<td>M5</td>
<td>145/12</td>
<td>MP3</td>
<td>8/6</td>
</tr>
<tr>
<td>M6</td>
<td>2647/6</td>
<td>MN3</td>
<td>244/6</td>
</tr>
<tr>
<td>MRC</td>
<td>48/10</td>
<td>MP4</td>
<td>43/12</td>
</tr>
<tr>
<td>CC</td>
<td>11.0</td>
<td>MN4</td>
<td>12/6</td>
</tr>
<tr>
<td>M1A, M2A</td>
<td>88/12</td>
<td>MP5</td>
<td>6/6</td>
</tr>
<tr>
<td>M3A, M4A</td>
<td>196/6</td>
<td>MN3A</td>
<td>6/6</td>
</tr>
<tr>
<td>M3HA, M4HA</td>
<td>10/12</td>
<td>MP3A</td>
<td>337/6</td>
</tr>
<tr>
<td>M5A</td>
<td>229/12</td>
<td>MN4A</td>
<td>24/12</td>
</tr>
<tr>
<td>M6A</td>
<td>2420/6</td>
<td>MP4A</td>
<td>20/12</td>
</tr>
<tr>
<td>C_F</td>
<td>10.0</td>
<td>MN5A</td>
<td>6/6</td>
</tr>
</tbody>
</table>

Simpler Implementation of Negative Feedback to Achieve Low Output Resistance

Output Resistance:

\[ R_{out} = \frac{R_o}{1 + |L_G|} \]

where

\[ R_o = \frac{1}{g_{ds6} + g_{ds7}} \]

and

\[ |L_G| = \frac{g_m^2}{2g_m^4(g_m6 + g_m7)R_o} \]

Therefore, the output resistance is

\[ R_{out} = \frac{1}{(g_{ds6} + g_{ds7}) \left[ 1 + \frac{g_m^2}{2g_m^4(g_m6 + g_m7)R_o} \right]} \]
Example 7.1-1 - Low Output Resistance Using the Simple Shunt Negative Feedback Buffer

Find the output resistance of above op amp using the model parameters of Table 3.1-2.

**Solution**

The current flowing in the output transistors, M6 and M7, is 1mA which gives \( R_o \) of

\[
R_o = \frac{1}{(\lambda_N + \lambda_P)1mA} = \frac{1000}{0.09} = 11.11k\Omega
\]

To calculate the loop gain, we find that

\[
\begin{align*}
g_m2 &= \sqrt{2K_N' \cdot 10 \cdot 100\mu A} = 469\mu S \\
g_m4 &= \sqrt{2K_P' \cdot 1 \cdot 100\mu A} = 100\mu S
\end{align*}
\]

and

\[
g_m6 = \sqrt{2K_P' \cdot 10 \cdot 1000\mu A} = 1mS
\]

Therefore, the loop gain is

\[
|LG| = \frac{469}{100} \cdot 12 \cdot 11.11 = 104.2
\]

Solving for the output resistance, \( R_{out} \), gives

\[
R_{out} = \frac{11.11k\Omega}{1 + 104.2} = 106\Omega \quad \text{(Assumes that} \ R_L \text{is large)}
\]

BJTs Available in CMOS Technology

Illustration of an NPN substrate BJT available in a p-well CMOS technology:

Comments:

• \( g_m \) of the BJT is larger than the FET so that the output resistance w/o feedback is lower
• Can use the lateral or substrate BJT but since the collector is on ac ground, the substrate BJT is preferred
• Current is required to drive the BJT
Two-Stage Op Amp with a Class-A BJT Output Buffer Stage

Purpose of the M8-M9 source follower:
1.) Reduce the output resistance (includes whatever is seen from the base to ground divided by $1+\beta_F$)
2.) Reduces the output load at the drains of M6 and M7

Small-signal output resistance:

$$R_{out} = r_{\pi 10} + \frac{1}{gm9} + \frac{1}{gm9(1+\beta_F)}$$

$$= 51.6\Omega + 6.7\Omega = 58.3\Omega$$

where $I_{10}=500\mu A$, $I_8=100\mu A$, $W_9/L_9=100$ and $\beta_F$ is 100

Maximum output voltage:

$$v_{OUT(max)} = V_{DD} - V_{SDS8(sat)} - v_{BE10} = V_{DD} - \sqrt{\frac{2K_p'}{I_8(W_8/L_8)}} - V_i \ln \left( \frac{I_{c10}}{I_{s10}} \right)$$

Voltage gain:

$$\frac{v_{out}}{v_{in}} = \left( g_{m1} + g_{m6} \left( g_{ds2} + g_{ds4} \right) + g_{m9} + g_{mbs9} + g_{ds8} + g_{\pi 10} + \frac{g_{m10}R_L}{1+g_{m10}R_L} \right)$$

Compensation will be more complex because of the additional stages.

Example 7.1-2 - Designing the Class-A, Buffered Op Amp

Use the parameters of Table 3.1-2 along with the BJT parameters of $I_s = 10^{-14}A$ and $\beta_F = 100$ to design the class-A, buffered op amp to give the following specifications.

Assume the channel length is to be 1µm.

$V_{DD} = 2.5V$  $V_{SS} = -2.5V$  $GB = 5MHz$  $A_{vdf}(0) \geq 5000V/V$  $Slew rate \geq 10V/\mu s$

$R_L = 500\Omega$  $R_{out} \leq 100\Omega$  $C_L = 100pF$  $ICMR = -1V$ to $2V$

**Solution**

Because the specifications above are similar to the two-stage design of Ex. 6.3-1, we can use these results for the first two stages of our design. However, we must convert the results of Ex. 6.3-1 to a PMOS input stage. The results of doing this give $W_1 = W_2 = 6\mu m$, $W_3 = W_4 = 7\mu m$, $W_5 = 11\mu m$, $W_6 = 43\mu m$, and $W_7 = 34\mu m$.

BJT follower:

$sR = 10V/\mu s$ and 100pF capacitor give $I_{11} = 1mA$.

If $W_1 = 44\mu m$, then $W_{11} = 44\mu m(1000\mu A/30\mu A) = 1467\mu m$.

$I_{11} = 1mA \Rightarrow 1/gm10 = 0.0258V/1mA = 25.8\Omega$

MOS follower:

To source 1mA, the BJT must provide 2mA which requires 20µA from the MOS follower. Therefore, select a bias current of 100µA for M8.

If $W_1 = 44\mu m$, then $W_8 = 44\mu m(100\mu A/30\mu A) = 146\mu m$. 

\[\]
**Example 7.1-2 - Continued**

If $1/g_{m10}$ is 25.8Ω, then design $g_{m9}$ as

$$g_{m9} = \frac{1}{R_{out} - (1/g_{m10})(1+\beta_{F})} = \frac{1}{(100-25.8)(101)} = 133.4\mu S$$

$g_{m9}$ and $I_9 \Rightarrow W/L = 0.809$

Let us select $W/L = 10$ for M9 in order to make sure that the contribution of M9 to the output resistance is sufficiently small and to increase the gain closer to unity. This gives a transconductance of M9 of 469µS.

To calculate the voltage gain of the MOS follower we need to find $g_{mbs9}$.

$$\therefore \quad g_{mbs9} = \frac{g_{m9}\gamma_{N}}{2\sqrt{2\phi_{F} + V_{BS9}}} = \frac{469\cdot0.4}{2\sqrt{0.7+2}} = 57.1\mu S$$

where we have assumed that the value of $V_{SB9}$ is approximately 2V.

$$\therefore \quad A_{MOS} = \frac{469\mu S + 57.1\mu S + 4\mu S + 5\mu S}{2} = 0.8765 \text{ V/V}.$$  

The voltage gain of the BJT follower is

$$A_{BJT} = \frac{500}{25.8+500} = 0.951 \text{ V/V}.$$  

Thus, the gain of the op amp is

$$A_{vd}(0) = (7777)(0.8765)(0.951) = 6483 \text{ V/V}.$$  

The power dissipation of this amplifier is, $P_{diss.} = 5V(1255\mu A) = 6.27mW$

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**Two-Stage Op Amp with a Class-AB BJT Output Buffer Stage**

This amplifier can reduce the quiescent power dissipation.

Slew Rate:

$$SR^+ = \frac{I^{+}_{OUT}}{C_L} = \frac{(1 + \beta_{F})I_7}{C_L} \quad \text{and} \quad SR^- = \frac{\beta_{9}(V_{DD} - 1V + |V_{SS}\rangle - V_{TB})^2}{2C_L}$$

If $\beta_{F} = 100$, $C_L = 1000pF$ and $I_7 = 95\mu A$ then $SR^+ = 8.59V/\mu s$.

Assuming a $W_9/L_9 = 60$ ($I_9 = 133\mu A$), ±2.5V power supplies and $C_L = 1000pF$ gives $SR^- = 35.9V/\mu s$.

(The current is not limited by $I_7$ as it is for the positive slew rate.)
Two-Stage Op Amp with a Class-AB BJT Output Buffer Stage

Small-signal characteristics:

Nodal equations:

\[
g_{m1}v_{in} = (G_I + sC_c)V_1 - sC_cV_2 + V_{out}
\]

\[
0 = (g_{mII} - sC_c)V_1 + (G_{II} + g_{\pi} + sC_c + sC_{\pi})V_2 - (g_{\pi} + sC_{\pi})V_{out}
\]

\[
0 \cong g_{m9}V_1 - (g_{m13} + sC_{\pi})V_2 + (g_{m13} + sC_{\pi})V_{out} \quad \text{where} \quad g_{\pi} > G_3
\]

The approximate voltage transfer function is:

\[
\frac{V_9(s)}{V_{in}(s)} \approx \frac{A_{v0}(s)}{(s/z_1 - 1)(s/z_2 - 1)}
\]

where

\[
A_{v0} = \frac{-g_{mll}g_{mll}}{G_I G_{II}}
\]

\[
z_1 = \frac{1}{G_{II}C_c - C_{\pi} \left[ 1 + \frac{g_{m9}}{g_{mll}} \right]}
\]

\[
z_2 = -\frac{g_{mll}g_{mll}C_c}{C_{\pi} \left[ 1 + \frac{g_{m9}}{g_{mll}} \right]}
\]

\[
p_1 = \frac{-G_I G_{II}}{g_{mll}C_c} \left[ 1 + \frac{g_{m9}}{g_{mll}} + \frac{C_{\pi}}{C_c} \left[ \frac{G_I G_{II}}{g_{mll}g_{mll}} \right] \right]^{-1}
\]

\[
p_2 \cong \frac{-g_{mll}g_{mll}}{(g_{mll} + g_{m9})C_{\pi}}
\]

Two-Stage Op Amp with a Class-AB BJT Output Buffer Stage - Continued

Output stage current, \( I_{C8} \):

\[
I_{C8} = I_{D9} = \frac{S_9}{S_9} I_{D6} = \frac{60}{43} \times 95 \mu A = 133 \mu A
\]

Small-signal output resistance:

\[
r_{out} = \frac{r_{\pi} + R_{ll}}{1 + \beta_F} = \frac{19.668k\Omega + 116.96k\Omega}{101} = 1353 \Omega
\]

if \( I_6 = I_7 = 95 \mu A \), and \( \beta_F = 100 \).

Loading effect of \( R_L \) on the voltage transfer curve (increasing \( W_9/L_9 \) will improve the negative part at the cost of power dissipation):
Example 7.1-3 - Performance of the Two-Stage, Class AB Output Buffer

Using the transistor currents given above for the output stages (output stage of the two-stage op amp and the buffer stage), find the small-signal output resistance and the maximum output voltage when $R_L = 50\,\Omega$. Use the W/L values of Example 7.1-2 and assume that the NPN BJT has the parameters of $\beta_F = 100$ and $I_S = 10\,fA$.

Solution

It was shown on the previous slide that the small-signal output resistance is

$$r_{out} = \frac{r_{\pi} + r_{ds6}||r_{ds7}}{1+\beta_F} = \frac{19.668\,k\Omega + 116.96\,k\Omega}{101} = 1353\,\Omega$$

Obviously, the MOS buffer of Fig. 7.1-11 would decrease this value.

The maximum output voltage is given above is only valid if the load current is small. If this is not the case, then a better approach is to assume that all of the current in M7 becomes base current for Q8. This base current is multiplied by $1+\beta_F$ to give the sourcing current. If M9 is off, then all this current flows through the load resistor to give an output voltage of

$$v_{OUT}(max) \approx (1+\beta_F)I_7R_L$$

If the value of $v_{OUT}(max)$ is close to $V_{DD}$, then the source-drain voltage across M7 may be too small to be in saturation causing $I_7$ to decrease. Using the above equation, we calculate $v_{OUT}(max)$ as $(101)\cdot95\mu A\cdot50\,\Omega$ or 0.48V which is close to the simulation results shown using the parameters of Table 3.1-2.

SUMMARY

- A buffered op amp requires an output resistance between $10\,\Omega \leq R_O \leq 1000\,\Omega$
- Output resistance using MOSFETs only can be reduced by,
  - Source follower output ($1/g_m$)
  - Negative shunt feedback (frequency is a problem in this approach)
- Use of substrate (or lateral) BJT’s can reduce the output resistance because $g_m$ is larger than the $g_m$ of a MOSFET
- Adding a buffer stage to lower the output resistance will most like complicate the compensation of the op amp