LECTURE 340 – LOW NOISE OP AMPS
(READING: AH – 402-414, GHLM – 788-798)

Objective

The objective of this presentation is:

1.) Review the principles of low noise design

2.) Show how to reduce the noise of op amps

Outline

- Review of noise analysis
- Low noise op amps
- Low noise op amps using lateral BJTs
- Low noise op amps using doubly correlated sampling
- Summary

Introduction

Why do we need low noise op amps?

Dynamic range:

Signal-to-noise ratio (*SNR*)

$$= \frac{\text{Maximum RMS Signal}}{\text{Noise}}$$

(*SNDR* includes both noise and distortion)

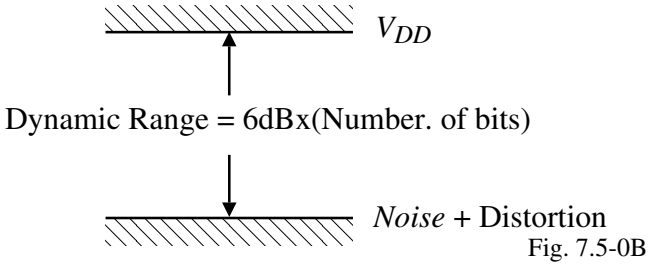


Fig. 7.5-0B

Consider a 14 bit digital-to-analog converter with a 1V reference with a bandwidth of 1MHz.

Maximum RMS signal is $\frac{0.5\text{V}}{\sqrt{2}} = 0.3535$ Vrms

A 14 bit D/A converter requires 14x6dB dynamic range or 84 dB or 16,400.

$\therefore$ The value of the least significant bit (*LSB*) $= \frac{0.3535}{16{,}400} = 21.6\mu\text{Vrms}$

If the equivalent input noise of the op amp is not less than this value, then the *LSB* cannot be resolved and the D/A converter will be in error. An op amp with an equivalent input-noise spectral density of $10\text{nV}/\sqrt{\text{Hz}}$ will have an rms noise voltage of approximately $(10\text{nV}/\sqrt{\text{Hz}})(1000\sqrt{\text{Hz}}) = 10\mu\text{Vrms}$ in a 1MHz bandwidth.

Transistor Noise Sources (Low-Frequency)

Drain current model:

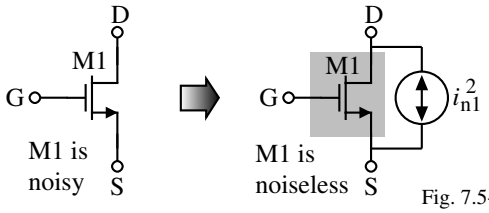


Fig. 7.5-0A

$$i_n^2 = \left[\frac{8kTg_m}{3} + \frac{(KF)I_D}{fC_{ox}L^2}\right] \quad \text{or} \quad i_n^2 = \left[\frac{8kTg_m(1+\eta)}{3} + \frac{(KF)I_D}{fC_{ox}L^2}\right] \text{ if } v_{BS} \neq 0$$

Recall that $\eta = \dfrac{g_m}{g_{mbs}}$

Gate voltage model assuming common source operation:

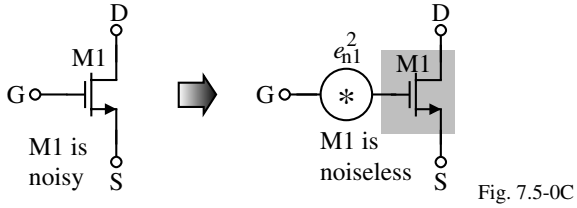


Fig. 7.5-0C

$$e_n^2 = \frac{\overline{i}_N^2}{g_m^2} = \left[\frac{8kT}{3g_m} + \frac{KF}{2fC_{ox}WLK'}\right] \quad \text{or} \quad e_n^2 = \left[\frac{8kT(1+\eta)}{3g_m} + \frac{KF}{2fC_{ox}WLK'}\right] \text{ if } v_{BS} \neq 0$$

Minimization of Noise in Op Amps

1.) Maximize the signal gain as close to the input as possible. (As a consequence, only the input stage will contribute to the noise of the op amp.)

2.) To minimize the 1/f noise:

   a.) Use PMOS input transistors with appropriately selected dc currents and W and L values.

   b.) Use lateral BJTs to eliminate the $1/f$ noise.

   c.) Use chopper stabilization to reduce the low-frequency noise.

Noise Analysis

1.) Insert a noise generator for each transistor that contributes to the noise. (Generally ignore the current source transistor of source-coupled pairs.)

2.) Find the output noise voltage across an open-circuit or output noise current into a short circuit.

3.) Reflect the total output noise back to the input resulting in the equivalent input noise voltage.

A Low-Noise, Two-Stage, Miller Op Amp

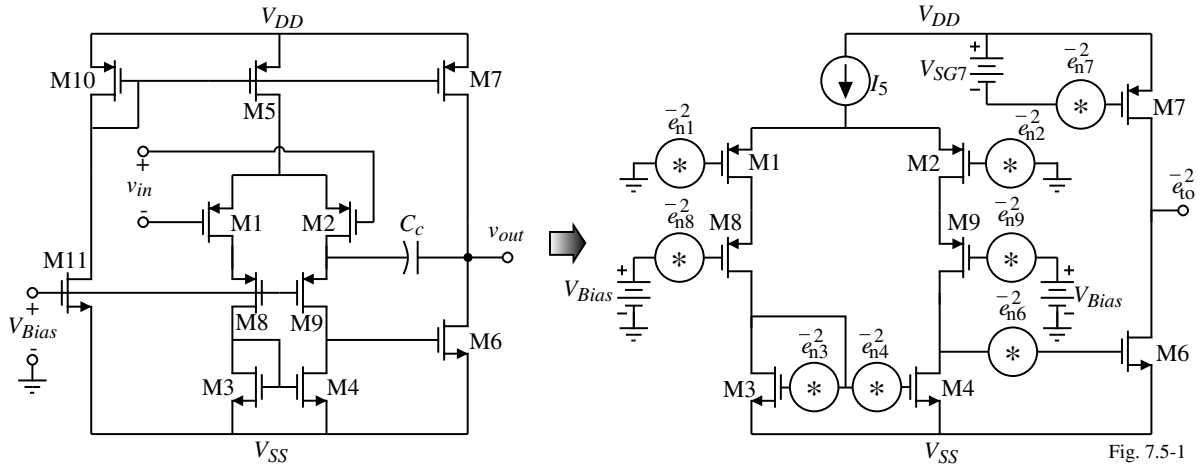


Fig. 7.5-1

The total output-noise voltage spectral density, e_{to}^2, is as follows where $g_{m8}(\text{eff}) \approx 1/r_{ds1}$,

$$e_{to}^2 = g_{m6}^2 R_{II}^2 \left[e_{n6}^2 + e_{n7}^2 + R_I^2 \left(g_{m1}^2 e_{n1}^2 + g_{m2}^2 e_{n2}^2 + g_{m3}^2 e_{n3}^2 + g_{m4}^2 e_{n4}^2 + (e_{n8}^2 / r_{ds1}^2) + (e_{n9}^2 / r_{ds2}^2) \right) \right]$$

Divide by $(g_{m1} R_I g_{m6} R_{II})^2$ to get the eq. input-noise voltage spectral density, e_{eq}^2, as

$$e_{eq}^2 = \frac{e_{to}^2}{(g_{m1} g_{m6} R_I R_{II})^2} = \frac{2e_{n6}^2}{g_{m1}^2 R_I^2} + 2e_{n1}^2 \left[1 + \left(\frac{g_{m3}}{g_{m1}} \right)^2 \left(\frac{e_{n3}^2}{e_{n1}^2} \right) + \frac{e_{n8}^2}{g_{m1}^2 r_{ds1}^2 e_{n1}^2} \right] \approx 2e_{n1}^2 \left[1 + \left(\frac{g_{m3}}{g_{m1}} \right)^2 \left(\frac{e_{n3}^2}{e_{n1}^2} \right) \right]$$

where $e_{n6}^2 = e_{n7}^2$, $e_{n3}^2 = e_{n4}^2$, $e_{n1}^2 = e_{n2}^2$ and $e_{n8}^2 = e_{n9}^2$ and $g_{m1} R_I$ is large.

1/*f* Noise of a Two-Stage, Miller Op Amp

Consider the 1/*f* noise:

Therefore the noise generators are replaced by,

$$e_{ni}^2 = \frac{B}{f W_i L_i} \quad (\text{V}^2/\text{Hz}) \qquad \text{and} \qquad i_{ni}^2 = \frac{2BK'I_i}{f L_i^2} \quad (\text{A}^2/\text{Hz})$$

Therefore, the approximate equivalent input-noise voltage spectral density is,

$$e_{eq}^2 = 2e_{n1}^2 \left[1 + \left(\frac{K_N' B_N}{K_P' B_P} \right) \left(\frac{L_1}{L_3} \right)^2 \right] \quad (\text{V}^2/\text{Hz})$$

Comments;

- Because we have selected PMOS input transistors, e_{n1}^2 has been minimized if we choose $W_1 L_1$ ($W_2 L_2$) large.
- Make $L_1 << L_3$ to remove the influence of the second term in the brackets.

Thermal Noise of a Two-Stage, Miller Op Amp

Let us focus next on the thermal noise:

The noise generators are replaced by,

$$e_{ni}^2 \approx \frac{8kT}{3g_m} \quad (\text{V}^2/\text{Hz}) \qquad \text{and} \qquad i_{ni}^2 \approx \frac{8kTg_m}{3} \quad (\text{A}^2/\text{Hz})$$

where the influence of the bulk has been ignored.

The approximate equivalent input-noise voltage spectral density is,

$$e_{eq}^2 = 2e_{n1}^2\left[1+\left(\frac{g_{m3}}{g_{m1}}\right)^2\left(\frac{e_{n3}^2}{e_{n1}^2}\right)\right] = 2e_{n1}^2\left[1+\sqrt{\frac{K_N W_3 L_1}{K_P W_1 L_3}}\right] (\text{V}^2/\text{Hz})$$

Comments:

- The choices that reduce the 1/*f* noise also reduce the thermal noise.

Noise Corner:

Equating the equivalent input-noise voltage spectral density for the 1/*f* noise and the thermal noise gives the noise corner, f_c, as

$$f_c = \frac{3g_m B}{8kTWL}$$

Example 7.5-1 Design of A Two-Stage, Miller Op Amp for Low 1/*f* Noise

Use the parameters of Table 3.1-2 along with the value of $KF = 4\text{x}10^{-28}$ F·A for NMOS and $0.5\text{x}10^{-28}$ F·A for PMOS and design the previous op amp to minimize the 1/f noise. Calculate the corresponding thermal noise and solve for the noise corner frequency. From this information, estimate the rms noise in a frequency range of 1Hz to 100kHz. What is the dynamic range of this op amp if the maximum signal is a 1V peak-to-peak sinusoid?

Solution

1.) The 1/f noise constants, B_N and B_P are calculated as follows.

$$B_N = \frac{KF}{2C_{ox}K_N'} = \frac{4\text{x}10^{-28}\text{F}\cdot\text{A}}{2\cdot 24.7\text{x}10^{-4}\text{F/m}^2\cdot 110\text{x}10^{-6}\text{A}^2/\text{V}} = 7.36\text{x}10^{-22}\,(\text{V}\cdot\text{m})^2$$

and

$$B_P = \frac{KF}{2C_{ox}K_P'} = \frac{0.5\text{x}10^{-28}\text{F}\cdot\text{A}}{2\cdot 24.7\text{x}10^{-4}\text{F/m}^2\cdot 50\text{x}10^{-6}\text{A}^2/\text{V}} = 2.02\text{x}10^{-22}\,(\text{V}\cdot\text{m})^2$$

2.) Now select the geometry of the various transistors that influence the noise performance.

To keep e_{n1}^2 small, let $W_1 = 100\mu\text{m}$ and $L_1 = 1\mu\text{m}$. Select $W_3 = 100\mu\text{m}$ and $L_3 = 20\mu\text{m}$ and let W_8 and L_8 be the same as W_1 and L_1 since they little influence on the noise.

Example 7.5-1 - Continued

Of course, M1 is matched with M2, M3 with M4, and M8 with M9.

$$\therefore \quad e_{n1}^2 = \frac{B_P}{fW_1L_1} = \frac{2.02\text{x}10^{-22}}{f\cdot 100\mu\text{m}\cdot 1\mu\text{m}} = \frac{2.02\text{x}10^{-12}}{f} \ (\text{V}^2/\text{Hz})$$

$$e_{eq}^2 = 2\text{x}\frac{2.02\text{x}10^{-12}}{f}\left[1+\left(\frac{110\cdot 7.36}{50\cdot 2.02}\right)^2\left(\frac{1}{20}\right)^2\right] = \frac{4.04\text{x}10^{-12}}{f}1.1606 = \frac{4.689\text{x}10^{-12}}{f}\ (\text{V}^2/\text{Hz})$$

Note at 100Hz, the voltage noise in a 1Hz band is $\approx 4.7\text{x}10^{-14}\text{V}^2$(rms) or 0.216μV(rms).

3.) The thermal noise at room temperature is

$$e_{n1}^2 = \frac{8kT}{3g_m} = \frac{8\cdot 1.38\text{x}10^{-23}\cdot 300}{3\cdot 707\text{x}10^{-6}} = 1.562\text{x}10^{-17}\ (\text{V}^2/\text{Hz})$$

which gives

$$e_{eq}^2 = 2\cdot 1.562\text{x}10^{-17}\left[1+\sqrt{\frac{110\cdot 100\cdot 1}{50\cdot 100\cdot 20}}\right] = 3.124\text{x}10^{-17}\cdot 1.33 = 4.164\text{x}10^{-17}\ (\text{V}^2/\text{Hz})$$

4.) The noise corner frequency is found by equating the two expressions for e_{eq}^2 to get

$$f_c = \frac{4.689\text{x}10^{-12}}{4.164\text{x}10^{-17}} = 112.6\text{kHz}$$

This noise corner is indicative of the fact that the thermal noise is much less than the 1/f noise.

Example 7.5-1 - Continued

5.) To estimate the rms noise in the bandwidth from 1Hz to 100,000Hz, we will ignore the thermal noise and consider only the 1/f noise. Performing the integration gives

$$V_{eq}(\text{rms})^2 = \int_1^{10^5}\frac{4.689\text{x}10^{-12}}{f}df = 4.689\text{x}10^{-12}[ln(100{,}000) - ln(1)]$$

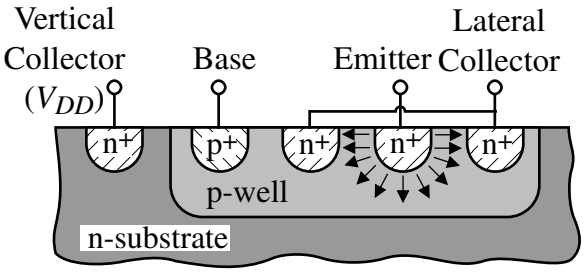
$$= 0.540\text{x}10^{-10}\ \text{Vrms}^2 = 7.34\ \mu\text{Vrms}$$

The maximum signal in rms is 0.353V. Dividing this by 7.34μV gives 48,044 or 93.6dB which is equivalent to about 15 bits of resolution.

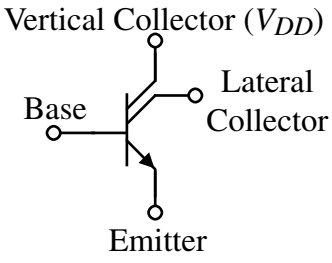
6.) Note that the design of the remainder of the op amp will have little influence on the noise and is not included in this example.

Lateral BJT

Since the 1/*f* noise is associated with current flowing at the surface of the channel, the lateral BJT offers a lower 1/*f* noise input device because the majority of current flows beneath the surface.



Cross-section of a NPN lateral BJT.



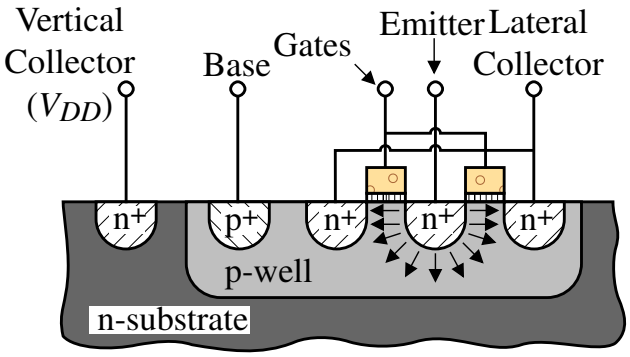
Symbol. Fig. 7.5-3

Comments:

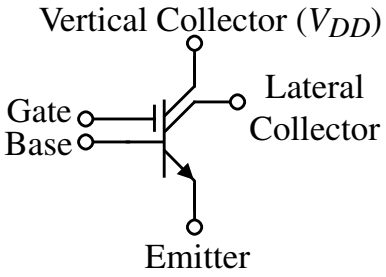
- Base of the BJT is the well
- Two collectors-one horizontal (desired) and one vertical (undesired)
- Collector efficiency is defined as $\frac{\text{Lateral collector current}}{\text{Total collector current}}$ and is 60-70%
- Reverse biased collector-base acts like a photodetector and is often used for light-sensing purposes

Field-Aided Lateral BJT

Polysilicon gates are used to ensure that the region beneath the gate does not invert forcing all current flow away from the surface and further eliminating the 1/*f* noise.



Cross-section of a field-aided NPN lateral BJT.



Symbol. Fig. 7.5-4

Physical Layout of a Lateral PNP Transistor

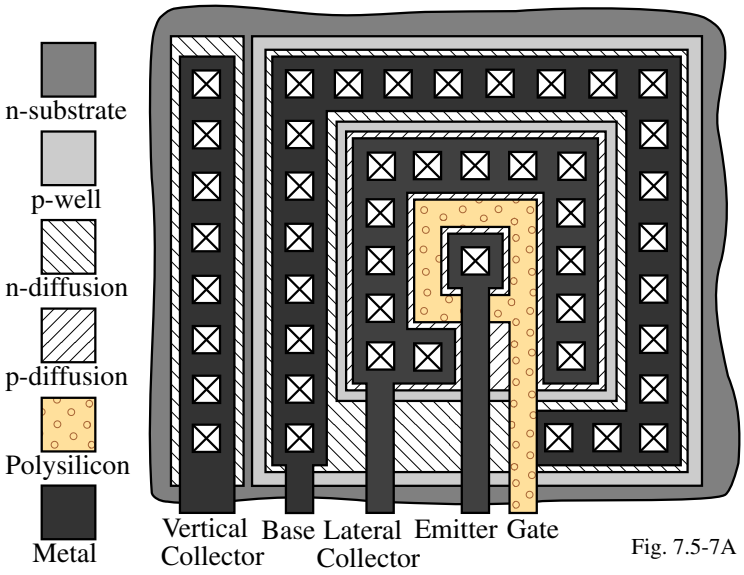


Fig. 7.5-7A

Experimental Results for a x40 PNP lateral BJT:

Characteristic	Value
Transistor area	$0.006mm^2$
Lateral β	90
Lateral efficiency	70%
Base resistance	150Ω
e_n at 5 Hz	$2.46nV/\sqrt{Hz}$
e_n at midband	$1.92nV/\sqrt{Hz}$
$f_c(e_n)$	3.2Hz
i_n at 5 Hz	$3.53pA/\sqrt{Hz}$
i_n at midband	$0.61pA/\sqrt{Hz}$
$f_c(i_n)$	162 Hz
f_T	85 MHz
Early voltage	16V
1.2μm CMOS with n-well	

Generally, the above structure is made as small as possible and then paralleled with identical geometries to achieve the desired BJT.

Low-Noise Op Amp using Lateral BJT's at the Input

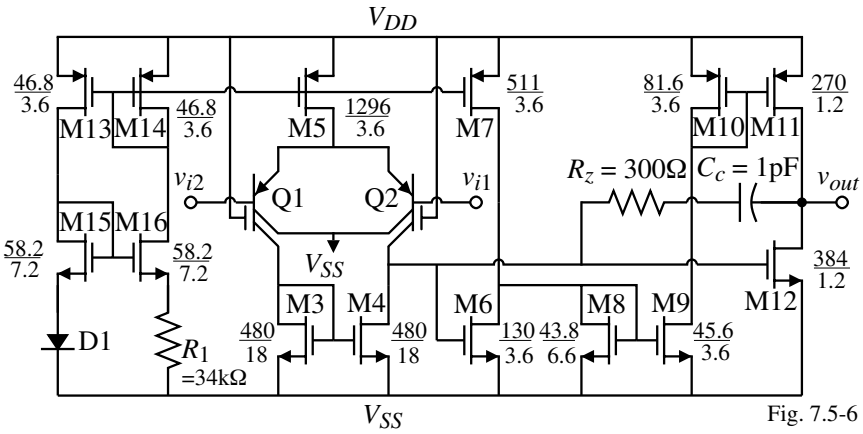


Fig. 7.5-6

Experimental noise performance:

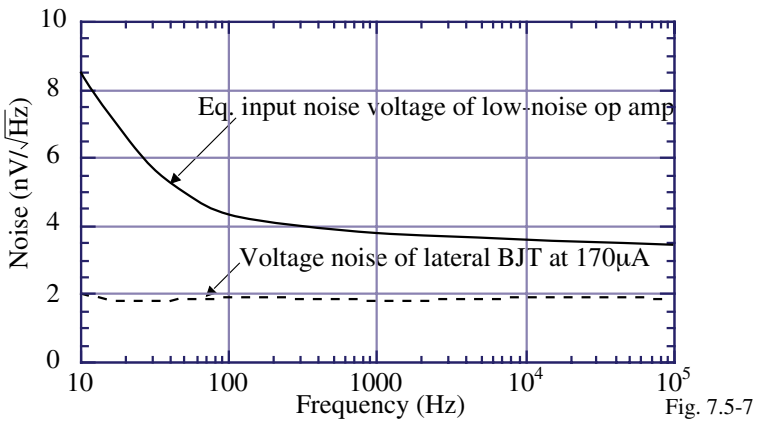


Fig. 7.5-7

Summary of Experimental Performance for the Low-Noise Op Amp

Experimental Performance	Value
Circuit area (1.2μm)	0.211 mm^2
Supply Voltages	±2.5 V
Quiescent Current	2.1 mA
-3dB frequency (at a gain of 20.8 dB)	11.1 MHz
e_n at 1Hz	23.8 nV/$\sqrt{\text{Hz}}$
e_n (midband)	3.2 nV/$\sqrt{\text{Hz}}$
$f_c(e_n)$	55 Hz
i_n at 1Hz	5.2 pA/$\sqrt{\text{Hz}}$
i_n (midband)	0.73 pA/$\sqrt{\text{Hz}}$
$f_c(i_n)$	50 Hz
Input bias current	1.68 μA
Input offset current	14.0 nA
Input offset voltage	1.0 mV
CMRR(DC)	99.6 dB
PSRR$^+$(DC)	67.6 dB
PSRR$^-$(DC)	73.9 dB
Positive slew rate (60 pF, 10 kΩ load)	39.0 V/μS
Negative slew rate (60 pF, 10 kΩ load)	42.5 V/μS

Chopper-Stabilized Op Amps - Doubly Correlated Sampling (DCS)

Illustration of the use of chopper stabilization to remove the undesired signal, v_u, form the desired signal, v_{in}.

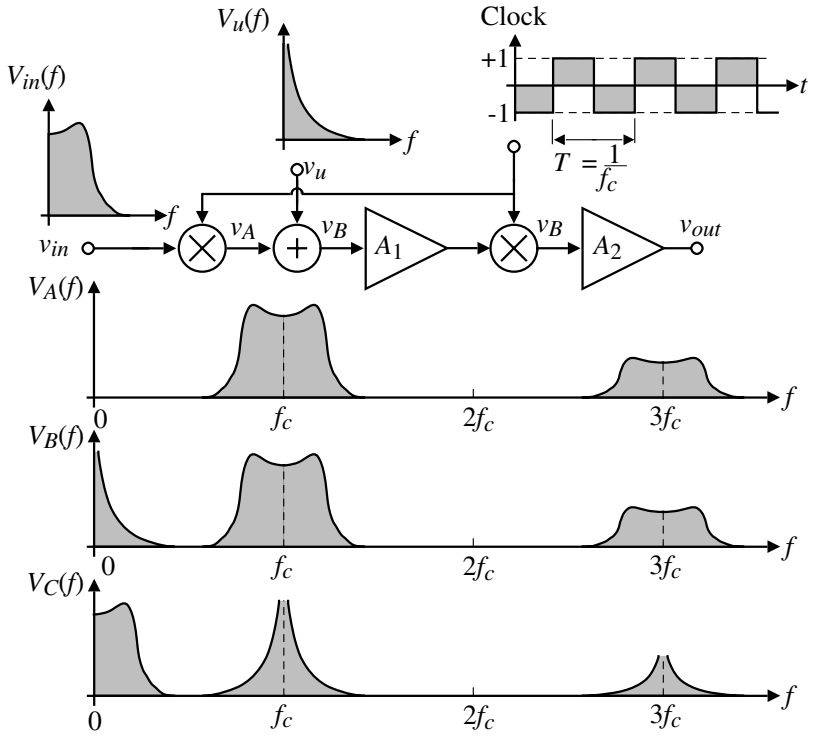
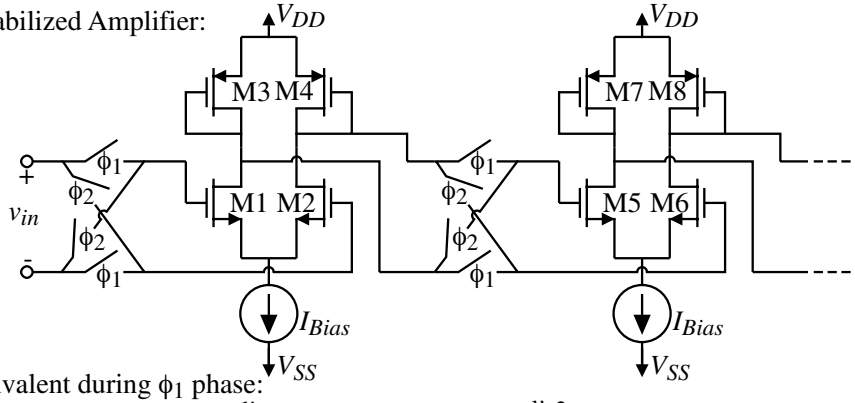


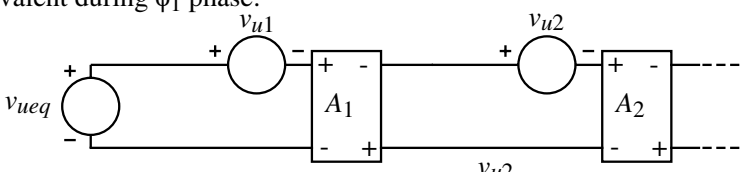
Fig. 7.5-8

Chopper-Stabilized Amplifier

Chopper-stabilized Amplifier:

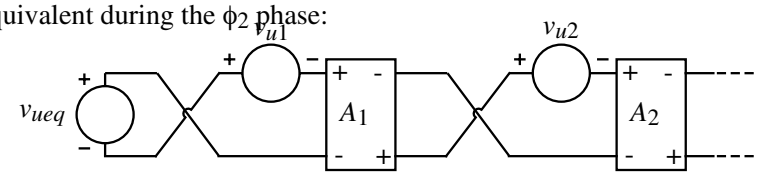


Circuit equivalent during ϕ_1 phase:



$$v_{ueq} = v_{u1} + \frac{v_{u2}}{A_1}$$

Circuit equivalent during the ϕ_2 phase:



$$v_{ueq} = -v_{u1} + \frac{v_{u2}}{A_1}\ ,\ v_{ueq}(\text{aver}) = \frac{v_{u2}}{A_1}$$

Fig. 7.5-10

Experimental Noise Response of the Chopper-Stabilized Amplifier

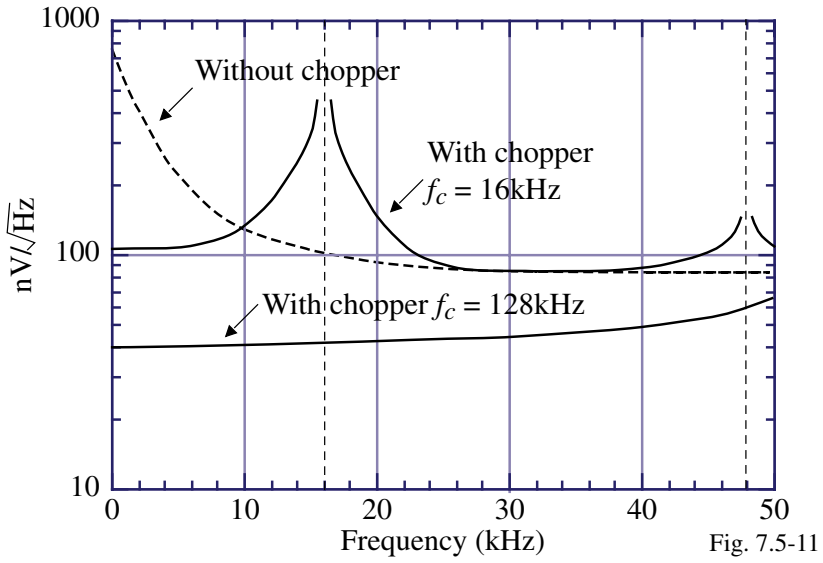


Fig. 7.5-11

Comments:

- The switches in the chopper-stabilized op amp introduce a thermal noise equal to *kT/C* where *k* is Boltzmann's constant, *T* is absolute temperature and *C* are capacitors charged by the switches (parasitics in the case of the chopper-stabilized amplifier).
- Requires two-phase, non-overlapping clocks.
- Trade-off between the lowering of 1/*f* noise and the introduction of the *kT/C* noise.

SUMMARY

- Primary sources of noise for CMOS circuits is thermal and 1/f
- Noise analysis:
  1.) Insert a noise generator for each transistor that contributes to the noise. (Generally ignore the current source transistor of source-coupled pairs.)
  2.) Find the output noise voltage across an open-circuit or output noise current into a short circuit.
  3.) Reflect the total output noise back to the input resulting in the equivalent input noise voltage.
- Noise is reduced in op amps by making the input stage gain as large as possible and reducing the noise of this stage as much as possible.
- The input stage noise can be reduced by using lateral BJTs (particularily the 1/f noise)
- Doubly correlated sampling can transfer the noise at low frequencies to the clock frequency (this technique is used to achieve low input offset voltage op amps).