LECTURE 350 – LOW VOLTAGE OP AMPS
(READING: AH – 415-432)

Objective

The objective of this presentation is:

1.) How to design standard circuit blocks with reduced power supply voltage

2.) Introduce new methods of designing low voltage circuits

Outline

- Low voltage input stages
- Low voltage bias circuits
- Low voltage op amps
- Examples
- Summary

Introduction

While low voltage op amps can be easily designed in weak inversion, strong inversion leads to higher performance and is the focus of this section.

Semiconductor Industry Associates Roadmap for Power Supplies:

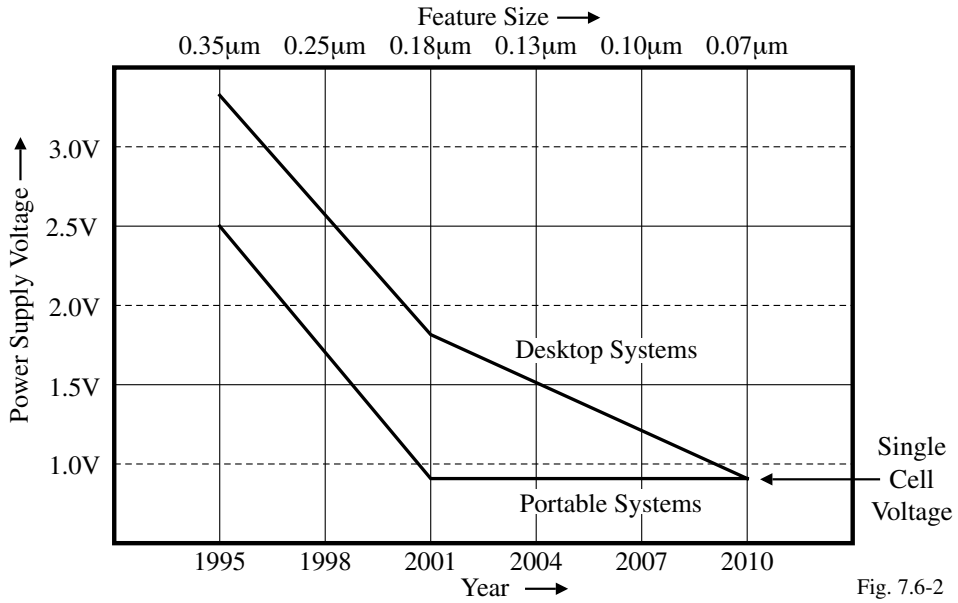


Fig. 7.6-2

Threshold voltages will remain about 0.5 to 0.7V in order to allow the MOSFET to be turned off.

Implications of Low-Voltage, Strong-Inversion Operation

- Reduced power supply means decreased dynamic range
- Nonlinearity will increase because the transistor is working close to V_{DS}(sat)
- Large values of λ because the transistor is working close to V_{DS}(sat)
- Increased drain-bulk and source-bulk capacitances because they are less reverse biased.
- Large values of currents and *W/L* ratios to get high transconductance
- Small values of currents and large values of *W/L* will give smallV_{DS}(sat)
- Severely reduced input common mode range
- Switches will require charge pumps

Approach

- Low voltage input stages with reasonable *ICMR*
- Low voltage bias and load circuits
- Low voltage op amps

Differential Amplifier with Current Source Loads

Minimum power supply (*ICMR* = 0):

$$V_{DD}(\text{min}) = V_{SD3}(\text{sat})-V_{T1}+V_{GS1}+V_{DS5}(\text{sat})$$
$$= V_{SD3}(\text{sat})+V_{DS1}(\text{sat})+V_{DS5}(\text{sat})$$

Input common-mode range:

$$V_{icm}(\text{upper}) = V_{DD} - V_{SD3}(\text{sat}) + V_{T1}$$
$$V_{icm}(\text{lower}) = V_{DS5}(\text{sat}) + V_{GS1}$$

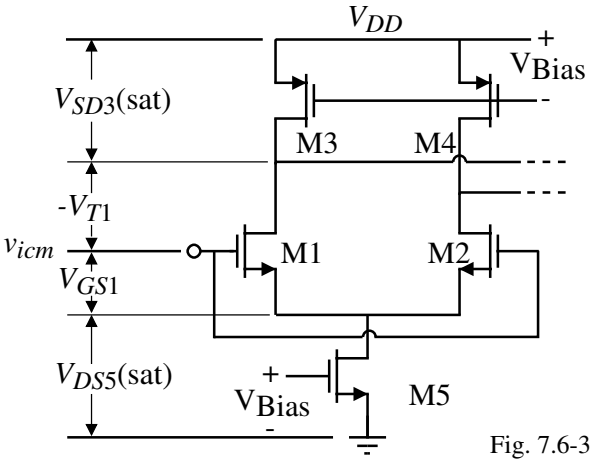


Fig. 7.6-3

Example:

If the threshold magnitudes are 0.7V, V_{DD} = 1.5V and the saturation voltages are 0.3V, then

V_{icm}(upper) = 1.5 - 0.3 + 0.7 = 1.9V and V_{icm}(lower) = 0.3 + 1.0 = 1.3V

giving an *ICMR* of 0.6V.

Increasing *ICMR* using Parallel Input Stages

Turn-on voltage for the n-channel input:

$V_{onn} = V_{DSN5}(\text{sat}) + V_{GSN1}$

Turn-on voltage for the p-channel input:

$V_{onp} = V_{DD} - V_{SDP5}(\text{sat}) - V_{SGP1}$

The sum of V_{onn} and V_{onp} equals the minimum power supply.

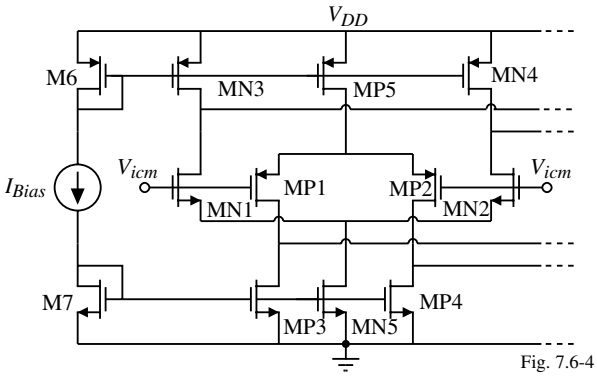


Fig. 7.6-4

Regions of operation:

$V_{DD} > V_{icm} > V_{onp}$: (n-channel on and p-channel off) $g_m(\text{eq}) = g_{mN}$

$V_{onp} \geq V_{icm} \geq V_{onn}$: (n-channel on and p-channel on) $g_m(\text{eq}) = g_{mN} + g_{mP}$

$V_{onn} > V_{icm} > 0$: (n-channel off and p-channel on) $g_m(\text{eq}) = g_{mP}$

where g_m(eq) is the equivalent input transconductance of the above input stage, g_{mN} is the input transconductance for the n-channel input and g_{mP} is the input transconductance for the p-channel input.

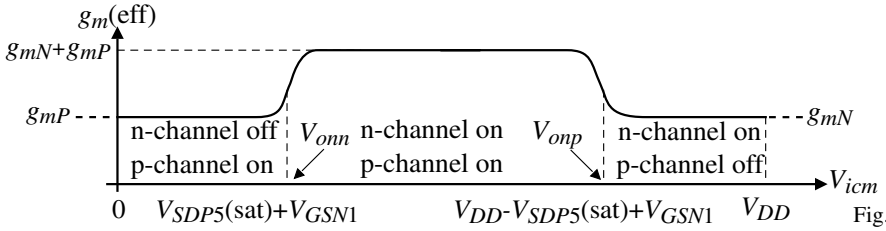


Fig. 7.6-5

Removing the Nonlinearity in Transconductances as a Function of *ICMR*

Increase the bias current in the differential amplifier that is on when the other differential amplifier is off.

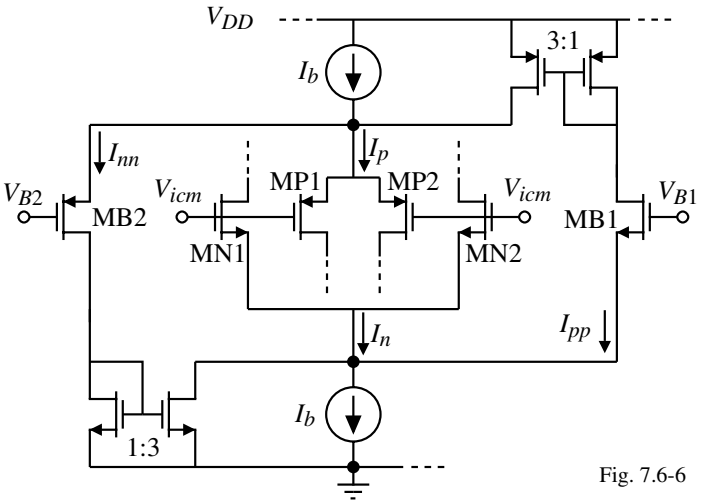


Fig. 7.6-6

Three regions of operation depending on the value of V_{icm}:

1.) $V_{icm} < V_{onn}$: n-channel diff. amp. off and p-channel on with $I_p = 4I_b$:

$$g_m(\text{eff}) = \sqrt{\frac{K_P' W_P}{L_P}}\, 2\sqrt{I_b}$$

2.) $V_{onn} < V_{icm} < V_{onp}$: both on with $I_n = I_p = I_b$:

$$g_m(\text{eff}) = \sqrt{\frac{K_N' W_N}{L_N}}\,\sqrt{I_b} + \sqrt{\frac{K_P' W_P}{L_P}}\,\sqrt{I_b}$$

3.) $V_{icm} > V_{onp}$: p-channel diff. amp. off and n-channel on with $I_n = 4I_b$:

$$g_m(\text{eff}) = \sqrt{\frac{K_N' W_N}{L_N}}\, 2\sqrt{I_b}$$

How Does the Current Compensation Work?

Set $V_{B1} = V_{onn}$ and $V_{B2} = V_{onp}$.

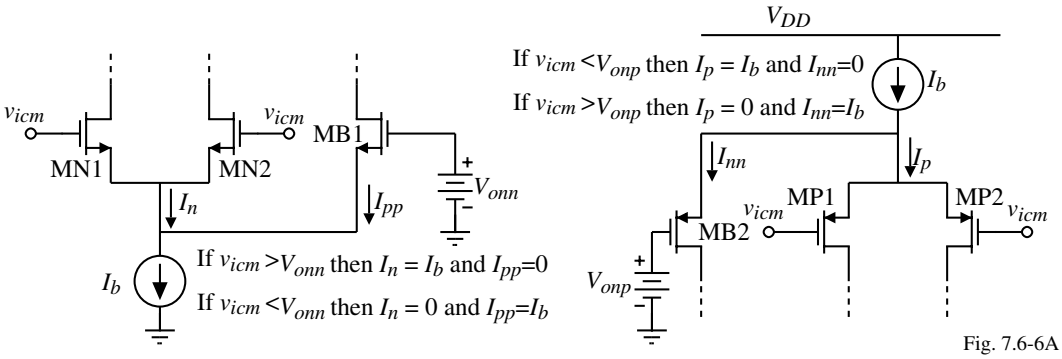


Fig. 7.6-6A

Result:

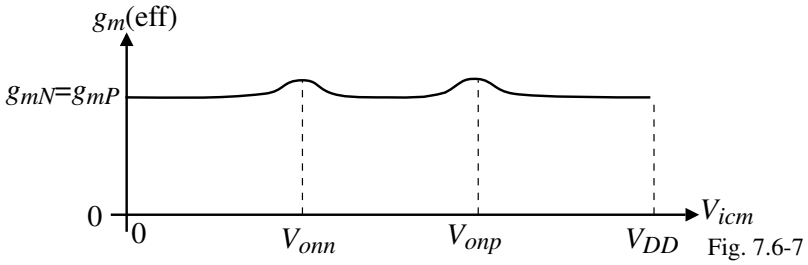


Fig. 7.6-7

The above techniques and many similar ones are good for power supply values down to about 1.5V. Below than, different techniques must be used or the technology must be modified (natural devices).

Bulk-Driven MOSFET

A depletion device would permit large *ICMR* even with very small power supply voltages because V_{GS} is zero or negative.

When a MOSFET is driven from the bulk with the gate held constant, it acts like a depletion transistor.

Cross-section of an n-channel bulk-driven MOSFET:

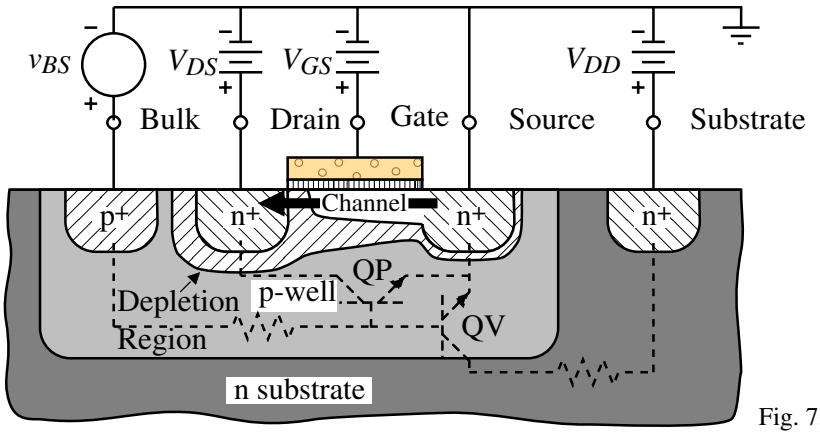


Fig. 7.6-8

Large signal equation:

$$i_D = \frac{K_N' W}{2L}\left[V_{GS} - V_{T0} - \gamma\sqrt{2|\phi_F| - v_{BS}} + \gamma\sqrt{2|\phi_F|}\right]^2$$

Small-signal transconductance:

$$g_{mbs} = \frac{\gamma\sqrt{(2K_N' W/L)I_D}}{2\sqrt{2|\phi_F| - V_{BS}}}$$

Bulk-Driven MOSFET - Continued

Transconductance characteristics:

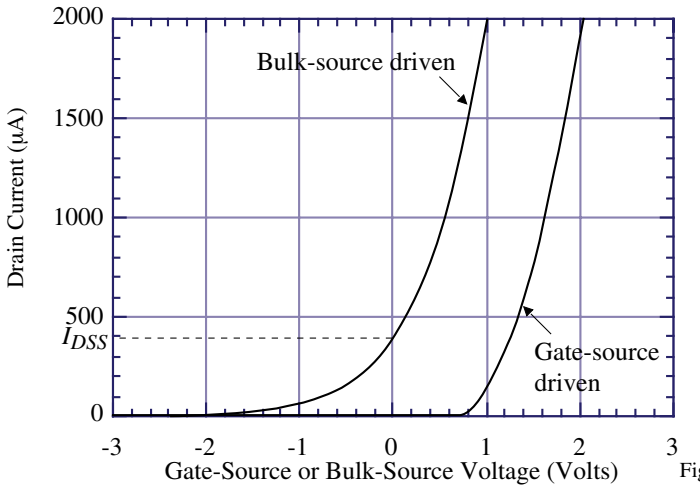


Fig. 7.6-9

Saturation: $V_{DS} > V_{BS} - V_P$ gives,

$$V_{BS} = V_P + V_{ON}$$

$$i_D = I_{DSS}\left(1 - \frac{V_{BS}}{V_P}\right)^2$$

Comments:

- g_m (bulk) > g_m(gate) if $V_{BS} > 0$ (forward biased)
- Noise of both configurations are the same (any differences comes from the gate versus bulk noise)
- Bulk-driven MOSFET tends to be more linear at lower currents than the gate-driven MOSFET
- Very useful for generation of I_{DSS} floating current sources.

Bulk-Driven, n-channel Differential Amplifier

What is the *ICMR*?

$$V_{icm}(\text{min}) = V_{SS} + V_{DS5}(\text{sat}) + V_{BS1} = V_{SS} + V_{DS5}(\text{sat}) - |V_{P1}| + V_{DS1}(\text{sat})$$

Note that V_{icm} can be less than V_{SS} if $|V_{P1}| > V_{DS5}(\text{sat}) + V_{DS1}(\text{sat})$

$V_{icm}(\text{max}) = ?$

As V_{icm} increases, the current through M1 and M2 is constant so the source increases. However, the gate voltage stays constant so that V_{GS1} decreases. Since the current must remain constant through M1 and M2 because of M5, the bulk-source voltage becomes less negative causing V_{TN1} to decrease and maintain the currents through M1 and M2 constant. If V_{icm} is increased sufficiently, the bulk-source voltage will become positive. However, current does not start to flow until V_{BS} is greater than 0.3 volts so the effective V_{icm}(max) is

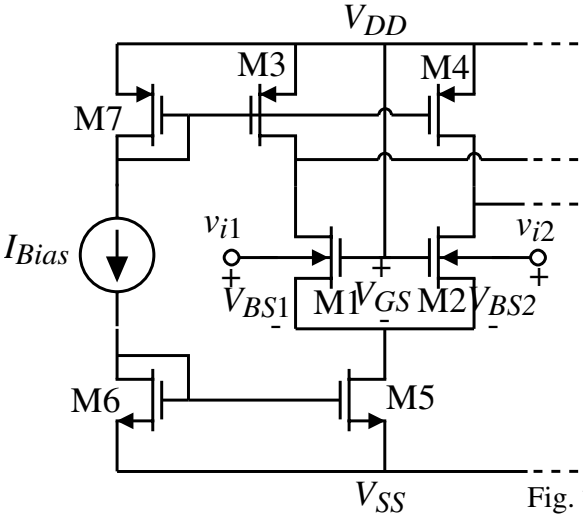


Fig. 7.6-10

$$V_{icm}(\text{max}) \approx V_{DD} - V_{SD3}(\text{sat}) - V_{DS1}(\text{sat}) + V_{BS1}.$$

Illustration of the *ICMR* of the Bulk-Driven, Differential Amplifier

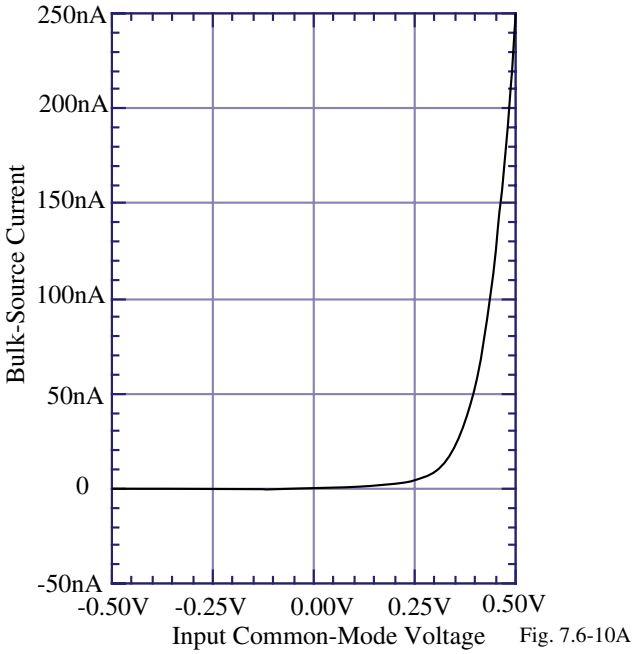


Fig. 7.6-10A

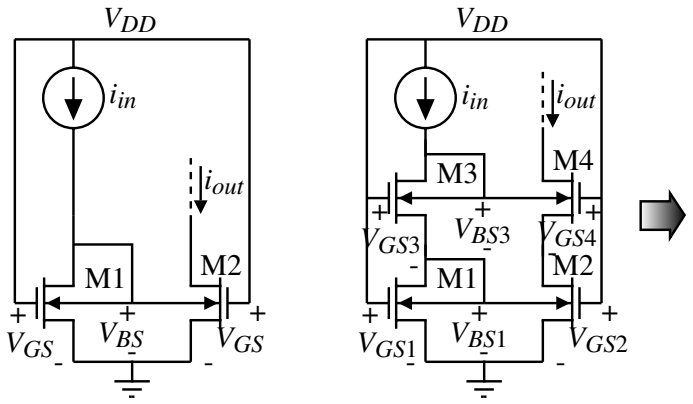
Comments:

- Effective *ICMR* is from V_{SS} to V_{DD} -0.3V
- The transconductance of the input stage can vary as much as 100% over the *ICMR* which makes it very difficult to compensate

Low-Voltage Current Mirrors using the Bulk-Driven MOSFET

The biggest problem with current mirrors is the large minimum input voltage required for previously examined current mirrors.

If the bulk-driven MOSFET is biased with a current that exceeds I_{DSS} then it is enhancement and can be used as a current mirror.



Simple bulk-driven current mirror

Cascodebulk-driven current mirror.

Fig.7.6-11

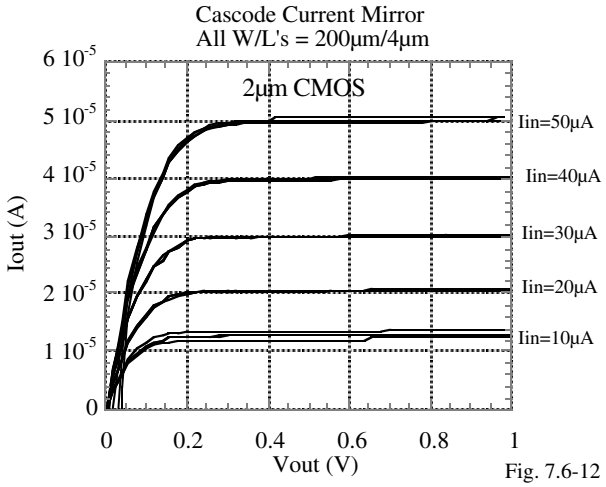


Fig. 7.6-12

The cascode current mirror gives a minimum input voltage of less than 0.5V for currents less than 100µA

Simple Current Mirror with Level Shifting

Since the drain can be V_T less than the gate, the drain could be biased to reduce the minimum input voltage as illustrated.

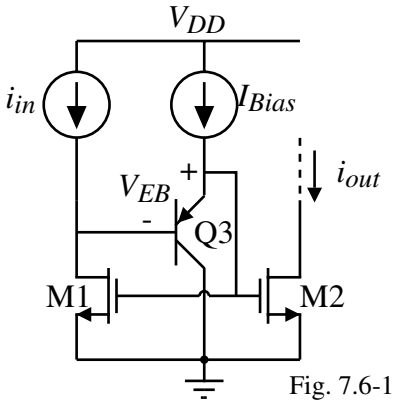


Fig. 7.6-13

A Low-Voltage Current Mirror with Wide Input and Output Swings

The current mirror below requires a power supply of V_T+3V_{ON} and has a V_{in}(min) = V_{ON} and a V_{out}(min) = $2V_{ON}$ (less for the regulated cascode output mirror).

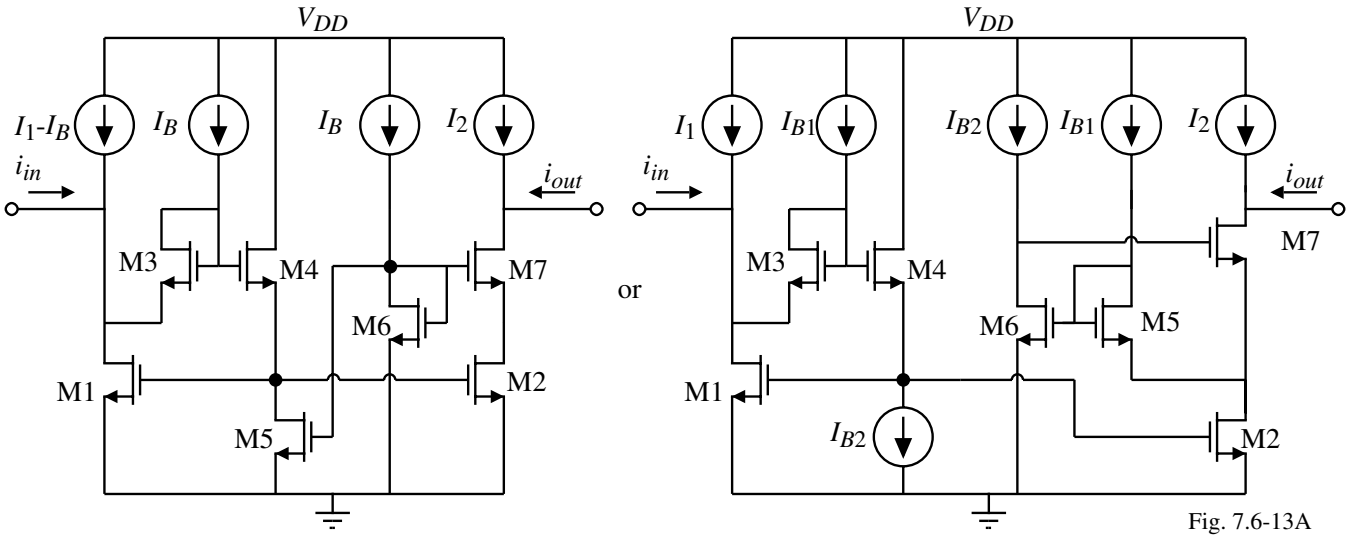
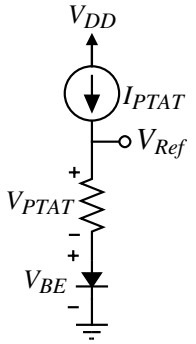
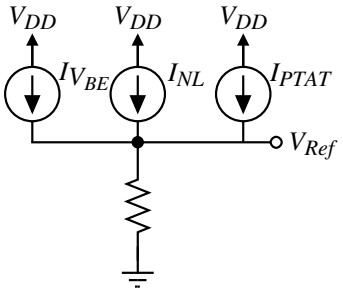


Fig. 7.6-13A

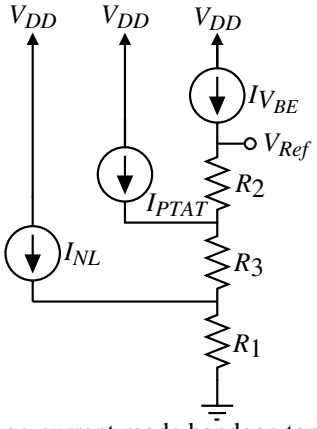
Bandgap Topologies Compatible with Low Voltage Power Supply



Voltage-mode bandgap topology.



Current-mode bandgap topology.



Voltage-current mode bandgap topology.

Fig. 7.6-14

Method of Generating Currents with *VBE* and PTAT Temperature Coefficients

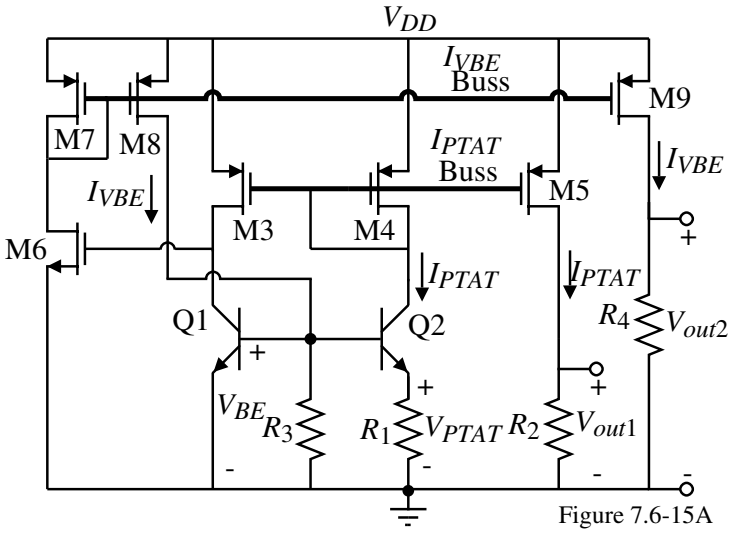
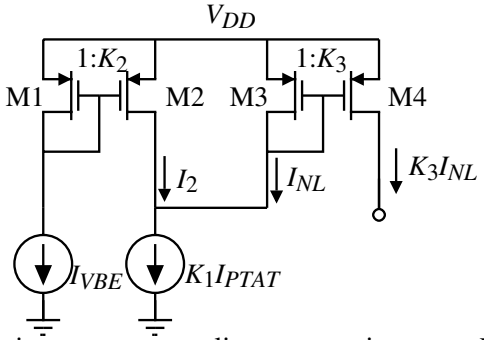


Figure 7.6-15A

$$V_{out1} = I_{PTAT}R_2 = \left(\frac{V_{PTAT}}{R_1}\right)R_2 = V_{PTAT}\frac{R_2}{R_1}$$

$$V_{out2} = I_{VBE}R_4 = \left(\frac{V_{BE}}{R_3}\right)R_4 = V_{BE}\frac{R_4}{R_3}$$

Technique for Canceling the Bandgap Curvature



Circuit to generate nonlinear correction term, I_{NL}.

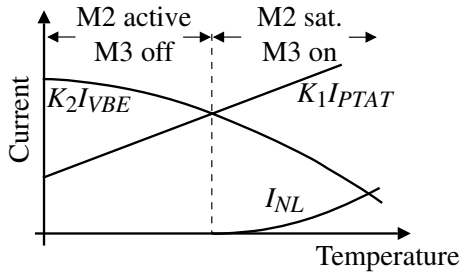


Illustration of the various currents.

Fig. 7.6-16

$$I_{NL} = \begin{cases} 0, & K_2I_{VBE} > K_1I_{PTAT} \\ K_1I_{PTAT} - K_2I_{VBE}, & K_2I_{VBE} < K_1I_{PTAT} \end{cases}$$

The combination of the above concept with the previous slide yielded a curvature-corrected bandgap reference of 0.596V with a TC of 20ppm/C° from -15C° to 90C° using a 1.1V power supply.† In addition, the line regulation was 408 ppm/V for $1.2 \le V_{DD} \le 10$V and 2000 ppm/V for $1.1 \le V_{DD} \le 10$V. The quiescent current was 14μA.

† G.A. Rincon-Mora and P.E. Allen, "A 1.1-V Current-Mode and Piecewise-Linear Curvature-Corrected Bandgap Reference," *J. of Solid-State Circuits*, vol. 33, no. 10, October 1998, pp. 1551-1554.

Low-Voltage Op Amp using Classical Techniques ($V_{DD} \geq 2V_T$)

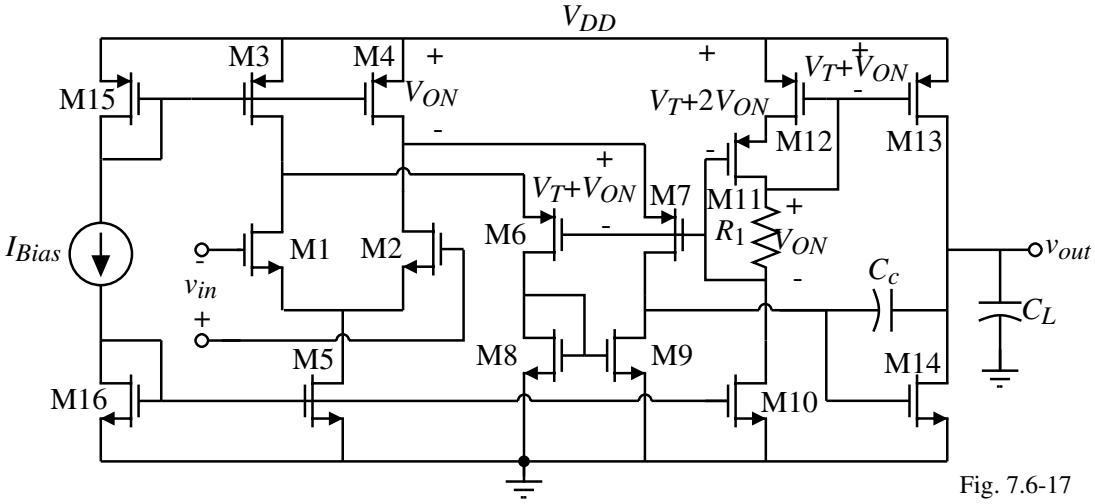


Fig. 7.6-17

Clever use of classical techniques.

Balanced inputs.

Example 7.6-1 - Design of a Low-Voltage Op Amp using the Previous Topology

Use the parameters of Table 3.1-2 to design the op amp above to meet the specifications given below.

$V_{DD} = 2V$ $V_{icm}(max) = 2.5V$ $V_{icm}(min) = 1V$

$V_{out}(max) = 1.75V$ $V_{out}(min) = 0.5V$ $GB = 10MHz$

Slew rate = ±10V/μs Phase margin = 60° for $C_L = 10pF$

Solution

Assuming the conditions for a two-stage op amp necessary to achieve 60° phase margin and that the RHP zero is at least 10*GB* gives

$$C_c = 0.2C_L = 2pF$$

The slew rate is directly related to the current in M5 and gives

$$I_5 = C_c \cdot SR = 2x10^{-12} \cdot 10^7 = 20\mu A$$

We also know the input transconductances from *GB* and C_c. They are given as

$$g_{m1} = g_{m2} = GB \cdot C_c = 20\pi x10^6 \cdot 2x10^{-12} = 125.67\mu S$$

Knowing the current flow in M1 and M2 gives the W/L ratios as

$$\frac{W_1}{L_1} = \frac{W_2}{L_2} = \frac{g_{m1}^2}{2K_N'(I_1/2)} = \frac{(125.67x10^{-6})^2}{2 \cdot 110x10^{-6} \cdot 10x10^{-6}} = 7.18$$

Example 7.6-1 - Continued

Next, we find the W/L of M5 that will satisfy $V_{icm}(min)$ specification.

$$V_{icm}(min) = V_{DS5}(sat) + V_{GS1}(10\mu A) = 1V$$

This gives

$$V_{DS5}(sat) = 1 - \sqrt{\frac{2 \cdot 10}{110 \cdot 7.18}} - 0.75 = 1 - 0.159 - 0.75 = 0.0909V$$

$$\therefore \quad V_{DS5}(sat) = 0.0909 = \sqrt{\frac{2 \cdot I_5}{K_N'(W_5/L_5)}} \quad \rightarrow \quad \frac{W_5}{L_5} = \frac{2 \cdot 20}{110 \cdot (0.0909)^2} = 44$$

The design of M3 and M4 is accomplished from the upper input common mode voltage:

$$V_{icm}(max) = V_{DD} - V_{SD3}(sat) + V_{TN} = 2 - V_{SD3}(sat) + 0.75 = 2.5V$$

Solving for $V_{SD3}(sat)$ gives 0.25V. Assume that the currents in M6 and M7 are 20μA. This gives a current of 30μA in M3 and M4. Knowing the current in M3 (M4) gives

$$V_{SD3}(sat) \le \sqrt{\frac{2 \cdot 30}{50 \cdot (W_3/L_3)}} \quad \rightarrow \quad \frac{W_3}{L_3} = \frac{W_4}{L_4} \ge \frac{2 \cdot 30}{(0.25)^2 \cdot 50} = 19.2$$

Next, using the $V_{SD}(sat) = V_{ON}$ of M3 and M4, design M10 through M12. Let us assume that $I_{10} = I_5 = 20\mu A$ which gives $W_{10}/L_{10} = 44$. R_1 is designed as $R_1 = 0.25V/20\mu A = 12.5k\Omega$. The W/L ratios of M11 and M12 can be expressed as

$$\frac{W_{11}}{L_{11}} = \frac{W_{12}}{L_{12}} = \frac{2 \cdot I_{11}}{K_P' \cdot V_{SD11}(sat)^2} = \frac{2 \cdot 20}{50 \cdot (0.25)^2} = 12.8$$

Example 7.6-1 - Continued

Since the source-gate voltages and currents of M6 and M7 are the same as M11 and M12 then the W/L values are equal. Thus

$$W_6/L_6 = W_7/L_7 = 12.8$$

M8 and M9 should be as small as possible to reduce the parasitic (mirror) pole. However, the voltage drop across M4, M6 and M8 must be less than the power supply. Using this to design the gate-source voltage of M8 gives

$$V_{GS8} = V_{DD} - 2V_{ON} = 2\text{V} - 2\cdot 0.25 = 1.5\text{V}$$

Thus,

$$\frac{W_8}{L_8} = \frac{W_9}{L_9} = \frac{2\cdot I_8}{K_N'\cdot V_{DS8}(\text{sat})^2} = \frac{2\cdot 30}{110\cdot(0.75)^2} = 0.97 \approx 1$$

Because M8 and M9 are small, the mirror pole will be insignificant. The next poles of interest would be those at the sources of M6 and M7. Assuming the channel length is 1μm, these poles are given as

$$p_6 \approx \frac{g_{m6}}{C_{GS6}} = \frac{\sqrt{2K_P'\cdot(W_6/L_6)\cdot I_6}}{(2/3)\cdot W_6\cdot L_6\cdot C_{ox}} = \frac{\sqrt{2\cdot 50\cdot 12.8\cdot 20}\ \text{x}10^{-6}}{(2/3)\cdot 12.8\cdot 1\cdot 2.47\text{x}10^{-15}} = 7.59\text{x}10^9 \text{ rads/sec}$$

which is about 100 times greater than *GB*.

Finally, the W/L ratios of the second stage must be designed. We can either use the relationship for 60° phase margin of $g_{m14} = 10g_{m1} = 1256.7\mu\text{S}$ or consider proper mirroring between M9 and M14.

Example 7.6-1 - Continued

Substituting 1256.7μS for g_{m14} and 0.5V for V_{DS14} in $W/L = g_m/(K_N'\ V_{DS}(\text{sat}))$ gives $W_{14}/L_{14} = 22.85$ which gives $I_{14} = 314\mu\text{A}$. The W/L of M13 is designed by the necessary current ratio desired between the two transistors and is

$$\frac{W_{13}}{L_{13}} = \frac{I_{13}}{I_{12}} I_{12} = \frac{314}{20}\cdot 12.8 = 201$$

Now, check to make sure that the $V_{out}(\text{max})$ is satisfied. The saturation voltage of M13 is

$$V_{SD13}(\text{sat}) = \sqrt{\frac{2\cdot I_{13}}{K_P'\ (W_{13}/L_{13})}} = \sqrt{\frac{2\cdot 314}{50\cdot 201}} = 0.25\text{V}$$

which exactly meets the specification. For proper mirroring, the W/L ratio of M14 is,

$$\frac{W_9}{L_9} = \frac{I_9}{I_{14}}\frac{W_{14}}{L_{14}} = 1.46$$

Since W_9/L_9 was selected as 1, this is close enough.

The parameters are $g_{ds7} = 1\mu\text{S}$, $g_{ds8} = 0.8\mu\text{S}$, $g_{ds13} = 15.7\mu\text{S}$ and $g_{ds14} = 12.56\mu\text{S}$. Therefore small signal voltage gain is ($R_I \approx r_{ds9}$ because M7 is part of a cascode conf.)

$$\frac{v_{out}}{v_{in}} \approx \left(\frac{g_{m1}}{g_{ds9}}\right)\left(\frac{g_{m14}}{g_{ds13}+g_{ds14}}\right) = \left(\frac{125.6}{1.8}\right)\left(\frac{1256.7}{28.26}\right) = 69.78\cdot 44.47 = 3{,}103\text{V/V}$$

The power dissipation, including I_{bias} of 20μA, is 708μW.

The minimum power supply voltage is $V_T + 3\Delta V \approx 1.5\text{V}$ if $V_T = 0.7\text{V}$ and $\Delta V \approx 0.25\text{V}$.

A 1-Volt, Two-Stage Op Amp

Uses a bulk-driven differential input amplifier.

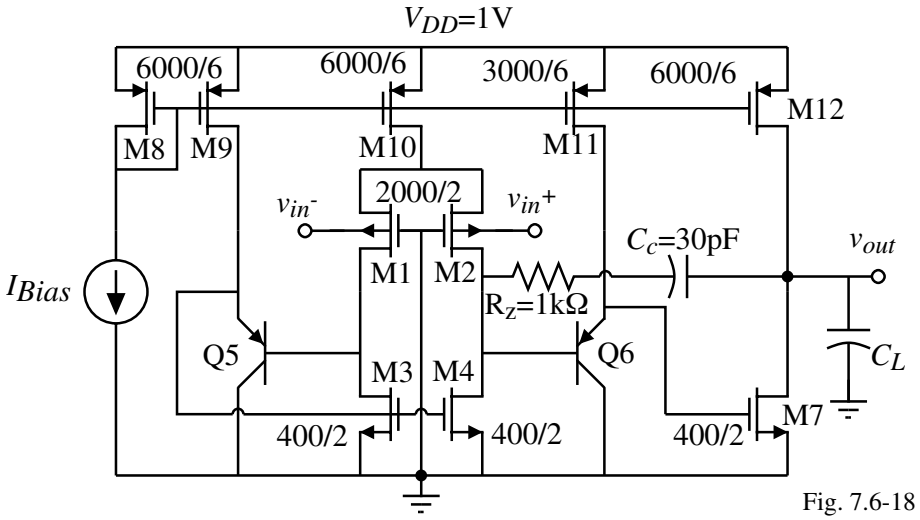


Fig. 7.6-18

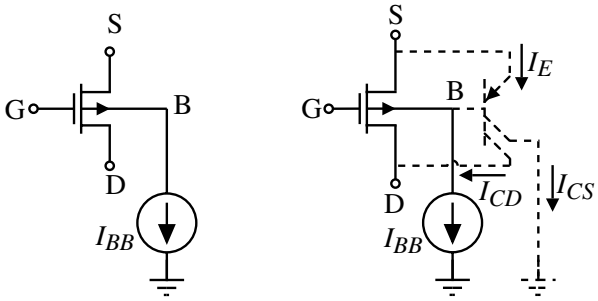
Performance of the 1-Volt, Two-Stage Op Amp

Specification (V_{DD}=0.5V, V_{SS}=-0.5V)	Measured Performance (C_L = 22pF)
DC open-loop gain	49dB (V_{icm} mid range)
Power supply current	300μA
Unity-gainbandwidth (*GB*)	1.3MHz (V_{icm} mid range)
Phase margin	57° (V_{icm} mid range)
Input offset voltage	±3mV
Input common mode voltage range	-0.475V to 0.450V
Output swing	-0.475V to 0.491V
Positive slew rate	+0.7V/μsec
Negative slew rate	-1.6V/μsec
THD, closed loop gain of -1V/V	-60dB (0.75Vp-p, 1kHz sinewave) -59dB (0.75Vp-p, 10kHz sinewave)
THD, closed loop gain of +1V/V	-59dB (0.75Vp-p, 1kHz sinewave) -57dB (0.75Vp-p, 10kHz sinewave)
Spectral noise voltage density	367nV/$\sqrt{\text{Hz}}$ @ 1kHz 181nV/$\sqrt{\text{Hz}}$ @ 10kHz, 81nV/$\sqrt{\text{Hz}}$ @ 100kHz 444nV/$\sqrt{\text{Hz}}$ @ 1MHz
Positive Power Supply Rejection	61dB at 10kHz, 55dB at 100kHz, 22dB at 1MHz
Negative Power Supply Rejection	45dB at 10kHz, 27dB at 100kHz, 5dB at 1MHz

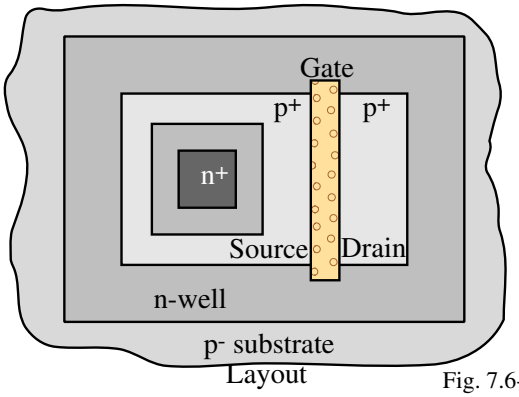
Further Considerations of the using the Bulk - Current Driven Bulk[†]

The bulk can be used to reduce the threshold sufficiently to permit low voltage applications. The key is to keep the substrate current confined.

One possible technique is:



Reduced Threshold MOSFET Parasitic BJT



Layout Fig. 7.6-19

Problem:

Want to limit the BJT current to some value called, I_{max}.

Therefore,

$$I_{BB} = \frac{I_{max}}{\beta_{CS} + \beta_{CD} + 1}$$

[†] T. Lehmann and M. Cassia, "1V Power Supply CMOS Cascode Amplifier," *IEEE J. of Solid-State Circuits*, Vol. 36, No. 7, 2001

Current-Driven Bulk Technique - Continued

Bias circuit for keeping the I_{max} defined independent of BJT betas.

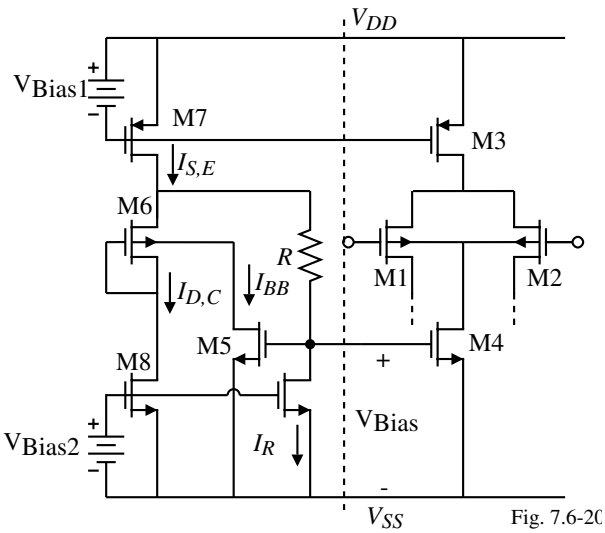


Fig. 7.6-20

Note:

$I_{D,C} = I_{DC} + I_D$

$I_{S,E} = I_D + I_E + I_R$

The circuit feedback causes a bulk bias current I_{BB} and hence a bias voltage V_{BIAS} such that

$I_{S,E} = I_D + I_{BB}(1+\beta_{CS} + \beta_{CD}) + I_R$ regardless of the actual values of the β's.

Use $V_{Bias}1$ and $V_{Bias}2$ to set $I_{D,C} \approx 1.1I_D$, $I_{S,E} \approx 1.3I_D$ and $I_R \approx 0.1I_D$ which sets I_{max} at $0.1I_D$.

For the circuit to work,

$V_{BE} < V_{TN} + I_R R$ and $|V_{TP}| + V_{DS}(\text{sat}) < V_{TN} + I_R R$

If $|V_{TP}| > V_{TN}$, then the level shifter $I_R R$ can be eliminated.

A 1-Volt, Folded-Cascode OTA using the Current-Driven Bulk Technique

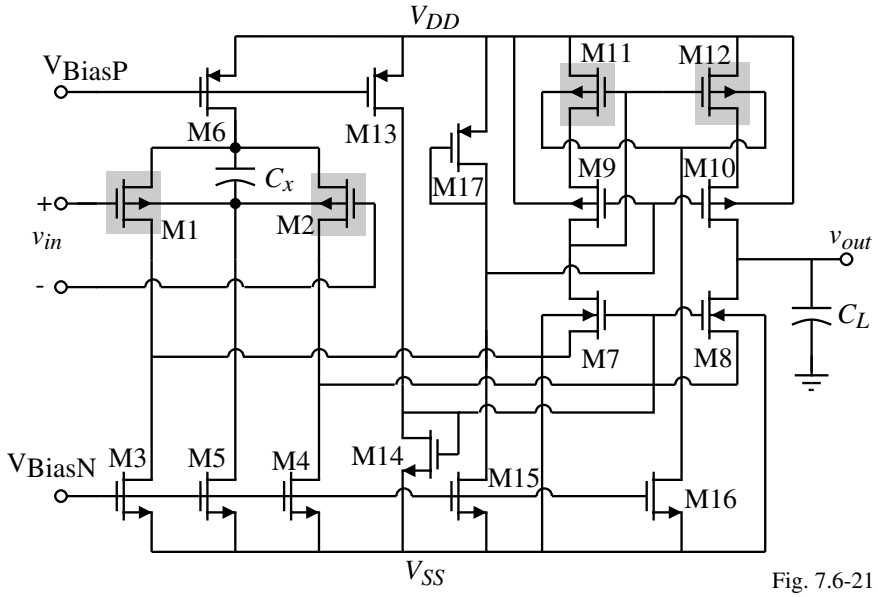


Fig. 7.6-21

Transistors with forward-biased bulks are in a shaded box.

For large common mode input changes, C_x, is necessary to avoid slewing in the input stage.

To get more voltage headroom at the output, the transistors of the cascode mirror have their bulks current driven.

A 1-Volt, Folded-Cascode OTA using the Current-Driven Bulk Technique - Continued

Experimental results:

0.5µm CMOS, 40µA total bias current (C_x = 10pF)

Supply Voltage	1.0V	0.8V	0.7V
Common-mode input range	0.0V-0.65V	0.0V-0.4V	0.0V-0.3V
High gain output range	0.35V-0.75V	0.25V-0.5V	0.2V-0.4V
Output saturation limits	0.1V-0.9V	0.15V-0.65V	0.1V-0.6V
DC gain	62dB-69dB	46dB-53dB	33dB-36dB
Gain-Bandwidth	2.0MHz	0.8MHz	1.3MHz
Slew-Rate (C_L=20pF)	0.5V/µs	0.4V/µs	0.1V/µs
Phase margin (C_L=20pF)	57°	54°	48°

The nominal value of bulk current is 10nA gives a 10% increase in differential pair quiescent current assuming a BJT β of 100.

SUMMARY

- Integrated circuit power supplies are rapidly decreasing (today 2-3Volts)
- Classical analog circuit design techniques begin to deteriorate at 1.5-2 Volts
- Approaches for lower voltage circuits:
  - Use natural NMOS transistors ($V_T \approx 0.1$V)
  - Drive the bulk terminal
  - Forward bias the bulk
  - Use depeletion devices
- The dynamic range will be compressed if the noise is not also reduced
- Fortunately, the threshold reduction continues to allow the techniques of this section to be used in today's technology