LECTURE 370 – TWO-STAGE OPEN-LOOP COMPARATORS-I
(READING: AH – 445-461)

Objective

The objective of this presentation is:

1.) Illustrate the performance and design of a two-stage open-loop comparator

Outline

- Two-stage, open-loop comparator performance
- Initial states of the two-stage, open-loop comparator
- Propagation delay time of a slewing, two-stage, open-loop comparator
- Design of a two-stage, open-loop comparator
- Summary

Two-Stage Comparator

An important category of comparators are those which use a high-gain stage to drive their outputs between V_{OH} and V_{OL} for very small input voltage changes.

The two-stage op amp without compensation is an excellent implementation of a high-gain, open-loop comparator.

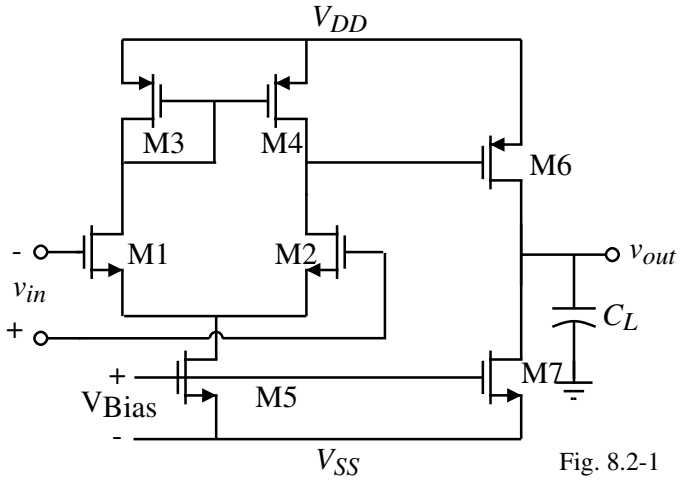

Fig. 8.2-1

Performance of the Two-Stage, Open-Loop Comparator

We know the performance should be similar to the uncompensated two-stage op amp.

Emphasis on comparator performance:

- Maximum output voltage

$$V_{OH} = V_{DD} - (V_{DD}-V_{G6}(\min)-|V_{TP}|)\left[1 - \sqrt{1 - \frac{8I_7}{\beta_6(V_{DD}-V_{G6}(\min)-|V_{TP}|)^2}}\right]$$

- Minimum output voltage

$$V_{OL} = V_{SS}$$

- Small-signal voltage gain

$$A_v(0) = \left(\frac{g_{m1}}{g_{ds2}+g_{ds4}}\right)\left(\frac{g_{m6}}{g_{ds6}+g_{ds7}}\right)$$

- Poles

Input:

$$p_1 = \frac{-(g_{ds2}+g_{ds4})}{C_I}$$

Output:

$$p_2 = \frac{-(g_{ds6}+g_{ds7})}{C_{II}}$$

- Frequency response

$$A_v(s) = \frac{A_v(0)}{\left(\frac{s}{p_1}+1\right)\left(\frac{s}{p_2}+1\right)}$$

Example 2-1 - Performance of a Two-Stage Comparator

Evaluate V_{OH}, V_{OL}, $A_v(0)$, $V_{in}(\min)$, p_1, p_2, for the two-stage comparator in Fig. 8.2-1. Assume that this comparator is the circuit of Ex. 6.3-1 with no compensation capacitor, C_c, and the minimum value of $V_{G6} = 0$V. Also, assume that $C_I = 0.2$pF and $C_{II} = 5$pF.

Solution

Using the above relations, we find that

$$V_{OH} = 2.5 - (2.5\text{-}0\text{-}0.7)\left[1 - \sqrt{1 - \frac{8\cdot 234\text{x}10^{-6}}{50\text{x}10^{-6}\cdot 38(2.5\text{-}0\text{-}0.7)^2}}\right] = 2.2\text{V}$$

The value of V_{OL} is -2.5V. The gain was evaluated in Ex. 6.3-1 as $A_v(0) = 7696$. Therefore, the input resolution is

$$V_{in}(\min) = \frac{V_{OH}-V_{OL}}{A_v(0)} = \frac{4.7\text{V}}{7696} = 0.611\text{mV}$$

Next, we find the poles of the comparator, p_1 and p_2. From Ex. 6.3-1 we find that

$$p_1 = \frac{g_{ds2} + g_{ds4}}{C_I} = \frac{15\text{x}10^{-6}(0.04+0.05)}{0.2\text{x}10^{-12}} = 6.75\text{x}10^6 \text{ (1.074MHz)}$$

and

$$p_2 = \frac{g_{ds6} + g_{ds7}}{C_{II}} = \frac{95\text{x}10^{-6}(0.04+0.05)}{5\text{x}10^{-12}} = 1.71\text{x}10^6 \text{ (0.272MHz)}$$

Linear Step Response of the Two-Stage Comparator

The step response of a circuit with two real poles ($p_1 \neq p_2$) is,

$$v_{out}(t) = A_v(0)V_{in}\left[1 + \frac{p_2 e^{-tp_1}}{p_1 - p_2} - \frac{p_1 e^{-tp_2}}{p_1 - p_2}\right]$$

Normalizing gives,

$$v_{out}'(t_n) = \frac{v_{out}(t)}{A_v(0)V_{in}} = 1 - \frac{m}{m-1}e^{-t_n} + \frac{1}{m-1}e^{-mt_n} \quad \text{where} \quad m = \frac{p_2}{p_1} \neq 1 \quad \text{and} \quad t_n = tp_1 = \frac{t}{\tau_1}$$

If $p_1 = p_2$ ($m = 1$), then $v_{out}'(t_n) = 1 - p_1 e^{-t_n} - \frac{t_n}{p_1} e^{-t_n} = 1 - e^{-t_n} - t_n e^{-t_n}$ where $p_1 = 1$.

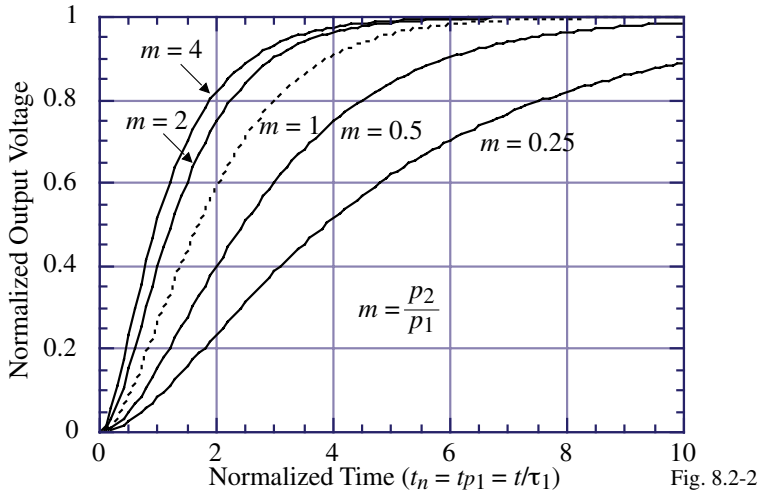

Fig. 8.2-2

Linear Step Response of the Two-Stage Comparator - Continued

The above results are valid as long as the slope of the linear response does not exceed the slew rate.

- Slope at $t = 0$ is zero
- Maximum slope occurs at ($m \neq 1$)

$$t_n(\max) = \frac{ln(m)}{m-1}$$

and is

$$\frac{dv_{out}'(t_n(\max))}{dt_n} = \frac{m}{m-1}\left[\exp\left(\frac{-ln(m)}{m-1}\right) - \exp\left(-m\frac{ln(m)}{m-1}\right)\right]$$

- For the two-stage comparator using NMOS input transistors, the slew rate is

$$SR^- = \frac{I_7}{C_{II}}$$

$$SR^+ = \frac{I_6 - I_7}{C_{II}} = \frac{0.5\beta_6(V_{DD} - V_{G6}(\min) - |V_{TP}|)^2 - I_7}{C_{II}}$$

Example 2-2 - Step Response of Ex. 2-1

Find the maximum slope of Ex. 2-1 and the time at which it occurs if the magnitude of the input step is v_{in}(min). If the dc bias current in M7 is 100μA, at what value of load capacitance, C_L would the transient response become slew limited? If the magnitude of the input step is $100v_{in}$(min), what is the new value of C_L at which slewing would occur?

Solution

The poles of the comparator were given in Ex. 2-1 as p_1 = -6.75x10^6 rads/sec. and p_2 = -1.71x10^6 rads/sec. This gives a value of m = 0.253. From the previous expressions, the maximum slope occurs at t_n(max) = 1.84 secs. Dividing by $|p_1|$ gives t(max) = 0.272μs. The slope of the transient response at this time is found as

$$\frac{dv_{out}'(t_n(\max))}{dt_n} = -0.338[\exp(-1.84) - \exp(-0.253\cdot 1.84)] = 0.159 \text{ V/sec}$$

Multiplying the above by $|p_1|$ gives

$$\frac{dv_{out}'(t(\max))}{dt} = 1.072\text{V/μs}$$

Therefore, if the slew rate is less than 1.072V/μs, the transient response will experience slewing. Also, if $C_L \geq$ 100μA/1.072V/μs or 93.3pF, the comparator will slew.

If the input is $100v_{in}$(min), then we must unnormalize the output slope as follows.

$$\frac{dv_{out}'(t(\max))}{dt} = \frac{v_{in}}{v_{in}(\min)}\frac{dv_{out}'(t(\max))}{dt} = 100\cdot 1.072\text{V/μs} = 107.2\text{V/μs}$$

Therefore, the comparator will now slew with a load capacitance of 0.933pF.

Propagation Delay Time (Non-Slew)

To find t_p, we want to set 0.5(V_{OH}-V_{OL}) equal to $v_{out}(t_n)$. However, $v_{out}(t_n)$ given as

$$v_{out}(t_n) = A_v(0)V_{in}\left[1 - \frac{m}{m\text{-}1}e^{-t_n} + \frac{1}{m\text{-}1}e^{-mt_n}\right]$$

can't be easily solved so approximate the step response as a power series to get

$$v_{out}(t_n) \approx A_v(0)V_{in}\left[1 - \frac{m}{m\text{-}1}\left(1\text{-}t_n + \frac{t_n^2}{2} + \cdots\right) + \frac{1}{m\text{-}1}\left(1\text{-}mt_n + \frac{m^2t_n^2}{2} + \cdots\right)\right] \approx \frac{mt_n^2A_v(0)V_{in}}{2}$$

Therefore, set $v_{out}(t_n) = 0.5(V_{OH}\text{-}V_{OL})$

$$\frac{V_{OH}+V_{OL}}{2} \approx \frac{mt_{pn}^2A_v(0)V_{in}}{2}$$

or

$$t_{pn} \approx \sqrt{\frac{V_{OH}+V_{OL}}{mA_v(0)V_{in}}} = \sqrt{\frac{V_{in}(\min)}{mV_{in}}} = \frac{1}{\sqrt{mk}}$$

This approximation is particularly good for large values of k.

Example 2-3 - Propagation Delay Time of a Two-Pole Comparator (Non-Slew)

Find the propagation time delay of Ex. 2-1 if V_{in} = 10mV, 100mV and 1V.

Solution

From Ex. 2-1 we know that V_{in}(min) = 0.611mV and m = 0.253. For V_{in} = 10mV, k = 16.366 which gives $t_{pn} \approx 0.491$. The propagation time delay is equal to 0.491/6.75x10^6 or 72.9nS. This corresponds well with Fig. 8.2-2 where the normalized propagation time delay is the time at which the amplitude is 1/2k or 0.031 which corresponds to t_{pn} of approximately 0.5. Similarly, for V_{in} = 100mV and 1V we get a propagation time delay of 23ns and 7.3ns, respectively.

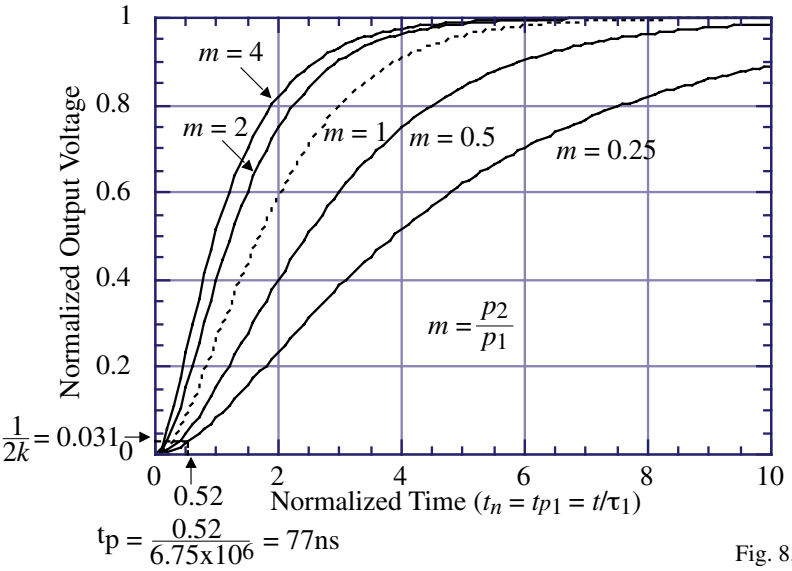

Fig. 8.2-2A

Initial Operating States for the Two-Stage, Open-Loop Comparator

What are the initial operating states for the two-stage, open-loop comparator?

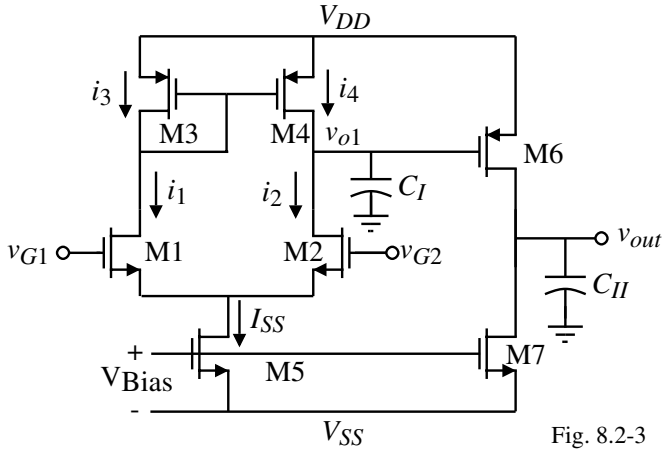

Fig. 8.2-3

1.) Assume $v_{G2} = V_{REF}$ and $v_{G1} > V_{REF}$ with $i_1 < I_{SS}$ and $i_2 > 0$.

Initially, $i_4 > i_2$ and v_{o1} increases, M4 becomes active and i_4 decreases until $i_3 = i_4$. v_{o1} is in the range of,

$V_{DD} - V_{SD4}(\text{sat}) < v_{o1} < V_{DD}$, $\quad v_{G1} > V_{REF}$, $i_1 < I_{SS}$ and $i_2 > 0$

and the value of v_{out} is

$v_{out} \approx V_{SS}$ $\quad v_{G1} > V_{REF}$, $i_1 < I_{SS}$ and $i_2 > 0$

2.) Assume $v_{G2} = V_{REF}$ and $v_{G1} >> V_{REF}$, therefore $i_1 = I_{SS}$ and $i_2 = 0$ which gives

$v_{o1} = V_{DD}$ and $v_{out} = V_{SS}$

Initial Operating States - Continued

3.) Assume $v_{G2} = V_{REF}$ and $v_{G1} < V_{REF}$ with $i_1>0$ and $i_2<I_{SS}$.

Initially, $i_4 < i_2$ and v_{o1} decreases. When $v_{o1} \leq V_{REF} - V_{TN}$, M2 becomes active and i_2 decreases. When $i_1 = i_2 = I_{SS}/2$ the circuit stabilizes and v_{o1} is in the range of,

$$V_{REF} - V_{GS2} < v_{o1} < V_{REF} - V_{GS2} + V_{DS2}(\text{sat})$$

or

$$V_{S2} < v_{o1} < V_{S2} + V_{DS2}(\text{sat}), \qquad v_{G1} < V_{G2},\ i_1 > 0 \text{ and } i_2 < I_{SS}$$

For the above conditions,

$$v_{out} = V_{DD} - (V_{DD}-v_{o1}-|V_{TP}|)\left[1 - \sqrt{1 - \frac{\beta_7 I_{SS}}{\beta_5\beta_6(V_{DD}-v_{o1}-|V_{TP}|)^2}}\right]$$

4.) Assume $v_{G2} = V_{REF}$ and $v_{G1} << V_{REF}$, therefore $i_2 = I_{SS}$ and $i_1 = 0$.

Same as in 3.) but now as v_{o1} approaches v_{S2} with $I_{SS}/2$ flowing, the value of v_{GS2} becomes larger and M5 becomes active and I_{SS} decreases. In the limit, $I_{SS} \rightarrow 0$, $v_{DS2} \approx 0$ and $v_{DS5} \approx 0$ resulting in

$$v_{o1} \approx V_{SS} \quad \text{and} \quad v_{out} = V_{DD} - (V_{DD}-V_{SS}-|V_{TP}|)\left[1 - \sqrt{1 - \frac{\beta_7 I_{SS}}{\beta_5\beta_6(V_{DD}-V_{SS}-|V_{TP}|)^2}}\right]$$

Initial Operating States - Continued

5.) Assume $v_{G1} = V_{REF}$ and $v_{G2}>V_{REF}$ with $i_2 < I_{SS}$ and $i_1>0$.

Initially, $i_4 < i_2$ and v_{o1} falls, M2 becomes active and i_2 decreases until $i_1 = i_2 = I_{SS}/2$. Therefore,

$$V_{REF} - V_{GS2}(I_{SS}/2) < v_{o1} < V_{REF} - V_{GS2}(I_{SS}/2) + V_{DS2}(\text{sat})$$

or

$$V_{S2}(I_{SS}/2) < v_{o1} < V_{S2}(I_{SS}/2) + V_{DS2}(\text{sat}), \qquad v_{G2} > V_{REF},\ i_1 > 0 \text{ and } i_2 < I_{SS}$$

and the value of v_{out} is

$$v_{out} = V_{DD} - (V_{DD}-v_{o1}-|V_{TP}|)\left[1 - \sqrt{1 - \frac{\beta_7 I_{SS}}{\beta_5\beta_6(V_{DD}-v_{o1}-|V_{TP}|)^2}}\right]$$

6.) Assume that $v_{G1} = V_{REF}$ and $v_{G2} >> V_{REF}$. When the source voltage of M1 or M2 causes M5 to be active, then I_{SS} decreases and

$$v_{o1} \approx V_{SS} \quad \text{and} \quad v_{out} = V_{DD} - (V_{DD}-V_{SS}-|V_{TP}|)\left[1 - \sqrt{1 - \frac{\beta_7 I_{SS}}{\beta_5\beta_6(V_{DD}-V_{SS}-|V_{TP}|)^2}}\right]$$

7.) Assume $v_{G1} = V_{REF}$ and $v_{G2} < V_{REF}$ and $i_1 <I_{SS}$ and $i_2 > 0$. Consequently, $i_4>i_2$ which causes v_{o1} to increase. When M4 becomes active i_4 decreases until $i_2 = i_4$ at which v_{o1} stabilizes at (M6 will be off under these conditions and $v_{out} \approx V_{SS}$).

$$V_{DD} - V_{SD4}(\text{sat}) < v_{o1} < V_{DD}, \qquad v_{G2} < V_{REF},\ i_1 < I_{SS} \text{ and } i_2 > 0$$

Initial Operating States - Continued

8.) Finally if $v_{G2} << V_{REF}$, then $i_1 = I_{SS}$ and $i_2 = 0$ and

$v_{o1} \approx V_{DD}$ and $v_{out} \approx V_{SS}$.

Summary of the Initial Operating States of the Two-Stage, Open-Loop Comparator using a N-channel, Source-coupled Input Pair:

Conditions	Initial State of v_{o1}	Initial State of v_{out}
$v_{G1}>V_{G2}$, $i_1<I_{SS}$ and $i_2>0$	$V_{DD}-V_{SD4}(\text{sat}) < v_{o1} < V_{DD}$	V_{SS}
$v_{G1}>>V_{G2}$, $i_1=I_{SS}$ and $i_2=0$	V_{DD}	V_{SS}
$v_{G1}<V_{G2}$, $i_1>0$ and $i_2<I_{SS}$	$v_{o1}=V_{G2}-V_{GS2,\text{act}}(I_{SS}/2)$, $\approx V_{SS}$ if M5 act.	Eq. (19), Sec. 5.1 for PMOS
$v_{G1}<<V_{G2}$, $i_1>0$ and $i_2<I_{SS}$	V_{SS}	Eq. (19), Sec. 5.1 for PMOS
$v_{G2}>V_{G1}$, $i_1>0$ and $i_2<I_{SS}$	$V_{S2}(I_{SS}/2)<v_{o1}<V_{S2}(I_{SS}/2)+V_{DS2}(\text{sat})$	Eq. (19), Sec. 5.1 for PMOS
$v_{G2}>>V_{G1}$, $i_1>0$ and $i_2<I_{SS}$	$V_{G1}-V_{GS1}(I_{SS}/2)$, $\approx V_{SS}$ if M5 active	Eq. (19), Sec. 5.1 for PMOS
$v_{G2}<V_{G1}$, $i_1<I_{SS}$ and $i_2>0$	$V_{DD}-V_{SD4}(\text{sat}) < v_{o1} < V_{DD}$	V_{SS}
$v_{G2}<<V_{G1}$, $i_1=I_{SS}$ and $i_2=0$	V_{DD}	V_{SS}

TO BE CONTINUED IN THE NEXT LECTURE