Objective
The objective of this presentation is:
1.) Illustrate the performance and design of a two-stage open-loop comparator

Outline
• Two-stage, open-loop comparator performance
• Initial states of the two-stage, open-loop comparator
• Propagation delay time of a slewing, two-stage, open-loop comparator
• Design of a two-stage, open-loop comparator
• Summary

Two-Stage Comparator
An important category of comparators are those which use a high-gain stage to drive their outputs between $V_{OH}$ and $V_{OL}$ for very small input voltage changes.

The two-stage op amp without compensation is an excellent implementation of a high-gain, open-loop comparator.

![Two-Stage Comparator Diagram](image-url)
Performance of the Two-Stage, Open-Loop Comparator

We know the performance should be similar to the uncompensated two-stage op amp. Emphasis on comparator performance:

- Maximum output voltage
  \[ V_{OH} = V_{DD} - (V_{DD} - V_{G6}(\text{min}) - |V_{TP}|)(1 - \sqrt{1 - \frac{8I_7}{\beta_6(V_{DD} - V_{G6}(\text{min}) - |V_{TP}|)^2}}) \]

- Minimum output voltage
  \[ V_{OL} = V_{SS} \]

- Small-signal voltage gain
  \[ A_v(0) = \frac{g_{m1}}{(g_{ds2} + g_{ds4})(g_{ds6} + g_{ds7})} \]

- Poles
  \[ p_1 = \frac{-(g_{ds2} + g_{ds4})}{C_I} \quad p_2 = \frac{-(g_{ds6} + g_{ds7})}{C_{II}} \]

- Frequency response
  \[ A_v(s) = \frac{s}{(s + p_1)(s + p_2)} \]

Example 2-1 - Performance of a Two-Stage Comparator

Evaluate \( V_{OH} \), \( V_{OL} \), \( A_v(0) \), \( V_{in}(\text{min}) \), \( p_1 \), \( p_2 \), for the two-stage comparator in Fig. 8.2-1. Assume that this comparator is the circuit of Ex. 6.3-1 with no compensation capacitor, \( C_c \), and the minimum value of \( V_{G6} = 0V \). Also, assume that \( C_I = 0.2pF \) and \( C_{II} = 5pF \).

Solution

Using the above relations, we find that
\[ V_{OH} = 2.5 - (2.5-0.7) \left[ 1 - \sqrt{1 - \frac{8 \times 10^{-6}}{50 \times 10^{-6} \times 38 \times (2.5-0.7)^2}} \right] = 2.2V \]
The value of \( V_{OL} \) is -2.5V. The gain was evaluated in Ex. 6.3-1 as \( A_v(0) = 7696 \). Therefore, the input resolution is
\[ V_{in}(\text{min}) = \frac{V_{OH} - V_{OL}}{A_v(0)} = \frac{4.7V}{7696} = 0.611mV \]

Next, we find the poles of the comparator, \( p_1 \) and \( p_2 \). From Ex. 6.3-1 we find that
\[ p_1 = \frac{g_{ds2} + g_{ds4}}{C_I} = \frac{15 \times 10^{-6} (0.04+0.05)}{0.2 \times 10^{-12}} = 6.75 \times 10^6 \text{ (1.074MHz)} \]
and
\[ p_2 = \frac{g_{ds6} + g_{ds7}}{C_{II}} = \frac{95 \times 10^{-6} (0.04+0.05)}{5 \times 10^{-12}} = 1.71 \times 10^6 \text{ (0.272MHz)} \]
Linear Step Response of the Two-Stage Comparator

The step response of a circuit with two real poles ($p_1 \neq p_2$) is,

$$v_{out}(t) = A_v(0)V_{in} \left[ 1 + \frac{p_2 e^{tp_1}}{p_1-p_2} - \frac{p_1 e^{tp_2}}{p_1-p_2} \right]$$

Normalizing gives,

$$v_{out}'(t_n) = \frac{v_{out}(t)}{A_v(0)V_{in}} = 1 - \frac{m}{m-1}e^{-tn} + \frac{1}{m-1}e^{-mtn} \quad \text{where} \quad m = \frac{p_2}{p_1} \neq 1 \quad \text{and} \quad t_n = tp_1 = \tau_1$$

If $p_1 = p_2$ ($m = 1$), then

$$v_{out}'(t_n) = 1 - p_1e^{-tn} - \frac{t_n}{p_1}e^{-tn} = 1 - e^{-tn} - t_ne^{-tn} \quad \text{where} \quad p_1 = 1.$$

![Normalized Output Voltage vs Normalized Time](image_url)

**Linear Step Response of the Two-Stage Comparator - Continued**

The above results are valid as long as the slope of the linear response does not exceed the slew rate.

- Slope at $t = 0$ is zero
- Maximum slope occurs at ($m \neq 1$)

$$t_{n(max)} = \frac{ln(m)}{m-1}$$

and is

$$\frac{dv_{out}'(t_{n(max)})}{dt_n} = m \left[ \frac{ln(m)}{m-1} \right] - \left[ \frac{ln(m)}{m-1} \right]$$

- For the two-stage comparator using NMOS input transistors, the slew rate is

$$SR^+ = \frac{I_7}{C_{II}}$$

$$SR^- = \frac{I_6-I_7}{C_{II}} = \frac{0.5\beta_6(V_{DD}-V_{G6(min)}-|V_{TPl}|)^2 - I_7}{C_{II}}$$
Example 2-2 - Step Response of Ex. 2-1

Find the maximum slope of Ex. 2-1 and the time at which it occurs if the magnitude of the input step is \( v_{in}(\text{min}) \). If the dc bias current in M7 is 100\( \mu \)A, at what value of load capacitance, \( C_L \) would the transient response become slew limited? If the magnitude of the input step is 100\( v_{in}(\text{min}) \), what is the new value of \( C_L \) at which slewing would occur?

**Solution**

The poles of the comparator were given in Ex. 2-1 as \( p_1 = -6.75 \times 10^6 \) rads/sec. and \( p_2 = -1.71 \times 10^6 \) rads/sec. This gives a value of \( m = 0.253 \). From the previous expressions, the maximum slope occurs at \( t_n(\text{max}) = 1.84 \) secs. Dividing by \(|p_1|\) gives \( t(\text{max}) = 0.272 \mu \)s. The slope of the transient response at this time is found as

\[
\frac{dv_{out}'(t_n(\text{max}))}{dt} = -0.338[\exp(-1.84) - \exp(-0.253 \times 1.84)] = 0.159 \text{ V/sec}
\]

Multiplying the above by \(|p_1|\) gives

\[
\frac{dv_{out}'(t(\text{max}))}{dt} = 1.072 \text{V/\mu s}
\]

Therefore, if the slew rate is less than 1.072V/\( \mu \)s, the transient response will experience slewing. Also, if \( C_L \geq 100\mu \)A/1.072V/\( \mu \)s or 93.3pF, the comparator will slew.

If the input is 100\( v_{in}(\text{min}) \), then we must unnormalize the output slope as follows.

\[
\frac{dv_{out}'(t(\text{max}))}{dt} = v_{in} \times \frac{dv_{out}'(t(\text{max}))}{dt} = 100 \times 1.072 \text{V/\mu s} = 107.2 \text{V/\mu s}
\]

Therefore, the comparator will now slew with a load capacitance of 0.933pF.

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**Propagation Delay Time (Non-Slew)**

To find \( t_p \), we want to set \( 0.5(VOH-VOL) \) equal to \( v_{out}(t_n) \). However, \( v_{out}(t_n) \) given as

\[
v_{out}(t_n) = A_v(0)V_{in} \left[ 1 - \frac{m}{m-1}e^{-t_n} + \frac{1}{m-1}e^{-mt_n} \right]
\]

can’t be easily solved so approximate the step response as a power series to get

\[
v_{out}(t_n) \approx A_v(0)V_{in} \left[ 1 - \frac{m}{m-1} \left(1-t_n^2 + \frac{t_n^2}{2} + \cdots \right) + \frac{1}{m-1} \left(1-mt_n^2 + \frac{m^2t_n^2}{2} + \cdots \right) \right] \approx \frac{mt_n^2 A_v(0)V_{in}}{2}
\]

Therefore, set \( v_{out}(t_n) = 0.5(VOH-VOL) \)

\[
\frac{VOH+VOL}{2} = \frac{mt_n^2 A_v(0)V_{in}}{2}
\]

or

\[
t_p = \sqrt{\frac{VOH+VOL}{mA_v(0)V_{in}}} = \sqrt{\frac{V_{in}(\text{min})}{mV_{in}}} = \frac{1}{\sqrt{mk}}
\]

This approximation is particularly good for large values of \( k \).
**Example 2-3 - Propagation Delay Time of a Two-Pole Comparator (Non-Slew)**

Find the propagation time delay of Ex. 2-1 if $V_{in} = 10$ mV, $100$ mV and $1$ V.

**Solution**

From Ex. 2-1 we know that $V_{in}(\text{min}) = 0.611$ mV and $m = 0.253$. For $V_{in} = 10$ mV, $k = 16.366$ which gives $t_{pn} \approx 0.491$. The propagation time delay is equal to $0.491/6.75 \times 10^6$ or 72.9 nS. This corresponds well with Fig. 8.2-2 where the normalized propagation time delay is the time at which the amplitude is $1/2k$ or 0.031 which corresponds to $t_{pn}$ of approximately 0.5. Similarly, for $V_{in} = 100$ mV and 1 V we get a propagation time delay of 23 nS and 7.3 nS, respectively.

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**Initial Operating States for the Two-Stage, Open-Loop Comparator**

What are the initial operating states for the two-stage, open-loop comparator?

1.) Assume $v_{G2} = V_{REF}$ and $v_{G1} > V_{REF}$ with $i_1 < I_{SS}$ and $i_2 > 0$.

Initially, $i_4 > i_2$ and $v_{o1}$ increases, M4 becomes active and $i_4$ decreases until $i_3 = i_4$. $v_{o1}$ is in the range of, $V_{DD} - V_{SD4(sat)} < v_{o1} < V_{DD}$, $v_{G1} > V_{REF}$, $i_1 < I_{SS}$ and $i_2 > 0$

and the value of $v_{out}$ is $v_{out} = V_{SS}$

2.) Assume $v_{G2} = V_{REF}$ and $v_{G1} >> V_{REF}$, therefore $i_1 = I_{SS}$ and $i_2 = 0$ which gives $v_{o1} = V_{DD}$ and $v_{out} = V_{SS}$
**Initial Operating States - Continued**

3.) Assume \( v_{G2} = V_{REF} \) and \( v_{G1} < V_{REF} \) with \( i_1 > 0 \) and \( i_2 < I_{SS} \).

Initially, \( i_4 < i_2 \) and \( v_{o1} \) decreases. When \( v_{o1} < V_{TN} \), M2 becomes active and \( i_2 \) decreases. When \( i_1 = i_2 = I_{SS}/2 \) the circuit stabilizes and \( v_{o1} \) is in the range of,

\[
V_{REF} - V_{GS2} < v_{o1} < V_{REF} - V_{GS2} + V_{DS2}(sat)
\]

or

\[
V_{S2} < v_{o1} < V_{S2} + V_{DS2}(sat), \quad v_{G1} < V_{G2}, \quad i_1 > 0 \quad \text{and} \quad i_2 < I_{SS}
\]

For the above conditions,

\[
v_{out} = V_{DD} - (V_{DD}-v_{o1}-|V_{TP1}|) \left[ 1 - \sqrt{1 - \frac{\beta_7 I_{SS}}{\beta_5 \beta_6 (V_{DD}-V_{SS}-|V_{TP1}|)^2}} \right]
\]

4.) Assume \( v_{G2} = V_{REF} \) and \( v_{G1} << V_{REF} \), therefore \( i_2 = I_{SS} \) and \( i_1 = 0 \).

Same as in 3.) but now as \( v_{o1} \) approaches \( V_{SS}/2 \) flowing, the value of \( v_{GS2} \) becomes larger and M5 becomes active and \( I_{SS} \) decreases. In the limit, \( I_{SS} \to 0, V_{DS2} \approx 0 \) and \( v_{DS5} \approx 0 \) resulting in

\[
v_{o1} \approx V_{SS} \quad \text{and} \quad v_{out} = V_{DD} - (V_{DD}-V_{SS}-|V_{TP1}|) \left[ 1 - \sqrt{1 - \frac{\beta_7 I_{SS}}{\beta_5 \beta_6 (V_{DD}-V_{SS}-|V_{TP1}|)^2}} \right]
\]

5.) Assume \( v_{G1} = V_{REF} \) and \( v_{G2} > V_{REF} \) with \( i_2 < I_{SS} \) and \( i_1 > 0 \).

Initially, \( i_4 < i_2 \) and \( v_{o1} \) falls, M2 becomes active and \( i_2 \) decreases until \( i_1 = i_2 = I_{SS}/2 \). Therefore,

\[
V_{REF} - V_{GS2}(I_{SS}/2) < v_{o1} < V_{REF} - V_{GS2}(I_{SS}/2) + V_{DS2}(sat)
\]

or

\[
V_{S2}(I_{SS}/2) < v_{o1} < V_{S2}(I_{SS}/2) + V_{DS2}(sat), \quad v_{G2} > V_{REF}, \quad i_1 > 0 \quad \text{and} \quad i_2 < I_{SS}
\]

and the value of \( v_{out} \) is

\[
v_{out} = V_{DD} - (V_{DD}-v_{o1}-|V_{TP1}|) \left[ 1 - \sqrt{1 - \frac{\beta_7 I_{SS}}{\beta_5 \beta_6 (V_{DD}-V_{SS}-|V_{TP1}|)^2}} \right]
\]

6.) Assume that \( v_{G1} = V_{REF} \) and \( v_{G2} >> V_{REF} \). When the source voltage of M1 or M2 causes M5 to be active, then \( I_{SS} \) decreases and

\[
v_{o1} \approx V_{SS} \quad \text{and} \quad v_{out} = V_{DD} - (V_{DD}-V_{SS}-|V_{TP1}|) \left[ 1 - \sqrt{1 - \frac{\beta_7 I_{SS}}{\beta_5 \beta_6 (V_{DD}-V_{SS}-|V_{TP1}|)^2}} \right]
\]

7.) Assume \( v_{G1} = V_{REF} \) and \( v_{G2} < V_{REF} \) and \( i_1 < I_{SS} \) and \( i_2 > 0 \). Consequently, \( i_4 > i_2 \) which causes \( v_{o1} \) to increase. When M4 becomes active \( i_4 \) decreases until \( i_1 = i_4 \) at which \( v_{o1} \) stabilizes at (M6 will be off under these conditions and \( v_{out} \approx V_{SS} \)).

\[
V_{DD} - V_{SD4}(sat) < v_{o1} < V_{DD}, \quad v_{G2} < V_{REF}, \quad i_1 < I_{SS} \quad \text{and} \quad i_2 > 0
\]
**Initial Operating States - Continued**

8.) Finally if $v_{G2} << V_{REF}$, then $i_1 = I_{SS}$ and $i_2 = 0$ and

$$v_{o1} = V_{DD} \quad \text{and} \quad v_{out} = V_{SS}.$$ 

Summary of the Initial Operating States of the Two-Stage, Open-Loop Comparator using a N-channel, Source-coupled Input Pair:

<table>
<thead>
<tr>
<th>Conditions</th>
<th>Initial State of $v_{o1}$</th>
<th>Initial State of $v_{out}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$v_{G1}&gt;V_{G2}$, $i_1&lt;I_{SS}$ and $i_2&gt;0$</td>
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<td>$V_{SS}$</td>
</tr>
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<tr>
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<td>$v_{o1}=V_{G2}-V_{GS2,act}(I_{SS}/2)$, $\approx V_{SS}$ if M5 active</td>
<td>Eq. (19), Sec. 5.1 for PMOS</td>
</tr>
<tr>
<td>$v_{G1}&lt;&lt;V_{G2}$, $i_1&gt;0$ and $i_2&lt;I_{SS}$</td>
<td>$V_{SS}$</td>
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</tr>
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TO BE CONTINUED IN THE NEXT LECTURE