LECTURE 380 – TWO-STAGE OPEN-LOOP COMPARATORS - II
(READING: AH – 445-461)

Trip Point of an Inverter

In order to determine the propagation delay time, it is necessary to know when the second stage of the two-stage comparator begins to "turn on".

Second stage:

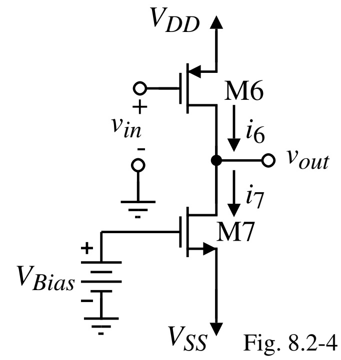

Fig. 8.2-4

Trip point:

Assume that M6 and M7 are saturated. (We know that the steepest slope occurs for this condition.)

Equate i_6 to i_7 and solve for v_{in} which becomes the trip point.

$$\therefore \qquad v_{in} = V_{TRP} = V_{DD} - |V_{TP}| - \sqrt{\frac{K_N(W_7/L_7)}{K_P(W_6/L_6)}}\,(V_{Bias} - V_{SS} - V_{TN})$$

Example:

If $W_7/L_7 = W_6/L_6$, $V_{DD} = 2.5$V, $V_{SS} = -2.5$V, and $V_{Bias} = 0$V the trip point for the circuit above is

$$V_{TRP} = 2.5 - 0.7 - \sqrt{110/50}\,(0 + 2.5 - 0.7) = -0.870\text{V}$$

Propagation Delay Time of a Slewing, Two-Stage, Open-Loop Comparator

Previously we calculated the propagation delay time for a nonslewing comparator.

If the comparator slews, then the propagation delay time is found from

$$i_i = C_i\frac{dv_i}{dt_i} = C_i\,\frac{\Delta v_i}{\Delta t_i}$$

where

C_i is the capacitance to ground at the output of the i-th stage

The propagation delay time of the i-th stage is,

$$t_i = \Delta t_i = C_i\frac{\Delta V_i}{I_i}$$

The propagation delay time is found by summing the delays of each stage.

$$t_p = t_1 + t_2 + t_3 + \cdots$$

Example 2-5 - Propagation Time Delay of a Two-Stage, Open-Loop Comparator

For the two-stage comparator shown assume that C_I = 0.2pF and C_{II} = 5pF. Also, assume that v_{G1} = 0V and that v_{G2} has the waveform shown. If the input voltage is large enough to cause slew to dominate, find the propagation time delay of the rising and falling output of the comparator and give the propagation time delay of the comparator.

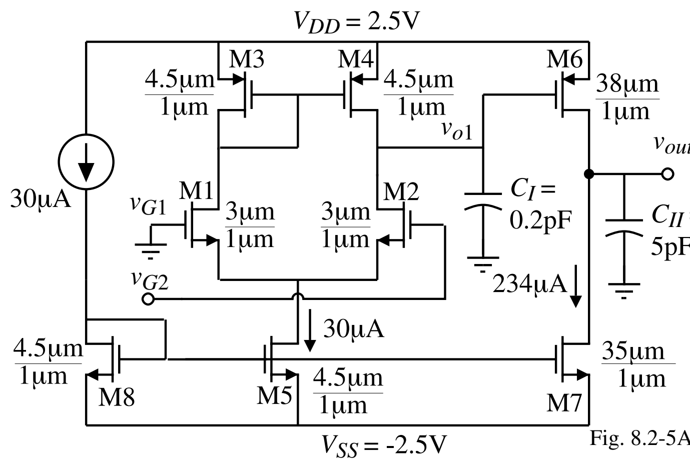

Fig. 8.2-5A

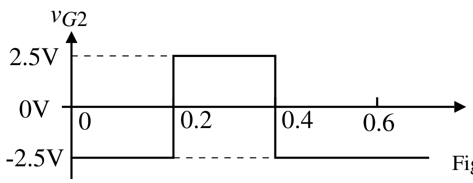

Fig. 8.2-5

Solution

1.) Total delay = sum of the first and second stage delays, t_1 and t_2

2.) First, consider the change of v_{G2} from -2.5V to 2.5V at 0.2µs.

The last row of Table 8.2-1 gives v_{o1} = +2.5V and v_{out} = -2.5V

3.) t_{f1}, requires C_I, ΔV_{o1}, and I_5. C_I = 0.2pF, I_5 = 30µA and ΔV_1 can be calculated by finding the trip point of the output stage/

Example 2-5 - Continued

4.) The trip point of the output stage by setting the current of M6 when saturated equal to 234µA.

$$\frac{\beta_6}{2}(V_{SG6}-|V_{TP}|)^2 = 234\mu A \;\rightarrow\; V_{SG6} = 0.7 + \sqrt{\frac{234\cdot 2}{110\cdot 38}} = 1.035V$$

Therefore, the trip point of the second stage is V_{TRP2} = 2.5 - 1.035 = 1.465V

Therefore, ΔV_1 = 2.5V - 1.465V = V_{SG6} = 1.035V. Thus the falling propagation time delay of the first stage is

$$t_{fo1} = 0.2pF\left(\frac{1.035V}{30\mu A}\right) = 6.9ns$$

5.) The rising propagation time delay of the second stage requires C_{II}, ΔV_{out}, and I_6. C_{II} is given as 5pF, ΔV_{out} = 2.5V (assuming the trip point of the circuit connected to the output of the comparator is 0V), and I_6 can be found as follows:

$$V_{G6}(\text{guess}) \approx 0.5[V_{G6}(I_6{=}234\mu A) + V_{G6}(\text{min})]$$

$$V_{G6}(\text{min}) = V_{G1} - V_{GS1}(I_{SS}/2) + V_{DS2} \approx -V_{GS1}(I_{SS}/2) = -0.7 - \sqrt{\frac{2\cdot 15}{110\cdot 3}} = -1.00V$$

$$V_{G6}(\text{guess}) \approx 0.5(1.465V-1.00V) = 0.232V$$

Therefore V_{SG6} = 2.27V and $I_6 = \frac{\beta_6}{2}(V_{SG6}-|V_{TP}|)^2 = \frac{38\cdot 50}{2}\,(2.27 - 0.7)^2 = 2{,}342\mu A$

Example 2-5 - Continued

6.) The rising propagation time delay for the output can expressed as

$$t_{rout} = 5\text{pF}\left(\frac{2.5\text{V}}{2{,}342\mu\text{A}-234\mu\text{A}}\right) = 5.93\text{ns}$$

Thus the total propagation time delay of the rising output of the comparator is approximately 12.8ns and most of this delay is attributable to the first stage.

7.) Next consider the change of v_{G2} from 2.5V to -2.5V which occurs at 0.4µs. We shall assume that v_{G2} has been at 2.5V long enough for the conditions of Table 8.2-1 to be valid. Therefore, $v_{o1} \approx V_{SS}$ = -2.5V and $v_{out} \approx V_{DD}$. The propagation time delays for the first and second stages are calculated as

$$t_{ro1} = 0.2\text{pF}\left(\frac{1.465\text{V}-(-1.13\text{V})}{30\mu\text{A}}\right) = 17.3\text{ns}$$

$$t_{fout} = 5\text{pF}\left(\frac{2.5\text{V}}{234\mu\text{A}}\right) = 53.42\text{ns}$$

8.) The total propagation time delay of the falling output is 70.72ns. Taking the average of the rising and falling propagation time delays gives a propagation time delay for this two-stage, open-loop comparator of about 41.76ns.

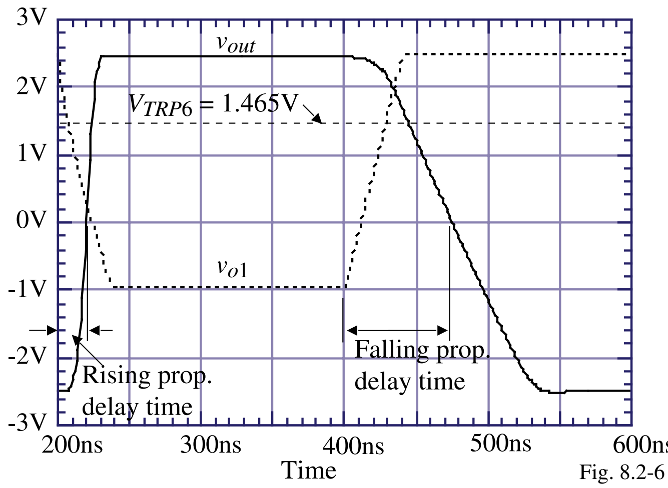

Fig. 8.2-6

Design of a Two-Stage, Open-Loop Comparator

Table 8.2-2 Design of the Two-Stage, Open-Loop Comparator of Fig. 8.2-3 for a Linear Response.

Specifications: t_p, C_{II}, V_{in}(min), V_{OH}, V_{OL}, V_{icm}^+, V_{icm}^-, and overdrive Constraints: Technology, V_{DD} and V_{SS}

Step	Design Relationships	Comments
1	$\lvert p_I\rvert = \lvert p_{II}\rvert = \frac{1}{t_p\sqrt{mk}}$, and $I_7 = I_6 = \frac{\lvert p_{II}\rvert C_{II}}{\lambda_N+\lambda_P}$	Choose m = 1
2	$\frac{W_6}{L_6} = \frac{2\cdot I_6}{K_P'(V_{SD6}(\text{sat}))^2}$ and $\frac{W_7}{L_7} = \frac{2\cdot I_7}{K_N'(V_{DS7}(\text{sat}))^2}$	$V_{SD6}(\text{sat}) = V_{DD}-V_{OH}$ $V_{DS7}(\text{sat}) = V_{OL} - V_{SS}$
3	Guess C_I as 0.1pF to 0.5pF $\therefore I_5 = I_7\frac{2C_I}{C_{II}}$	A result of choosing m = 1. Will check C_I later
4	$\frac{W_3}{L_3} = \frac{W_4}{L_4} = \frac{I_5}{K_P'(V_{SG3}-\lvert V_{TP}\rvert)^2}$	$V_{SG3} = V_{DD}-V_{icm}^{+}+V_{TN}$
5	$g_{m1} = \frac{A_v(0)(g_{ds2}+g_{ds4})(g_{ds6}+g_{ds7})}{g_{m6}}$ $\frac{W_1}{L_1} = \frac{W_2}{L_2} = \frac{g_{m1}^2}{K_N I_5}$	$g_{m6} = \sqrt{\frac{2K_P' W_6 I_6}{L_6}}$ $A_v(0) = \frac{V_{OH}+V_{OL}}{V_{in}(\text{min})}$
6	Find C_I and check assumption $C_I = C_{gd2}+C_{gd4}+C_{gs6}+C_{bd2}+C_{bd4}$	If C_I is greater than the guess in step 3, then increase C_I and repeat steps 4 through 6
7	$V_{DS5}(\text{sat}) = V_{icm}^{-}-V_{GS1}-V_{SS}$ $\frac{W_5}{L_5} = \frac{2\cdot I_5}{K_N'(V_{DS5}(\text{sat}))^2}$	If V_{DS5}(sat) is less than 100mV, increase W_1/L_1.

Example 2-6 - Two-Stage, Open-Loop Comparator Design for a Linear Response.

Assume the specifications of the comparator shown are given below.

$t_p = 50\text{ns}$ $\quad V_{OH} = 2\text{V}$ $\quad V_{OL} = -2\text{V}$

$V_{DD} = 2.5\text{V}$ $\quad V_{SS} = -2.5\text{V}$ $\quad C_{II} = 5\text{pF}$

$V_{in}(\text{min}) = 1\text{mV}$ $\quad V_{icm}^{+} = 2\text{V}$ $\quad V_{icm}^{-} = -1.25\text{V}$

Also assume that the overdrive will be a factor of 10. Use this architecture to achieve the above specifications and assume that all channel lengths are to be 1µm.

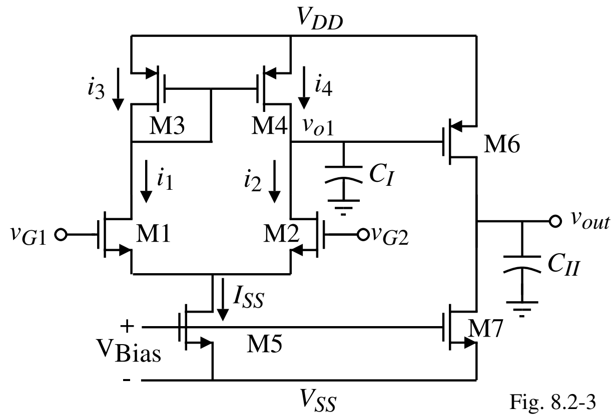

Fig. 8.2-3

Solution

Following the procedure outlined in Table 8.2-2, we choose $m = 1$ to get

$$|p_I| = |p_{II}| = \frac{10^9}{50\sqrt{10}} = 6.32\text{x}10^6 \text{ rads/sec}$$

This gives

$$I_6 = I_7 = \frac{6.32\text{x}10^6 \cdot 5\text{x}10^{-12}}{0.04+0.05} = 351\mu\text{A} \rightarrow \quad I_6 = I_7 = 400\mu\text{A}$$

Therefore,

$$\frac{W_6}{L_6} = \frac{2\cdot 400}{(0.5)^2 \cdot 50} = 64 \quad \text{and} \quad \frac{W_7}{L_7} = \frac{2\cdot 400}{(0.5)^2 \cdot 110} = 29$$

Example 2-6 - Continued

Next, we guess $C_I = 0.2\text{pF}$. This gives $I_5 = 32\mu\text{A}$ and we will increase it to 40µA for a margin of safety. Step 4 gives V_{SG3} as 1.2V which results in

$$\frac{W_3}{L_3} = \frac{W_4}{L_4} = \frac{40}{50(1.2\text{-}0.7)^2} = 3.2 \quad \rightarrow \quad \frac{W_3}{L_3} = \frac{W_4}{L_4} = 4$$

The desired gain is found to be 4000 which gives an input transconductance of

$$g_{m1} = \frac{4000\cdot 0.09\cdot 20}{44.44} = 162\mu\text{S}$$

This gives the *W*/*L* ratios of M1 and M2 as

$$\frac{W_1}{L_1} = \frac{W_2}{L_2} = \frac{(162)^2}{110\cdot 40} = 5.96 \quad \rightarrow \quad \frac{W_1}{L_1} = \frac{W_2}{L_2} = 6$$

To check the guess for C_I we need to calculate it which is done as

$$C_I = C_{gd2}+C_{gd4}+C_{gs6}+C_{bd2}+C_{bd4} = 0.9\text{fF}+1.3\text{fF}+119.5\text{fF}+20.4\text{fF}+36.8\text{fF} = 178.9\text{fF}$$

which is less than what was guessed so we will make no changes.

Example 2-6 - Continued

Finally, the W/L value of M5 is found by finding V_{GS1} as 0.946V which gives $V_{DS5}(\text{sat}) = 0.304\text{V}$. This gives

$$\frac{W_5}{L_5} = \frac{2\cdot 40}{(0.304)^2\cdot 110} = 7.87 \approx 8$$

Obviously, M5 and M7 cannot be connected gate-gate and source-source. The value of I_5 and I_7 must be derived separately as illustrated below. The W values are summarized below assuming that all channel lengths are 1μm.

$W_1 = W_2 = 6\mu\text{m}$ $W_3 = W_4 = 4\mu\text{m}$ $W_5 = 8\mu\text{m}$ $W_6 = 64\mu\text{m}$ $W_7 = 29\mu\text{m}$

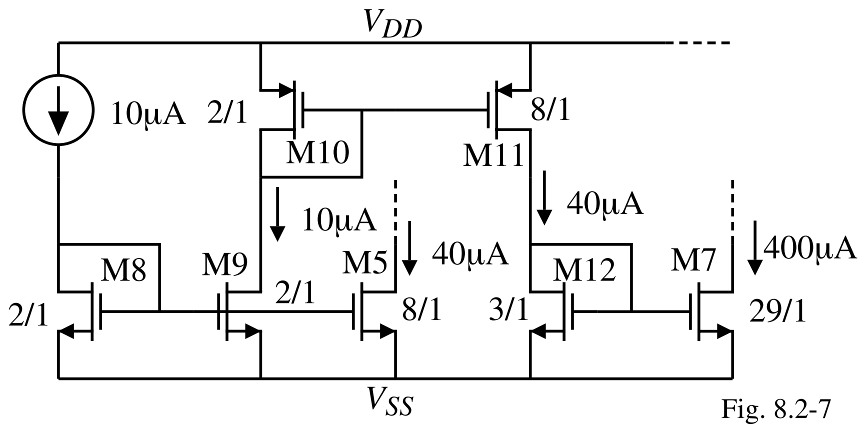

Fig. 8.2-7

Design of a Two-Stage Comparator for a Slewing Response

Table 8.2-3 Two-Stage, Open-Loop Comparator Design for a Slewing Response.

Specifications: t_p, C_{II}, $V_{in}(\text{min})$, V_{OH}, V_{OL}, V_{icm}^+, V_{icm}^- Constraints: Technology, V_{DD} and V_{SS}

Step	Design Relationships	Comments
1	$I_7 = I_6 = C_{II}\cdot\frac{dv_{out}}{dt} = \frac{C_{II}(V_{OH}-V_{OL})}{t_p}$	Assume the trip point of the output is $(V_{OH}-V_{OL})/2$.
2	$\frac{W_6}{L_6} = \frac{2\cdot I_6}{K_P'(V_{SD6}(\text{sat}))^2}$ and $\frac{W_7}{L_7} = \frac{2\cdot I_7}{K_N'(V_{DS7}(\text{sat}))^2}$	$V_{SD6}(\text{sat}) = V_{DD}-V_{OH}$ $V_{DS7}(\text{sat}) = V_{OL} - V_{SS}$
3	Guess C_I as 0.1pF to 0.5pF $\therefore\ I_5 = I_7\frac{2C_I}{C_{II}}$	Typically $0.1\text{pf} < C_I < 0.5\text{pF}$
4	$I_5 = C_I\cdot\frac{dv_{o1}}{dt} \approx \frac{C_I(V_{OH}-V_{OL})}{t_p}$	Assume that v_{o1} swings between V_{OH} and V_{OL}.
5	$\frac{W_3}{L_3} = \frac{W_4}{L_4} = \frac{I_5}{K_P'(V_{SG3}-\lvert V_{TP}\rvert)^2}$	$V_{SG3} = V_{DD}-V_{icm}^+ + V_{TN}$
6	$g_{m1} = \frac{A_v(0)(g_{ds2}+g_{ds4})(g_{ds6}+g_{ds7})}{g_{m6}}$ $\frac{W_1}{L_1} = \frac{W_2}{L_2} = \frac{g_{m1}^2}{K_N I_5}$	$g_{m6} = \sqrt{\frac{2K_P' W_6 I_6}{L_6}}$ $A_v(0) = \frac{V_{OH}+V_{OL}}{V_{in}(\text{min})}$
7	Find C_I and check assumption $C_I = C_{gd2}+C_{gd4}+C_{gs6}+C_{bd2}+C_{bd4}$	If C_I is greater than the guess in step 3, increase the value of C_I and repeat steps 4 through 6
8	$V_{DS5}(\text{sat}) = V_{icm}^- - V_{GS1} - V_{SS}$ $\frac{W_5}{L_5} = \frac{2\cdot I_5}{K_N'(V_{DS5}(\text{sat}))^2}$	If $V_{DS5}(\text{sat})$ is less than 100mV, increase W_1/L_1.

Example 2-7 - Two-Stage, Open-Loop Comparator Design for a Slewing Response

Assume the specifications of Fig. 8.2-3 are given below.

t_p = 50ns V_{OH} = 2V V_{OL} = -2V V_{DD} = 2.5V V_{SS} = -2.5V

C_{II} = 5pF V_{in}(min) = 1mV V_{icm}^+ = 2V V_{icm}^- = -1.25V

Design a two-stage, open-loop comparator using the circuit of Fig. 8.2-3 to the above specifications and assume all channel lengths are to be 1µm.

Solution

Following the procedure outlined in Table 8.2-3, we calculate I_6 and I_7 as

$$I_6 = I_7 = \frac{5\text{x}10^{-12}\cdot 4}{50\text{x}10^{-9}} = 400\mu\text{A}$$

Therefore,

$$\frac{W_6}{L_6} = \frac{2\cdot 400}{(0.5)^2\cdot 50} = 64 \qquad \text{and} \frac{W_7}{L_7} = \frac{2\cdot 400}{(0.5)^2\cdot 110} = 29$$

Next, we guess C_I = 0.2pF. This gives

$$I_5 = \frac{0.2\text{pF}(4\text{V})}{50\text{ns}} = 16\mu\text{A} \quad \rightarrow \quad I_5 = 20\mu\text{A}$$

Step 5 gives V_{SG3} as 1.2V which results in

$$\frac{W_3}{L_3} = \frac{W_4}{L_4} = \frac{20}{50(1.2\text{-}0.7)^2} = 1.6 \quad \rightarrow \quad \frac{W_3}{L_3} = \frac{W_4}{L_4} = 2$$

Example 2-7 - Continued

The desired gain is found to be 4000 which gives an input transconductance of

$$g_{m1} = \frac{4000\cdot 0.09\cdot 10}{44.44} = 81\mu\text{S}$$

This gives the *W*/*L* ratios of M1 and M2 as

$$\frac{W_3}{L_3} = \frac{W_4}{L_4} = \frac{(81)^2}{110\cdot 40} = 1.49 \quad \rightarrow \quad \frac{W_1}{L_1} = \frac{W_2}{L_2} = 2$$

To check the guess for C_I we need to calculate it which done as

$$C_I = C_{gd2}+C_{gd4}+C_{gs6}+C_{bd2}+C_{bd4} = 0.9\text{fF}+0.4\text{fF}+119.5\text{fF}+20.4\text{fF}+15.3\text{fF} = 156.5\text{fF}$$

which is less than what was guessed.

Finally, the *W*/*L* value of M5 is found by finding V_{GS1} as 1.00V which gives V_{DS5}(sat) = 0.25V. This gives

$$\frac{W_5}{L_5} = \frac{2\cdot 20}{(0.25)^2\cdot 110} = 5.8 \approx 6$$

As in the previous example, M5 and M7 cannot be connected gate-gate and source-source and a scheme like that of Example 8.2-6 must be used. The *W* values are summarized below assuming that all channel lengths are 1µm.

$W_1 = W_2$ = 2µm $W_3 = W_4$ = 4µm W_5 = 6µm W_6 = 64µm W_7 = 29µm

SUMMARY

- The two-stage, open-loop comparator has two poles which should as large as possible
- The transient response of a two-stage, open-loop comparator will be limited by either the bandwidth or the slew rate
- It is important to know the initial states of a two-stage, open-loop comparator when finding the propagation delay time
- If the comparator is gainbandwidth limited then the poles should be as large as possible for minimum propagation delay time
- If the comparator is slew rate limited, then the current sinking and sourcing ability should be as large as possible