LECTURE 400 – DISCRETE-TIME COMPARATORS (LATCHES)

(READING: AH – 475-483)

Objective

The objective of this presentation is:

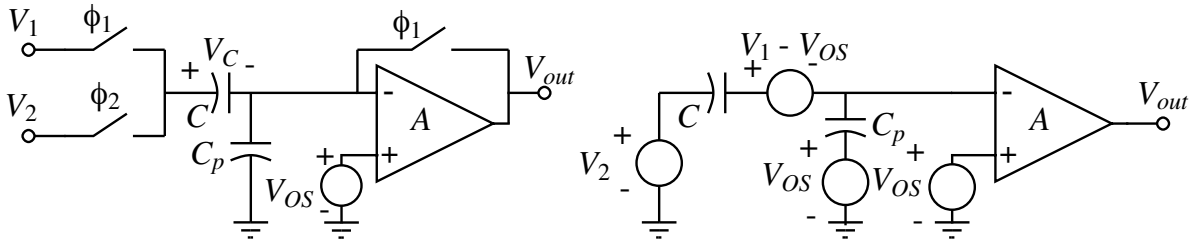
1.) Illustrate discrete-time comparators

2.) Estimate the propagation delay time

Outline

- Switched capacitor comparators
- Regenerative comparators (latches)
- Summary

Switched Capacitor Comparator



A switched capacitor comparator

Equivalent circuit when the ϕ_2 switches are closed

Fig. 8.5-1

ϕ_1 Phase:

The V_1 input is sampled and the dc input offset voltage is autozeroed.

$$V_C(\phi_1) = V_1 - V_{OS} \quad \text{and} \quad V_{Cp}(\phi_1) = V_{OS}$$

ϕ_2 Phase:

$$V_{out}(\phi_2) = -A\left[\frac{V_2 C}{C+C_p} - \frac{(V_1-V_{OS})C}{C+C_p} + \frac{V_{OS}C_p}{C+C_p}\right] + AV_{OS}$$

$$= -A\left[(V_2-V_1)\frac{C}{C+C_p} + V_{OS}\left(\frac{C}{C+C_p} + \frac{C_p}{C+C_p}\right)\right] + AV_{OS} = -A(V_2-V_1)\frac{C}{C+C_p} \approx A(V_1-V_2)$$

if C_p is smaller than C.

Differential-In, Differential-Out Switched Capacitor Comparator

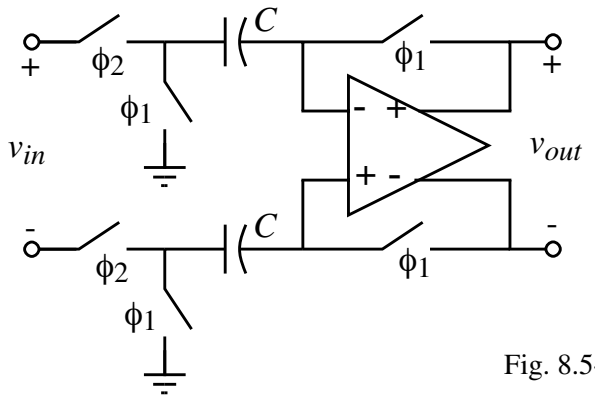


Fig. 8.5-2

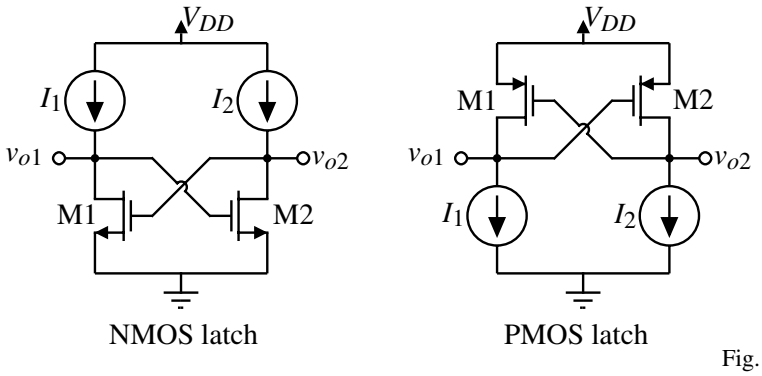
Comments:

- Reduces the influence of charge injection
- Eliminates even harmonics

Regenerative Comparators

Regenerative comparators use positive feedback to accomplish the comparison of two signals. Latches have a faster switching speed that the previous bistable comparators.

NMOS and PMOS latch:



NMOS latch PMOS latch

Fig. 8.5-3

How is the input applied to a latch?

The inputs are initially applied to the outputs of the latch.

V_{o1}' = initial input applied to v_{o1}

V_{o2}' = initial input applied to v_{o2}

Step Response of a Latch

Circuit:

R_i and C_i are the resistance and capacitance seen to ground from the i-th transistor.

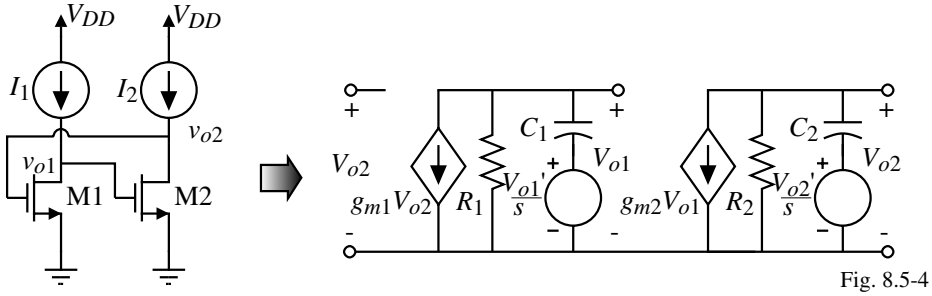


Fig. 8.5-4

Nodal equations:

$$g_{m1}V_{o2}+G_1V_{o1}+sC_1\left(V_{o1}-\frac{V_{o1}'}{s}\right)=g_{m1}V_{o2}+G_1V_{o1}+sC_1V_{o1}-C_1V_{o1}'=0$$

$$g_{m2}V_{o1}+G_2V_{o2}+sC_2\left(V_{o2}-\frac{V_{o2}'}{s}\right)=g_{m2}V_{o1}+G_2V_{o2}+sC_2V_{o2}-C_2V_{o2}'=0$$

Solving for V_{o1} and V_{o2} gives,

$$V_{o1}=\frac{R_1C_1}{sR_1C_1+1}V_{o1}'-\frac{g_{m1}R_1}{sR_1C_1+1}V_{o2}=\frac{\tau_1}{s\tau_1+1}V_{o1}'-\frac{g_{m1}R_1}{s\tau_1+1}V_{o2}$$

$$V_{o2}=\frac{R_2C_2}{sR_2C_2+1}V_{o2}'-\frac{g_{m2}R_2}{sR_2C_2+1}V_{o1}=\frac{\tau_2}{s\tau_2+1}V_{o2}'-\frac{g_{m2}R_2}{s\tau_2+1}V_{o1}$$

Defining the output, ΔV_o, and input, ΔV_i, as

$$\Delta V_o=V_{o2}-V_{o1} \quad \text{and} \quad \Delta V_i=V_{o2}'-V_{o1}'$$

Step Response of the Latch - Continued

Solving for ΔV_o gives,

$$\Delta V_o=V_{o2}-V_{o1}=\frac{\tau}{s\tau+1}\Delta V_i+\frac{g_mR}{s\tau+1}\Delta V_o$$

or

$$\Delta V_o=\frac{\tau\,\Delta V_i}{s\tau+(1-g_mR)}=\frac{\frac{\tau\,\Delta V_i}{1-g_mR}}{\frac{s\tau}{1-g_mR}+1}=\frac{\tau'\,\Delta V_i}{s\tau'+1}$$

where

$$\tau'=\frac{\tau}{1-g_mR}$$

Taking the inverse Laplace transform gives

$$\Delta v_o(t)=\Delta V_i'\,e^{-t/\tau}=\Delta V_i\,e^{-t(1-g_mR)/\tau}\approx e^{g_mRt/\tau}\Delta V_i, \quad \text{if } g_mR>>1.$$

Define the latch time constant as

$$\tau_L\approx\frac{\tau}{g_mR}=\frac{C}{g_m}=\frac{0.67WLC_{ox}}{\sqrt{2K'(W/L)I}}=0.67C_{ox}\sqrt{\frac{WL^3}{2K'I}}$$

if $C\approx C_{gs}$.

$$\therefore \quad \Delta V_{out}(t)=e^{t/\tau_L}\Delta V_i$$

Step Response of a Latch - Continued

Normalize the output voltage by $(V_{OH}\text{-}V_{OL})$ to get

$$\frac{\Delta V_{out}(t)}{V_{OH}\text{-}V_{OL}} = e^{t/\tau_L}\frac{\Delta V_i}{V_{OH}\text{-}V_{OL}}$$

which is plotted as,

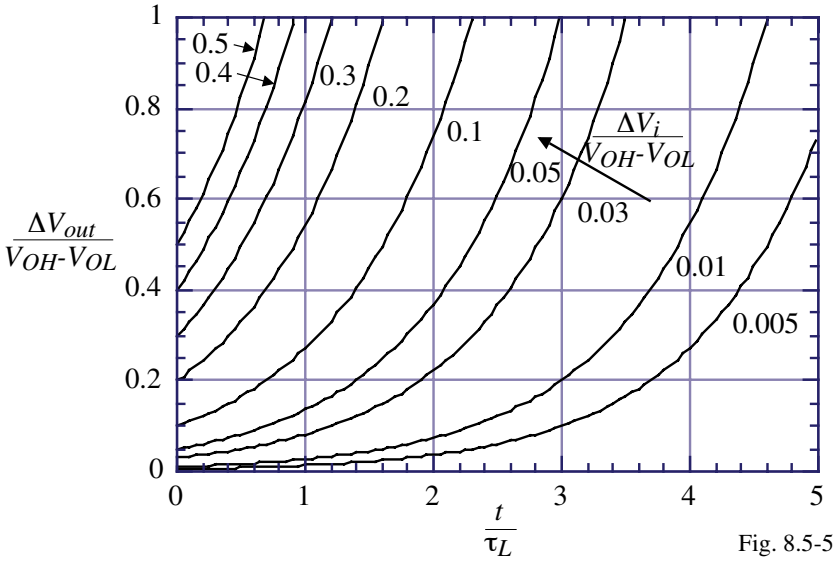


Fig. 8.5-5

The propagation delay time is $t_p = \tau_L\, ln\left(\frac{V_{OH}\text{-}\,V_{OL}}{2\Delta V_i}\right)$

Example 8.5-1 - Time domain characteristics of a latch.

Find the time it takes from the time the latch is enabled until the output voltage, ΔV_{out}, equals $V_{OH}\text{-}V_{OL}$ if the W/L of the latch NMOS transistors is 10μm/1μm and the latch dc current is 10μA when $\Delta V_i = 0.1(V_{OH}\text{-}V_{OL})$ and $\Delta V_i = 0.01(V_{OH}\text{-}V_{OL})$. Find the propagation time delay (ΔV_{out}=$0.5(V_{OH}\text{-}V_{OL})$) for the latch for each of these conditions.

Solution

The transconductance of the latch transistors is

$$g_m = \sqrt{2\cdot 110\cdot 10\cdot 10} = 148\mu S$$

The output conductance is 0.4μS which gives g_mR of 59.2V/V. Since g_mR is greater than 1, we can use the above results. Therefore the latch time constant is found as

$$\tau_L = 0.67C_{ox}\sqrt{\frac{WL^3}{2K'I}} = 0.67(24\text{x}10^{-4})\sqrt{\frac{(10\cdot 1)\text{x}10^{-18}}{2\cdot 110\text{x}10^{-6}\cdot 10\text{x}10^{-6}}} = 108\text{ns}$$

If we assume that the propagation time delay is the time for the output to reach $(V_{OH}\text{-}V_{OL})$, then for $\Delta V_i = 0.01(V_{OH}\text{-}V_{OL})$ that $t_p = 4.602\tau_L = 497$ns and for $\Delta V_i = 0.1(V_{OH}\text{-}V_{OL})$ that $t_p = 2.306\tau_L = 249$ns.

If we assume that the propagation time delay is the time when the output is $0.5(V_{OH}\text{-}V_{OL})$, then using the above results or Fig. 8.5-5 we find for $\Delta V_i = 0.01(V_{OH}\text{-}V_{OL})$ that $t_p = 3.91\tau_L = 422$ns and for $\Delta V_i = 0.1(V_{OH}\text{-}V_{OL})$ that $t_p = 1.61\tau_L = 174$ns.

Comparator using a Latch with a Built-In Threshold[†]

How does it operate?

1.) Devices in shaded region operate in the triode region.

2.) When the latch/reset goes high, the upper cross-coupled inverter-latch regenerates. The drain currents of M5 and M6 are steered to obtain a final state determined by the mismatch between the R_1 and R_2 resistances.

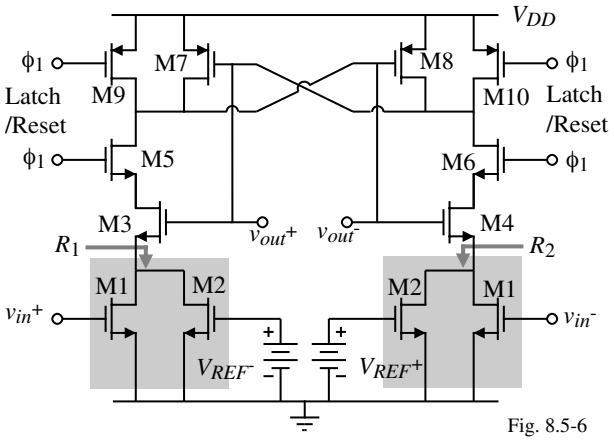


Fig. 8.5-6

$$\frac{1}{R_1} = K_N\left[\frac{W_1}{L}(v_{in}^+ - V_T) + \frac{W_2}{L}(V_{REF}^- - V_T)\right]$$

and

$$\frac{1}{R_2} = K_N\left[\frac{W_1}{L}(v_{in}^- - V_T) + \frac{W_2}{L}(V_{REF}^+ - V_T)\right]$$

3.) The input voltage which causes R_1 and R_2 to be equal is given by

$$v_{in}(\text{threshold}) = (W_2/W_1)V_{REF}$$

$W_2/W_1 = 1/4$ generates a threshold of $\pm 0.25V_{REF}$.

Performance → 20Ms/s & 200μW

[†] T.B. Cho and P.R. Gray, "A 10b, 20Msamples/s, 35mW pipeline A/D Converter," *IEEE J. Solid-State Circuits*, vol. 30, no. 3, pp. 166-172, March 1995.

Simple, Low Power Latched Comparator[†]

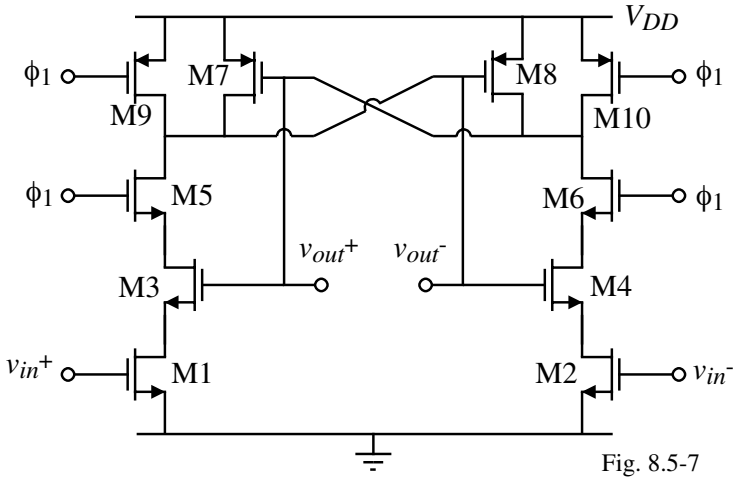


Fig. 8.5-7

Dissipated 50μW when clocked at 2MHz.

[†] A. Coban, "1.5V, 1mW, 98-dB Delta-Sigma ADC", Ph.D. dissertation, School of ECE, Georgia Tech, Atlanta, GA 30332-0250.

Dynamic Latch

Circuit:

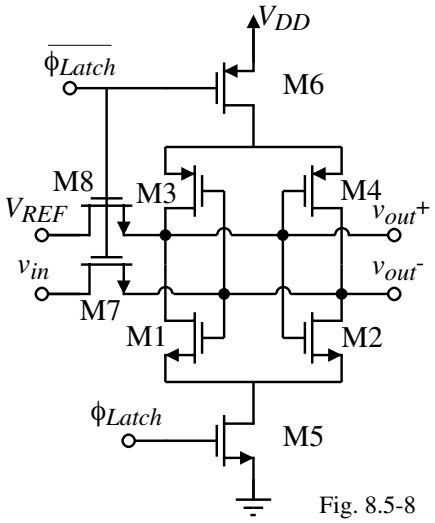


Fig. 8.5-8

Input offset voltage distribution:

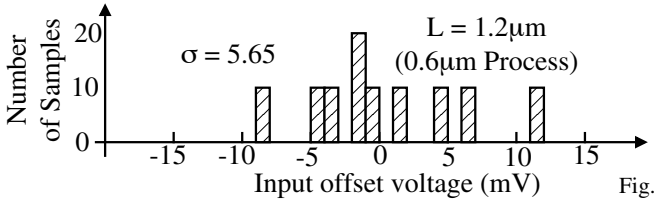


Fig. 8.5-9

Power dissipation/sampling rate = 4.3μW/Ms/s

SUMMARY

- Discrete-time comparators must work with clocks
- Switched capacitor comparators use op amps to transfer charge and autozero
- Regenerative comparators (latches) use positive feedback
- The propagation delay of the regenerative comparator is slow at the beginning and speeds up rapidly as time increases
- The highest speed comparators will use a combination of open-loop comparators and latches